

Key Features

Processor

- XuanTie C906 RISC-V CPU

Memory

- 16-bit DDR2/DDR3/DDR3L, maximum capability up to 256 MB
- SD3.0, eMMC4.41, SPI Nor Flash

Video Engine

- Video decoding
 - H.265 up to 1920x1080@60fps
 - H.264 up to 1920x1080@60fps
 - H.263, MPEG-1/2/4, VC-1, up to 1080p@60fps
- Image decoding
 - JPEG up to 1080p@60fps
- Video encoding
 - JPEG/MJPEG up to 1920x1080@60fps
 - Maximum resolution: 8192x8192
 - Supports input picture scaling. The scaling ratio for width and height is 0.25 to 8.

Video Output

- 1 x RGB888 output interface up to 1920 x 1080@60fps
- Dual link LVDS interface up to 1920 x 1080@60fps
- 4-lane MIPI DSI interface up to 1920 x 1200@60fps

Audio

- 2 DACs and 1 ADC
- Analog audio interfaces: MICIN1P/N, FMINL, HPOUTL/R
- Digital audio interfaces: I2S/PCM, DMIC, OWA IN/OUT

Peripherals Interfaces

- USB2.0 DRD x 1
- USB2.0 Host x 1
- SPI x 2
- UART x 6
- TWI x 4
- PWM (8-ch)
- GPADC (1-ch)
- GPIO_ADC (2-ch, GPIO_ADC pad can be used by GPIO)
- IR TX&RX, LEDC, SDIO3.0

Security Subsystem

- AES, DES, and 3DES encryption and decryption algorithms
- MD5, SHA, and HMAC tamper proofing
- RSA signature and verification algorithms
- Hardware random number generator
- Integrated 2 Kbits eFuse storage space

Device Summary

Orderable Device(s)	Package
F135MX-XXX	QFP 128 pins Body size: 14 mm x 14 mm Maximum height: 1.60 mm

Revision History

Revision	Date	Author	Description
0.10	January 7, 2025	AWA1896	Draft Version
0.11	April 28, 2025	AWA1896	1. Add Table 4-9. 2. Update section 2.7.1. 3. Update section 4.11.4. 4. Update section 3.1.5. 5. Update Table 4-26.

Content

Key Features	1
Revision History	i
Content	ii
Figures	vi
Tables	viii
About This Document	1
1 Overview	3
2 Features	4
2.1 Processors	4
2.2 Memory	4
2.2.1 Boot ROM (BROM)	4
2.2.2 SDRAM	4
2.2.3 SD/MMC Host Controller (SMHC)	4
2.3 Graphics Processing	5
2.3.1 Display Engine (DE)	5
2.3.2 De-interlacer (DI)	5
2.3.3 Graphic 2D (G2D)	6
2.4 Video Engine	6
2.4.1 Video Decoder	6
2.4.2 Video Encoder	7
2.5 Video Output Interfaces	7
2.5.1 LCD	7
2.5.2 MIPI DSI	7
2.6 System Peripherals	7
2.6.1 Clock Controller Unit (CCU)	7
2.6.2 Power Reset Clock Management (PRCM)	7
2.6.3 RTC	7
2.6.4 Thermal Sensor Controller (THS)	8
2.6.5 LDO Power	8
2.6.6 Timer	8
2.6.7 High Speed Timer (HSTimer)	8
2.7 Audio	9
2.7.1 Audio Codec	9

2.7.2	I2S/PCM.....	9
2.7.3	DMIC	10
2.7.4	One Wire Audio (OWA)	10
2.8	Peripheral Interfaces	10
2.8.1	USB2.0 DRD	10
2.8.2	USB2.0 Host.....	11
2.8.3	UART	11
2.8.4	PWM	11
2.8.5	SPI and SPI_DBI	12
2.8.6	Two Wire Interface (TWI)	13
2.8.7	General Purpose ADC (GPADC)	13
2.8.8	GPIO_ADC	13
2.8.9	LED Controller (LEDC).....	13
2.8.10	Consumer Infrared Transmitter (IR_TX).....	14
2.8.11	Consumer Infrared Receiver (IR_RX)	14
2.9	Security.....	14
2.9.1	Crypto Engine (CE)	14
2.9.2	Security ID (SID)	14
2.10	Package	15
3	Pin Description.....	16
3.1	Pin Characteristics.....	16
3.1.1	SDRAM.....	17
3.1.2	System Control.....	19
3.1.3	RTC&PLL	19
3.1.4	DCXO	19
3.1.5	GPIO Groups	19
3.1.6	USB.....	22
3.1.7	Audio Codec	22
3.1.8	GPADC	23
3.1.9	Power	23
3.2	GPIO Multiplex Function	24
3.2.1	Port A.....	24
3.2.2	Port B	24
3.2.3	Port C	24
3.2.4	Port D	24
3.2.5	Port F.....	25
3.2.6	Port G	25

3.3	Detailed Signal Description	26
3.3.1	SDRAM.....	26
3.3.2	System Control.....	28
3.3.3	RTC&PLL	28
3.3.4	DCXO	28
3.3.5	SD Card/SDIO/eMMC	28
3.3.6	USB.....	29
3.3.7	I2S/PCM	29
3.3.8	Audio Codec	30
3.3.9	DMIC.....	30
3.3.10	OWA.....	31
3.3.11	GPADC.....	31
3.3.12	GPIO_ADC	31
3.3.13	LCD	31
3.3.14	LVDS.....	32
3.3.15	MIPI DSI.....	33
3.3.16	SPI&SPI DBI	33
3.3.17	UART	34
3.3.18	PWM	35
3.3.19	TWI	35
3.3.20	IR RX	36
3.3.21	IR TX	36
3.3.22	LEDC.....	36
3.3.23	JTAG.....	36
3.3.24	Interrupt	37
4	Electrical characteristics	38
4.1	Parameter Conditions	38
4.1.1	Minimum and Maximum Values	38
4.1.2	Typical Values.....	38
4.1.3	Temperature Definitions	38
4.2	Absolute Maximum Ratings	39
4.3	Recommended Operating Conditions	40
4.4	GPIO DC Electrical Characteristics	41
4.5	SMHC Electrical Characteristics.....	42
4.6	GPADC Electrical Characteristics.....	43
4.7	GPIO_ADC Electrical Characteristics.....	43
4.8	Audio Codec Electrical Characteristics	43

4.9	MIPI DPHY Electrical Characteristics	45
4.10	External Clock Source Electrical Characteristics	46
4.10.1	High-speed Crystal/Ceramic Resonator Characteristics	46
4.11	Interface Timing Characteristics	47
4.11.1	SMHC Interface Timing.....	47
4.11.2	LCD Interface Timing	52
4.11.3	MIPI DPHY Interface Timing	54
4.11.4	SPI Interface Timing	55
4.11.5	SPI-DBI Interface Timing	56
4.11.6	UART Interface Timing.....	58
4.11.7	I2C Interface Timing.....	59
4.11.8	I2S/PCM Interface Timing.....	60
4.11.9	DMIC Interface Timing	63
4.11.10	OWA Interface Timing.....	64
4.12	Power-Up and Power-Down Sequence	64
4.12.1	Power-Up Sequence	64
4.12.2	Power-Down Sequence	65
5	Temperature and Thermal Characteristics	67
5.1.1	Temperature	67
5.1.2	Package Thermal Characteristics	67
6	Pin Assignment	69
6.1.1	Pin Map	69
6.1.2	Package Dimension	70
7	Carrier, Storage and Backing Information.....	71
7.1	Carrier	71
7.2	Storage	72
7.2.1	Moisture Sensitivity Level (MSL)	72
7.2.2	Bagged Storage Conditions	73
7.2.3	Out-of-bag Duration	73
7.3	Baking.....	73
8	Reflow Profile	74
9	Part Marking	76
9.1	F135MX-XXX	76

Figures

Figure 1-1 System Block Diagram.....	3
Figure 4-1 SMHC Voltage Waveform	42
Figure 4-2 SMHC HS-SDR Mode Output Timing Diagram	47
Figure 4-3 SMHC HS-SDR Mode Input Timing Diagram	48
Figure 4-4 SMHC HS-DDR Mode Output Timing Diagram	48
Figure 4-5 SMHC HS-DDR Mode Input Timing Diagram	49
Figure 4-6 SMHC SDR104 Mode Host Output and Device Input Timing Diagram	50
Figure 4-7 SMHC SDR104 Mode Host Input and Device Output Timing Diagram	50
Figure 4-8 HV_IF Vertical Timing.....	52
Figure 4-9 HV_IF Horizontal Timing.....	53
Figure 4-10 MIPI DPHY Timing.....	54
Figure 4-11 SPI Writing Timing.....	55
Figure 4-12 SPI Reading Timing.....	55
Figure 4-13 DBI 3-line Serial Interface Timing.....	56
Figure 4-14 DBI 4-line Serial Interface Timing.....	57
Figure 4-15 UART RX Timing.....	58
Figure 4-16 UART nCTS Timing.....	59
Figure 4-17 UART nRTS Timing.....	59
Figure 4-18 TWI Timing.....	59
Figure 4-19 Data Output Timing of I2S/PCM in Master Mode	60
Figure 4-20 Data Input Timing of I2S/PCM in Master Mode	62
Figure 4-21 DMIC Timing	63
Figure 4-22 OWA Timing	64
Figure 4-23 Power-Up Sequence	65
Figure 4-24 Power-Down Sequence	66
Figure 6-1 Pin Map	69
Figure 6-2 Package Dimension	70
Figure 7-1 Tray Dimension Drawing	72
Figure 8-1 Lead-free Reflow Profile	74
Figure 8-2 Measuring the Reflow Soldering Process.....	75
Figure 9-1 F135MX-XXX Marking.....	76

Draft Version

ALLWINNER

Tables

Table 3-1 SDRAM Pin Characteristics	17
Table 3-2 System Control Pin Characteristics	19
Table 3-3 RTC&PLL Pin Characteristics	19
Table 3-4 DCXO Pin Characteristics	19
Table 3-5 Port A Pin Characteristics	19
Table 3-6 Port B Pin Characteristics	19
Table 3-7 Port C Pin Characteristics	20
Table 3-8 Port D Pin Characteristics	20
Table 3-9 Port F Pin Characteristics	21
Table 3-10 Port G Pin Characteristics	22
Table 3-11 USB Pin Characteristics	22
Table 3-12 Audio Codec Pin Characteristics	22
Table 3-13 GPADC Pin Characteristics	23
Table 3-14 Power Pin Characteristics	23
Table 3-15 Port A Multiplex Function	24
Table 3-16 Port B Multiplex Function	24
Table 3-17 Port C Multiplex Function	24
Table 3-18 Port D Multiplex Function	24
Table 3-19 Port F Multiplex Function	25
Table 3-20 Port G Multiplex Function	25
Table 3-21 SDRAM Signal Description	26
Table 3-22 System Control Signal Description	28
Table 3-23 RTC&PLL Signal Description	28
Table 3-24 DCXO Signal Description	28
Table 3-25 SD Card/SDIO/eMMC Signal Description	28
Table 3-26 USB Signal Description	29
Table 3-27 I2S/PCM Signal Description	29
Table 3-28 Audio Codec Signal Description	30
Table 3-29 DMIC Signal Description	30
Table 3-30 OWA Signal Description	31
Table 3-31 GPADC Signal Description	31

Table 3-32 GPIO_ADC Signal Description	31
Table 3-33 LCD Signal Description	31
Table 3-34 LVDS Signal Description	32
Table 3-35 MIPI DSI Signal Description	33
Table 3-36 SPI&SPI DBI Signal Description.....	33
Table 3-37 UART Signal Description	34
Table 3-38 PWM Signal Description.....	35
Table 3-39 TWI Signal Description.....	35
Table 3-40 IR RX Signal Description.....	36
Table 3-41 IR TX Signal Description.....	36
Table 3-42 LEDC Signal Description	36
Table 3-43 JTAG Signal Description	36
Table 3-44 Interrupt Signal Description.....	37
Table 4-1 Absolute Maximum Ratings.....	39
Table 4-2 Recommended Operating Conditions.....	40
Table 4-3 GPIO DC Electrical Characteristics ⁽¹⁾	41
Table 4-4 3.3 V SMHC Electrical Parameters.....	42
Table 4-5 1.8 V SMHC Electrical Parameters.....	42
Table 4-6 GPADC Electrical Characteristics	43
Table 4-7 GPIO_ADC Electrical Characteristics	43
Table 4-8 Audio Codec Typical Performance Parameters.....	43
Table 4-9 MIPI DPHY CTS Reference	45
Table 4-10 High-speed 24 MHz Crystal Requirements	46
Table 4-11 Crystal Circuit Parameters.....	46
Table 4-12 SMHC HS-SDR Mode Output Timing Constants.....	47
Table 4-13 SMHC HS-SDR Mode Input Timing Constants.....	48
Table 4-14 SMHC HS-DDR Mode Output Timing Constants	48
Table 4-15 SMHC HS-DDR Mode Input Timing Constants	49
Table 4-16 SMHC SDR104 Mode Host Output and Device Input Timing Constants	50
Table 4-17 SMHC SDR104 Mode Host Input and Device Output Timing Constants	51
Table 4-18 LCD HV_IF Timing Constants.....	53
Table 4-19 MIPI DPHY Timing Constants.....	54
Table 4-20 SPI Timing Constants.....	55

Table 4-21 DBI 3-line Serial Interface Write Timing Parameters	56
Table 4-22 DBI 3-line Serial Interface Read Timing Parameters	56
Table 4-23 DBI 4-line Serial Interface Write Timing Parameters	57
Table 4-24 DBI 4-line Serial Interface Read Timing Parameters	58
Table 4-25 UART Timing Constants	59
Table 4-26 TWI Timing Parameters	60
Table 4-27 Data Output Timing Parameters of I2S/PCM in Master Mode.....	61
Table 4-28 Data Input Timing Parameters of I2S/PCM in Master Mode.....	62
Table 4-29 DMIC Timing Constants	64
Table 4-30 OWA Timing Constants	64
Table 5-1 Operating and Storage Temperature	67
Table 5-2 Junction Temperature	67
Table 5-3 Package Thermal Characteristics	67
Table 7-1 Matrix Tray Carrier Information	71
Table 7-2 Packing Quantity Information.....	71
Table 7-3 MSL Summary.....	72
Table 7-4 Bagged Storage Conditions.....	73
Table 7-5 Out-of-bag Duration.....	73
Table 8-1 Lead-free Reflow Profile Conditions.....	74
Table 9-1 F135MX-XXX Marking Definitions.....	76

About This Document

Purpose and Scope

The documentation describes features of each module, pin/signal characteristics, current consumption, interface timing, thermal and package of the F135 family. For details about register descriptions of each module, see the *F135_User_Manual*.

Intended Audience

The document is intended for:

- Hardware designers and maintenance personnel for electronics
- Sales personnel for electronic parts and components

Related Documentation

For a complete listing of related documentation and development-support tools for the device, contact the Allwinner FAE or access the Allwinner Customer Service Platform by visiting <https://open.allwinnertech.com/>.

Revision Number Definition

Revision 0.10-0.1x

This document is released based on the experimental sample(s). Therefore, it may be modified, calibrated and supplemented hereafter.

All statements, information and recommendations in this document do not constitute any express or implied representation or warranty (including, but not limited to, the warranties of fitness for a particular purpose, merchantability, non-infringement, and accuracy and completeness of the document). Allwinner shall not be liable for any person's use of such information or/and this document.

If you have any questions about the document, please contact us to confirm and obtain the latest version.

Conventions

Symbol Conventions

The symbols that may be found in this document are defined as follows.

Symbol	Description
--------	-------------

Symbol	Description
 CAUTION	A caution means that damage to equipment is possible.
 NOTE	Provides additional information to emphasize or supplement important points of the main text.

Table Content Conventions

The table content conventions that may be found in this document are defined as follows.

Symbol	Description
-	The cell is blank.

Numerical System

The expressions of the data capacity, the frequency, and the data rate are described as follows.

Type	Symbol	Value
Data capacity	K	1024
	M	1,048,576
	G	1,073,741,824
Frequency, data rate	k	1000
	M	1,000,000
	G	1,000,000,000

FT/QA/QC Test

All Allwinner chips provided for clients have passed the following tests.

Test Item	Description
FT Test	FT test is the finished product testing after the chip is packaged, and it is a functional test of all modules for each produced chip.
QA Test	QA test is a system-level sampling test for good-quality chips. According to the application level of the chip, a certain percentage of good-quality chips are selected for system-level testing to make the chip work in a typical application scenario, and judge whether the chip works normally in this scenario.
QC Test	QC test is a module-level sampling test for good-quality chips. According to the chip application level, a certain percentage of good-quality chips are selected for module-level functional testing to monitor whether the chip production process is normal.

1 Overview

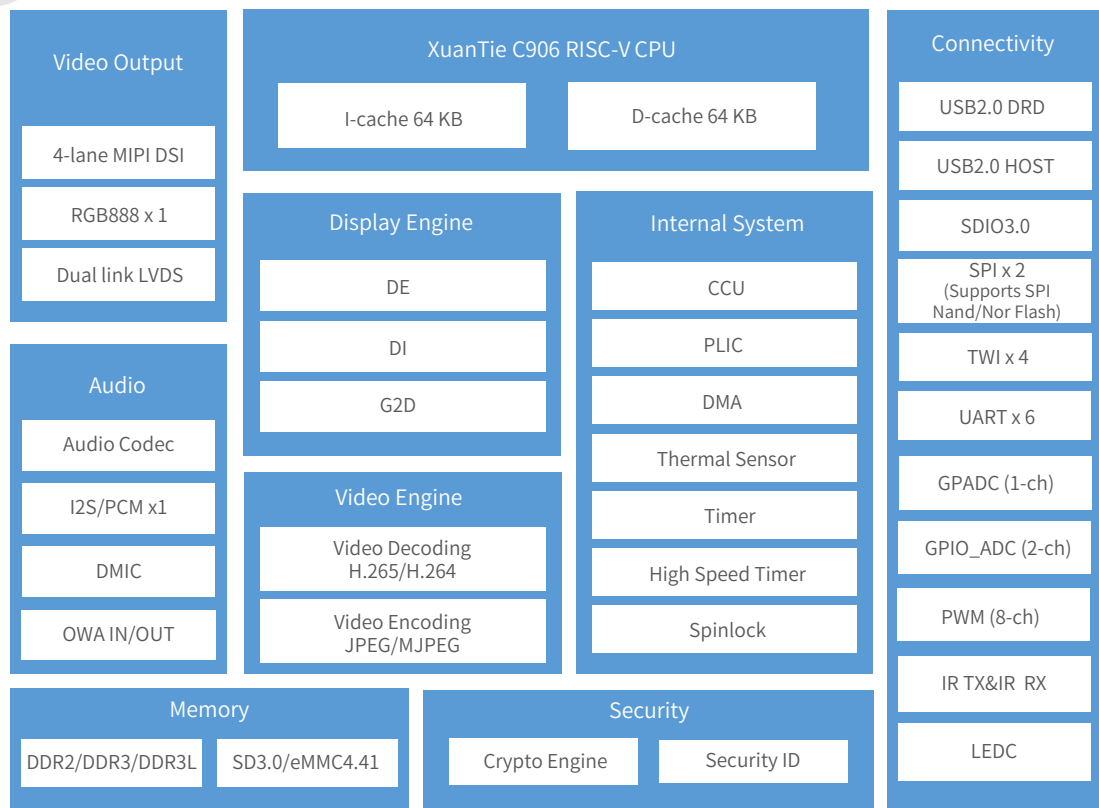
The F135 is an advanced application processor designed specifically for the video decoding market. It has a rich set of peripheral interfaces and many new features to provide a low-cost solution design.

The F135 has the following highlights:

- Integrated 64-bit RISC CPU processor provides powerful computing performance.
- Supports external DDR2/DDR3/DDR3L, maximum capability up to 256 MB.
- Supports H.265/H.264 1080p@60fps video decoding, and MJPEG/JPEG 1080p@60fps video encoding.
- Rich peripheral interfaces, such as USB, SDIO, UART, SPI, PWM, GPADC, GPIO_ADC, IR, and so on.
- Rich video interfaces, RGB888, Dual-LVDS, MIPI-DSI for Display.

The following figure shows the system block diagram for the device.

Figure 1-1 System Block Diagram



2 Features

2.1 Processors

- XuanTie C906 RISC-V CPU
- 64 KB I-cache + 64 KB D-cache

2.2 Memory

2.2.1 Boot ROM (BROM)

- On-chip memory
- Supports system boot from the following devices:
 - SD Card
 - eMMC
 - SPI NOR Flash (Quad Mode and Single Mode)
 - SPI NAND Flash
- Supports mandatory upgrade process through USB or SD card
- Supports GPIO pin and eFuse module to select the boot media type
- Supports BROM loads only certified firmware

2.2.2 SDRAM

- 16-bit DDR2/DDR3/DDR3L interface
- Clock frequency up to 533 MHz for DDR2
- Clock frequency up to 792 MHz for DDR3/DDR3L

2.2.3 SD/MMC Host Controller (SMHC)

- Three SD/MMC Host Controller (SMHC) interfaces
 - SMHC0, compliant with the protocol Secure Digital Memory (up to SD3.0)
 - SMHC1, compliant with the protocol Secure Digital I/O (up to SDIO3.0)
 - SMHC2, compliant with the protocol Multimedia Card (up to eMMC4.41)
- The SMHC0 and SMHC1 supports the following:
 - 1-bit or 4-bit data width
 - Maximum performance:
 - SDR mode 150 MHz@1.8 V IO pad
 - DDR mode 50 MHz@1.8 V IO pad
 - SDR mode 50 MHz@3.3 V IO pad

- The SMHC2 supports the following:
 - 1-bit or 4-bit data width
 - Maximum performance:
 - SDR mode 50 MHz@3.3V IO pad
 - DDR mode 50 MHz@3.3V IO pad
- Supports block size of 1 to 65535 bytes
- Supports hardware CRC generation and error detection
- Internal 1024-Bytes RX FIFO and 1024-Bytes TX FIFO
- Supports descriptor-based internal DMA controller

2.3 Graphics Processing

2.3.1 Display Engine (DE)

- Output size up to 2048 x 2048
- Supports two alpha blending channels for main display
- Supports four overlay layers in each channel, and has an independent scaler
- Supports potter-duff compatible blending operation
- Support LBC buffer decoder for YUV420
- Supports dither output to TCON
- Supports input format Semi-planar YUV422/YUV420/YUV411 and Planar YUV422/YUV420/YUV411, ARGB8888/XRGB8888/RGB888/ARGB4444/ARGB1555/RGB565/palette
- Supports Awonder1.1 Lite for excellent display experience
 - Adaptive luminance de-noising for compression noise or mosquito noise for yuv420/422 input
 - Adaptive horizontal detail/edge enhancement
 - Hue gain, Saturation gain, and Value gain controlled
 - Fully programmable color matrix
 - Dynamic gamma
 - 17x17x17 programmable LUT for 3D color management
 - global dynamic contrast enhancement
 - Color temperature tuning/Auto white balance
- Supports write back only for verification
- Support RCQ to configure registers
- Support keystone correction

2.3.2 De-interlacer (DI)

- Supports YUV420 (Planar/NV12/NV21) and YUV422 (Planar/NV16/NV61) data format
- Supports video resolution from 32 x 32 to 2048 x 1280 pixel

- Supports Inter-field interpolation/motion adaptive de-interlace method
- Performance: module clock 600 MHz for 1080p@60Hz YUV420

2.3.3 Graphic 2D (G2D)

- Supports mixer layer size up to 2048 x 2048 pixels, and rotation size up to 4096x4096 pixels
- Supports pre-multiply alpha image data
- Supports color key
- Supports two pipes Porter-Duff alpha blending
- Supports multiple video formats 4:2:0, 4:2:2, 4:1:1 and multiple pixel formats (8/16/24/32 bits graphics layer)
- Supports memory scan order option
- Supports any format convert function
- Supports 1/16× to 32× resize ratio
- Supports 32-phase 8-tap horizontal anti-alias filter and 32-phase 4-tap vertical anti-alias filter
- Supports window clip
- Supports FillRectangle, BitBlit, StretchBlit and MaskBlit
- Supports horizontal and vertical flip, clockwise 0/90/180/270 degree rotate for normal buffer

2.4 Video Engine

2.4.1 Video Decoder

2.4.1.1 Video Decoding

- H.265/HEVC Main Profile@Level4.1, up to 1920 x 1080@60fps
- H.264/AVC, BP/MP/HP@Level4.2, up to 1920 x 1080@60fps
- H.263 BP, up to 1920 x 1080@60fps
- MPEG-4 SP@L0-3, ASP@L0-5, up to 1920 x 1080@60fps
- MPEG-2 SP@ML, MP@HL, up to 1920 x 1080@60fps
- MPEG-1, up to 1920 x 1080@60fps
- VC-1 SP@ML, MP@HL, AP@L0-4, up to 1920 x 1080@60fps

2.4.1.2 Image Decoding

- JPEG decoding
 - Up to 1920 x 1080@60fps
 - Maximum decoding resolution: 1920x1088

2.4.2 Video Encoder

- JPEG/MJPEG up to 1920x1080@60fps
- Maximum resolution is 8192x8192
- Supports input picture scaling. The scaling ratio for width and height is 0.25 to 8

2.5 Video Output Interfaces

2.5.1 LCD

- One panel interface
 - RGB interface with DE/SYNC mode, up to 1920 x 1080@60fps
 - Serial/dummy RGB interface, up to 800 x 480@60fps
 - Dither function for RGB888, RGB666 and RGB565
 - Support BT.656 interface for NTSC and PAL
 - i8080 interface, up to 800x480@60fps
 - Dual-link LVDS interface
 - Up to 1920x1080@60fps for dual-link
 - Up to 1366x768@60fps for single-link

2.5.2 MIPI DSI

- Compliant with MIPI DSI specification v1.01 and MIPI D-PHY specification v1.0
- Supports one 4-lane MIPI DSI display, up to 1920 x 1200@60fps (reduced blanking)
- Up to 1.0 Gbit/s per lane

2.6 System Peripherals

2.6.1 Clock Controller Unit (CCU)

- Supports clock configuration and clock generation for corresponding modules
- Supports software-controlled clock gating and software-controlled reset for corresponding modules

2.6.2 Power Reset Clock Management (PRCM)

- Module clock configuration
- Bus gating, bus reset, and clock configuration
- RAM configuration control

2.6.3 RTC

- One on-chip RC oscillator

- Supports one external 24 MHz DCXO
- Provides a 16-bit counter for counting day, 5-bit counter for counting hour, 6-bit counter for counting minute, 6-bit counter for counting second
- Timer frequency is 1 kHz
- Configurable initial value by software anytime
- Supports timing alarm, and generates interrupt and wakeup the external devices
- 8 general purpose registers for storing power-off information in RTC domain

2.6.4 Thermal Sensor Controller (THS)

- One thermal sensor
- Averaging filter for thermal sensor reading
- Supports over-temperature protection interrupt and over-temperature alarm interrupt
- Support $\pm 3^{\circ}\text{C}$ error limit from 60°C to 125°C , and $\pm 5^{\circ}\text{C}$ from -40°C to 60°C

2.6.5 LDO Power

- Integrated 1 LDO(LDOA)
- LDOA: 1.8 V power output
- LDOA for IO and analog module
- Input voltage is 2.8 V to 3.6 V

2.6.6 Timer

- Supports Timer0 and Timer1
- Timer0 supports the following features:
 - The timer module implements the timing and counting functions, which includes timer0, timer1, watchdog, and audio video synchronization (AVS)
 - The timer0/timer1 is a 32-bit down counter. The timer0 and timer1 are completely consistent
 - The watchdog is used to transmit a reset signal to reset the entire system when an exception occurs in the system
 - The AVS is used to synchronize the audio and video. The AVS sub-block includes AVS0 and AVS1, which are completely consistent
- Timer1 contains timer0-3. The timer0/timer1/timer2/timer3 is a 32-bit down counter. They are completely consistent.

2.6.7 High Speed Timer (HSTimer)

- The HSTimer module consists of HSTimer0 and HSTimer1. HSTimer0 and HSTimer1 are down counters that implement timing and counting functions. They are completely consistent.
- Configurable 56-bit down timer

- Supports 5 prescale factors
- The clock source is synchronized with AHB0 clock, much more accurate than other timers
- Supports 2 working modes: periodic mode and single counting mode
- Generates an interrupt when the count is decreased to 0

2.7 Audio

2.7.1 Audio Codec

- One differential microphone input: MICIN1P/N
- One mono FMIN input: FMINL
- One stereo headphone output: HPOUTL and HPOUTR
- One audio ADC
 - 16-bit and 20-bit sample resolution
 - 8 kHz to 48 kHz ADC sample rate
 - 95 ± 3 dB SNR@A-weight, -80 ± 3 dB THD+N
- Two audio DACs
 - 16-bit and 20-bit sample resolution
 - 8 kHz to 192 kHz DAC sample rate
 - 100 ± 2 dB SNR@A-weight, -85 ± 3 dB THD+N
- Stereo headphone driver
 - 95 ± 3 dB SNR@A-weight
 - Output Level $0.54 V_{rms}@10 k\Omega/THD+N -77 \pm 3$ dB, $0.37 V_{rms}@16 \Omega/THD+N -40$ dB
- Supports Dynamic Range Controller adjusting the DAC playback and ADC recording
- One 128x20-bits FIFO for DAC data transmit, one 128x20-bits FIFO for ADC data receive
- Programmable FIFO thresholds
- Supports interrupts and DMA

2.7.2 I2S/PCM

- One I2S/PCM external interface (I2S2) for connecting external power amplifier and MIC ADC
- Compliant with standard Philips Inter-IC sound (I2S) bus specification
 - Left-justified, Right-justified, PCM mode, and TDM format
 - Programmable PCM frame width: 1 BCLK width (short frame) and 2 BCLKs width (long frame)
- FIFOs for transmitting and receiving data
 - Programmable FIFO thresholds
 - 128 depth x 32-bit width TXFIFO and 64 depth x 32-bit width RXFIFO
- Supports multiple function clocks
 - Clock up to 24.576 MHz Data Output of I2S/PCM in Master mode (Only if the IO PAD and Peripheral I2S/PCM satisfy Timing Parameters)

- Clock up to 12.288 MHz Data Input of I2S/PCM in Master mode
- Supports TX/RX DMA slave interface
- Supports multiple application scenarios
 - Up to 16 channels ($f_s = 48 \text{ kHz}$) which has adjustable width from 8-bit to 32-bit
 - Sample rate from 8 kHz to 384 kHz (sample rate * channel * slot width = 24.576 MHz)
 - 8-bit u-law and 8-bit A-law companded sample
- Supports master/slave mode

2.7.3 DMIC

- Supports maximum 8 digital PDM microphones
- Supports sample rate from 8 kHz to 48 kHz

2.7.4 One Wire Audio (OWA)

- One OWA TX and One OWA RX, compliant with S/PDIF interface
- Compatible with IEC-60958 and IEC-61937
 - IEC-60958 supports data formats: 16 bits, 20 bits, and 24 bits
- Transmit and receive data FIFOs
 - Programmable FIFO thresholds
 - One 128x24bits TXFIFO and one 64x24bits RXFIFO for audio data transfer
- Supports TX/RX DMA Slave interface
- Supports Multiple function clock
- Separate OWA TX and RX clock
 - OWA TX function clock includes a series of 24.576MHz and 22.579MHz frequency
 - OWA RX function clock includes a series of 24.576*8MHz frequency RX function clock 24.576*8MHz support CDR of sample rate from 8KHz to 192KHz
- Supports hardware parity On TX/RX
 - Hardware parity generation on the transmitter
 - Hardware parity checking on the receiver
- Supports channel status capture on the receiver
- Supports channel sample rate capture on the receiver
- Supports insertion detection for the receiver
- Support channel status insertion for the transmitter

2.8 Peripheral Interfaces

2.8.1 USB2.0 DRD

- One USB2.0 DRD (USB0), with integrated USB 2.0 analog PHY
- Complies with USB2.0 Specification
- Static host and device mode

- USB host that supports the following:
 - Compatible with Enhanced Host Controller Interface (EHCI) specification, version 1.0
 - Compatible with Open Host Controller Interface (OHCI) specification, version 1.0a
 - High-Speed (HS, 480 Mbit/s), Full-Speed (FS, 12 Mbit/s), and Low-Speed (LS, 1.5 Mbit/s)
 - Supports only 1 USB Root Port shared between EHCI and OHCI
- USB device that supports the following:
 - High-Speed (HS, 480 Mbit/s), Full-Speed (FS, 12 Mbit/s)
 - Up to 8KB+64Bytes FIFO for EPs (including EP0)
- Supports an internal DMA controller for data transfer with memory
- Device and Host controller share a 4KB SRAM and a physical PHY

2.8.2 USB2.0 Host

- One USB 2.0 Host (USB1), with integrated USB 2.0 analog PHY
- Compatible with Enhanced Host Controller Interface (EHCI) specification, version 1.0
- Compatible with Open Host Controller Interface (OHCI) specification, version 1.0a
- Supports High-Speed (HS, 480 Mbit/s), Full-Speed (FS, 12 Mbit/s) and Low-Speed (LS, 1.5 Mbit/s) Device
- An internal DMA Controller for data transfer with memory
- Supports only 1 USB Root Port shared between EHCI and OHCI

2.8.3 UART

- Up to 6 UART controllers (UART0, UART1, UART2, UART3, UART4, UART5)
- Compatible with industry-standard 16450/16550 UARTs
- 5-8 data bits, 1/1.5/2 stop bits, programmable parity (even, odd, or no parity)
- The working reference clock is from the APB bus clock
 - Speed up to 1.5 Mbit/s with 24 MHz APB clock
- Two separate FIFOs: one is RX FIFO, and the other is TX FIFO
 - 64 bytes RXFIFO and 64 bytes TXFIFO for UART0
 - 256 bytes RXFIFO and 256 bytes TXFIFO for UART1, UART2, UART3, UART4, UART5
- Supports 9-bit/RS-485 format and RS-485 full duplex mode
- Supports Software/hardware flow control
- Supports interrupts and DMA mode
- Supports auto-flow by using CTS & RTS for UART2, UART3

2.8.4 PWM

- Up to 8 PWM channels
 - Supports PWM continuous mode output
 - Supports PWM pulse mode output, and the pulse number is configurable
 - Output frequency range:

- 0 to 24 MHz (when the clock source is DCXO)
- 0 to 100 MHz (when the clock source is APB1 clock)
- Various duty-cycle: 0% -100%
- Minimum resolution: 1/65536
- Maximum 4 complementary pairs output
 - PWM01 pair (PWM-0 + PWM-1), PWM23 pair (PWM-2 + PWM-3), PWM45 pair (PWM-4 + PWM-5), PWM67 pair (PWM-6 + PWM-7)
 - Supports dead-zone generator, and the dead-zone time is configurable
- Maximum 4 group of PWM channel output for controlling stepping motors
 - Supports any plural channels to form a group, and output the same duty-cycle pulse
 - In group mode, the relative phase of the output waveform for each channel is configurable
- Maximum 8 channels capture input
 - Supports rising edge detection and falling edge detection for input waveform pulse
 - Supports pulse-width measurement for input waveform pulse

2.8.5 SPI and SPI_DBI

- Up to 2 SPI controllers
 - SPI0, supporting SPI mode
 - SPI1, supporting SPI mode and display bus interface (DBI) mode

SPI mode

- Multiple SPI modes:
 - Master mode and slave mode for standard SPI
 - Master mode for Dual-Output/Dual-Input SPI and Dual I/O SPI
 - Master mode for Quad-Output/Quad-Input SPI
 - Master mode for 3-wire SPI, with programmable serial data frame length of 1 bit to 32 bits
- Supports mode0, mode1, mode2, and mode3
- TX/RX DMA Slave interface
- Transmit data FIFO with 8-bit wide and 64-entry
- Receive data FIFO with 8-bit wide and 64-entry
- Transmit data buffer with 8-bit wide and 4-entry
- Receive data buffer with 8-bit wide and 128-entry
- Supports control signal configuration
 - One chip select
 - Polarity and phase of the Chip Select (SPI_CS) and SPI Clock (SPI_CLK) are configurable

DBI mode

- DBI Type C 3 Line/4 Line Interface Mode

- 2 Data Lane Interface Mode
- RGB111/444/565/666/888 video format
- Maximum resolution of RGB666 240 x 320@30Hz with single data lane
- Maximum resolution of RGB888 240 x 320@60Hz or 320 x 480@30Hz with dual data lane
- Tearing effect
- Software flexible control video frame rate

2.8.6 Two Wire Interface (TWI)

- Up to 4 TWI controllers (TWI0, TWI1, TWI2, TWI3)
- Compliant with I2C bus standard
- master mode and slave mode
- 7-bit and 10-bit device addressing modes
- Standard mode (up to 100 Kbit/s) and fast mode (up to 400 Kbit/s)
- Supports multi-master devices

2.8.7 General Purpose ADC (GPADC)

- One 1-ch ADC
- 12-bit sampling resolution
- Maximum sampling frequency up to 1 MHz
- Supports three operation modes: single conversion mode, continuous conversion mode, burst conversion mode
- Analog input range: 0 to 1.8 V

2.8.8 GPIO_ADC

- 2-ch ADC
- 12-bit SAR type A/D converter
- 32x12 FIFO for storing A/D conversion result
- Supports DMA slave interface
- Maximum sampling rate of 750 kHz
- Analog input range: 0 to 1.8 V

2.8.9 LED Controller (LEDC)

- LEDC is used to control the external intelligent control LED lamp
- Configurable LED output high/low level width and reset time
- LEDC data supports DMA configuration mode and CPU configuration mode
- Maximum 1024 LEDs serial connect
- Configurable interval time between data packets and frame data
- Configurable RGB display mode
- Configurable default level of non-data output

2.8.10 Consumer Infrared Transmitter (IR_TX)

- One IR_TX interface
- Supports arbitrary wave generator
- Configurable carrier frequency
- Supports handshake mode and waiting mode of DMA
- 128 bytes FIFO for data buffer

2.8.11 Consumer Infrared Receiver (IR_RX)

- One IR_RX interface
- NEC format infra data
- RLC encoding
- 64x8 bits FIFO for data buffer
- Sample clock up to 1 MHz

2.9 Security

2.9.1 Crypto Engine (CE)

- Supports Symmetrical algorithm for encryption and decryption: AES, DES, 3DES
 - Supports ECB, CBC, CTS, CTR, CFB, OFB mode for AES
 - Supports 128/192/256-bit key for AES
 - Supports ECB, CBC, CTR mode for DES/3DES
- Supports Hash algorithm for tamper proofing: MD5, SHA, HMAC
 - Supports SHA1, SHA224, SHA256, SHA384, SHA512 for SHA
 - Supports HMAC-SHA1, HMAC-SHA256 for HMAC
 - Supports multi-package mode for MD5/SHA1/SHA224/SHA256/SHA384/SHA512
- Supports Asymmetrical algorithm for signature verification: RSA
 - RSA supports 512/1024/2048-bit width
- Supports 160-bit hardware PRNG with 175-bit seed
- Supports 256-bit hardware TRNG
- Internal DMA controller for data transfer with memory

2.9.2 Security ID (SID)

- 2048-bit eFuse
- Backup eFuse information by using SID_SRAM
- One-time programming
- Selecting double-bit check by parameter definition
- Data scrambling
- Reading and writing protection

2.10 Package

QFP 128 pins, 14 mm x 14 mm body size, 1.60 mm height (maximum)

Draft Version

The Allwinner logo, consisting of a large, light gray 'A' inside a circle, with the word 'ALLWINNER' in bold, light gray capital letters to its right.

3 Pin Description

3.1 Pin Characteristics

This section lists the characteristics of the device pins from the following seven aspects.

[1] **Pin#:** Package pin numbers associated with each signal.

[2] **Pin Name:** The name of the package pin.

NC means these pins are not connected.

[3] **Type:** Denotes the signal direction

I (Input),

O (Output),

I/O (Input/Output),

OD (Open-Drain),

A (Analog),

AI (Analog Input),

AO (Analog Output),

P (Power),

G (Ground)

N/A (Not Applicable)

[4] **Ball Reset State:** The state of the terminal at reset.

PU: Pull Up

PD: Pull Down

Z: High Impedance

N/A: Not Applicable

[5] **Pull Up/Down:** Denotes the presence of an internal pull-up or pull-down resistor. Pull-up and pull-down resistors can be enabled or disabled via software.

PU: Internal pullup

PD: Internal pulldown

PU/PD: Internal pullup and pulldown

N/A: Not Applicable

[6] **Default Buffer Strength:** Defines the default drive strength of the associated output buffer. The maximum drive strength of each GPIO is 6 mA.

N/A means Not Applicable.

[7] I/O Power Supply: The voltage supplies for the IO buffers of the terminal.

N/A means Not Applicable.

3.1.1 SDRAM

Table 3-1 SDRAM Pin Characteristics

Ball# ^[1]	Pin Name ^[2]	Type ^[3]	Ball Reset State ^[4]	Pull Up/Down ^[5]	Default Buffer Strength ^[6]	I/O Power Supply ^[7]
68	SA0	O	N/A	N/A	N/A	VCC-DRAM
70	SA1	O	N/A	N/A	N/A	VCC-DRAM
75	SA2	O	N/A	N/A	N/A	VCC-DRAM
69	SA3	O	N/A	N/A	N/A	VCC-DRAM
80	SA4	O	N/A	N/A	N/A	VCC-DRAM
78	SA5	O	N/A	N/A	N/A	VCC-DRAM
67	SA6	O	N/A	N/A	N/A	VCC-DRAM
85	SA7	O	N/A	N/A	N/A	VCC-DRAM
64	SA8	O	N/A	N/A	N/A	VCC-DRAM
65	SA9	O	N/A	N/A	N/A	VCC-DRAM
72	SA10	O	N/A	N/A	N/A	VCC-DRAM
61	SA11	O	N/A	N/A	N/A	VCC-DRAM
62	SA12	O	N/A	N/A	N/A	VCC-DRAM
84	SA13	O	N/A	N/A	N/A	VCC-DRAM
76	SBA0	O	N/A	N/A	N/A	VCC-DRAM
83	SBA1	O	N/A	N/A	N/A	VCC-DRAM
82	SBA2	O	N/A	N/A	N/A	VCC-DRAM
71	SCAS	O	N/A	N/A	N/A	VCC-DRAM
63	SCKE0	O	N/A	N/A	N/A	VCC-DRAM
73	SCKN	O	N/A	N/A	N/A	VCC-DRAM
74	SCKP	O	N/A	N/A	N/A	VCC-DRAM
86	SCS0	O	N/A	N/A	N/A	VCC-DRAM
44	SDQ0	I/O	N/A	N/A	N/A	VCC-DRAM
36	SDQ1	I/O	N/A	N/A	N/A	VCC-DRAM
35	SDQ2	I/O	N/A	N/A	N/A	VCC-DRAM

Ball# ^[1]	Pin Name ^[2]	Type ^[3]	Ball Reset State ^[4]	Pull Up/Down ^[5]	Default Buffer Strength ^[6]	I/O Power Supply ^[7]
37	SDQ3	I/O	N/A	N/A	N/A	VCC-DRAM
42	SDQ4	I/O	N/A	N/A	N/A	VCC-DRAM
43	SDQ5	I/O	N/A	N/A	N/A	VCC-DRAM
38	SDQ6	I/O	N/A	N/A	N/A	VCC-DRAM
45	SDQ7	I/O	N/A	N/A	N/A	VCC-DRAM
56	SDQ8	I/O	N/A	N/A	N/A	VCC-DRAM
54	SDQ9	I/O	N/A	N/A	N/A	VCC-DRAM
48	SDQ10	I/O	N/A	N/A	N/A	VCC-DRAM
47	SDQ11	I/O	N/A	N/A	N/A	VCC-DRAM
52	SDQ12	I/O	N/A	N/A	N/A	VCC-DRAM
51	SDQ13	I/O	N/A	N/A	N/A	VCC-DRAM
55	SDQ14	I/O	N/A	N/A	N/A	VCC-DRAM
57	SDQ15	I/O	N/A	N/A	N/A	VCC-DRAM
41	SDQM0	I/O	N/A	N/A	N/A	VCC-DRAM
53	SDQM1	I/O	N/A	N/A	N/A	VCC-DRAM
40	SDQS0N	I/O	N/A	N/A	N/A	VCC-DRAM
39	SDQS0P	I/O	N/A	N/A	N/A	VCC-DRAM
50	SDQS1N	I/O	N/A	N/A	N/A	VCC-DRAM
49	SDQS1P	I/O	N/A	N/A	N/A	VCC-DRAM
87	SODT0	I/O	N/A	N/A	N/A	VCC-DRAM
79	SRAS	O	N/A	N/A	N/A	VCC-DRAM
81	SRST	O	N/A	N/A	N/A	VCC-DRAM
66	SWE	O	N/A	N/A	N/A	VCC-DRAM
46	VCC-DRAM0	P	N/A	N/A	N/A	N/A
58	VCC-DRAM1	P	N/A	N/A	N/A	N/A
77	VCC-DRAM2	P	N/A	N/A	N/A	N/A
60	VDD18-DRAM	P	N/A	N/A	N/A	N/A

3.1.2 System Control

Table 3-2 System Control Pin Characteristics

Ball# ^[1]	Pin Name ^[2]	Type ^[3]	Ball Reset State ^[4]	Pull Up/Down ^[5]	Default Buffer Strength ^[6]	I/O Power Supply ^[7]
109	RESET	I/O, OD	N/A	N/A	N/A	VCC-RTC-PLL-HPVCC

3.1.3 RTC&PLL

Table 3-3 RTC&PLL Pin Characteristics

Ball# ^[1]	Pin Name ^[2]	Type ^[3]	Ball Reset State ^[4]	Pull Up/Down ^[5]	Default Buffer Strength ^[6]	I/O Power Supply ^[7]
108	VCC-RTC-PLL-HPVCC	P	N/A	N/A	N/A	N/A

3.1.4 DCXO

Table 3-4 DCXO Pin Characteristics

Ball# ^[1]	Pin Name ^[2]	Type ^[3]	Ball Reset State ^[4]	Pull Up/Down ^[5]	Default Buffer Strength ^[6]	I/O Power Supply ^[7]
110	DXIN	AI	N/A	N/A	N/A	VCC-RTC-PLL-HPVCC
111	DXOUT	AO	N/A	N/A	N/A	VCC-RTC-PLL-HPVCC

3.1.5 GPIO Groups

3.1.5.1 Port A

Table 3-5 Port A Pin Characteristics

Ball# ^[1]	Pin Name ^[2]	Type ^[3]	Ball Reset State ^[4]	Pull Up/Down ^[5]	Default Buffer Strength ^[6]	I/O Power Supply ^[7]
96	PA0	I/O	Z	PU/PD	4 mA	AVCC
97	PA1	I/O	Z	PU/PD	4 mA	AVCC

3.1.5.2 Port B

Table 3-6 Port B Pin Characteristics

Ball# ^[1]	Pin Name ^[2]	Type ^[3]	Ball Reset State ^[4]	Pull Up/Down ^[5]	Default Buffer Strength ^[6]	I/O Power Supply ^[7]
27	PB1	I/O	Z	PU/PD	4 mA	VCC33-USB-LDOIN-IO

Ball# ^[1]	Pin Name ^[2]	Type ^[3]	Ball Reset State ^[4]	Pull Up/Down ^[5]	Default Buffer Strength ^[6]	I/O Power Supply ^[7]
26	PB2	I/O	Z	PU/PD	4 mA	VCC33-USB-LDOIN-IO
25	PB3	I/O	Z	PU/PD	4 mA	VCC33-USB-LDOIN-IO
23	PB4	I/O	Z	PU/PD	4 mA	VCC33-USB-LDOIN-IO
22	PB5	I/O	Z	PU/PD	4 mA	VCC33-USB-LDOIN-IO
21	PB6	I/O	Z	PU/PD	4 mA	VCC33-USB-LDOIN-IO
20	PB7	I/O	Z	PU/PD	4 mA	VCC33-USB-LDOIN-IO

3.1.5.3 Port C

Table 3-7 Port C Pin Characteristics

Ball# ^[1]	Pin Name ^[2]	Type ^[3]	Ball Reset State ^[4]	Pull Up/Down ^[5]	Default Buffer Strength ^[6]	I/O Power Supply ^[7]
94	PC0	I/O	Z	PU/PD	4 mA	VCC33-USB-LDOIN-IO
93	PC1	I/O	PU	PU/PD	4 mA	VCC33-USB-LDOIN-IO
92	PC2	I/O	PU	PU/PD	4 mA	VCC33-USB-LDOIN-IO
90	PC3	I/O	PU	PU/PD	4 mA	VCC33-USB-LDOIN-IO
91	PC4	I/O	Z	PU/PD	4 mA	VCC33-USB-LDOIN-IO
89	PC5	I/O	Z	PU/PD	4 mA	VCC33-USB-LDOIN-IO

3.1.5.4 Port D

Table 3-8 Port D Pin Characteristics

Ball# ^[1]	Pin Name ^[2]	Type ^[3]	Ball Reset State ^[4]	Pull Up/Down ^[5]	Default Buffer Strength ^[6]	I/O Power Supply ^[7]
5	PD0	I/O	Z	PU/PD	4 mA	VCC33-PD/VCC18-LVDS-EFUSE
6	PD1	I/O	Z	PU/PD	4 mA	VCC33-PD/VCC18-LVDS-EFUSE
7	PD2	I/O	Z	PU/PD	4 mA	VCC33-PD/VCC18-LVDS-EFUSE
8	PD3	I/O	Z	PU/PD	4 mA	VCC33-PD/VCC18-LVDS-EFUSE
9	PD4	I/O	Z	PU/PD	4 mA	VCC33-PD/VCC18-LVDS-EFUSE
10	PD5	I/O	Z	PU/PD	4 mA	VCC33-PD/VCC18-LVDS-EFUSE
13	PD6	I/O	Z	PU/PD	4 mA	VCC33-PD/VCC18-LVDS-EFUSE

Ball# ^[1]	Pin Name ^[2]	Type ^[3]	Ball Reset State ^[4]	Pull Up/Down ^[5]	Default Buffer Strength ^[6]	I/O Power Supply ^[7]
14	PD7	I/O	Z	PU/PD	4 mA	VCC33-PD/VCC18-LVDS-EFUSE
15	PD8	I/O	Z	PU/PD	4 mA	VCC33-PD/VCC18-LVDS-EFUSE
16	PD9	I/O	Z	PU/PD	4 mA	VCC33-PD/VCC18-LVDS-EFUSE
123	PD10	I/O	Z	PU/PD	4 mA	VCC33-PD/VCC18-LVDS-EFUSE
124	PD11	I/O	Z	PU/PD	4 mA	VCC33-PD/VCC18-LVDS-EFUSE
125	PD12	I/O	Z	PU/PD	4 mA	VCC33-PD/VCC18-LVDS-EFUSE
126	PD13	I/O	Z	PU/PD	4 mA	VCC33-PD/VCC18-LVDS-EFUSE
127	PD14	I/O	Z	PU/PD	4 mA	VCC33-PD/VCC18-LVDS-EFUSE
128	PD15	I/O	Z	PU/PD	4 mA	VCC33-PD/VCC18-LVDS-EFUSE
1	PD16	I/O	Z	PU/PD	4 mA	VCC33-PD/VCC18-LVDS-EFUSE
2	PD17	I/O	Z	PU/PD	4 mA	VCC33-PD/VCC18-LVDS-EFUSE
3	PD18	I/O	Z	PU/PD	4 mA	VCC33-PD/VCC18-LVDS-EFUSE
4	PD19	I/O	Z	PU/PD	4 mA	VCC33-PD/VCC18-LVDS-EFUSE
17	PD20	I/O	Z	PU/PD	4 mA	VCC33-PD
18	PD21	I/O	Z	PU/PD	4 mA	VCC33-PD
19	PD22	I/O	Z	PU/PD	4 mA	VCC33-PD
11	VCC33-PD	P	N/A	N/A	N/A	N/A
12	VCC18-LVDS-EFUSE	P	N/A	N/A	N/A	N/A

3.1.5.5 Port F

Table 3-9 Port F Pin Characteristics

Ball# ^[1]	Pin Name ^[2]	Type ^[3]	Ball Reset State ^[4]	Pull Up/Down ^[5]	Default Buffer Strength ^[6]	I/O Power Supply ^[7]
116	PF0	I/O	Z	PU/PD	4 mA	VCC33-PD/VCC18-LVDS-EFUSE
117	PF1	I/O	Z	PU/PD	4 mA	VCC33-PD/VCC18-LVDS-EFUSE
118	PF2	I/O	Z	PU/PD	4 mA	VCC33-PD/VCC18-LVDS-EFUSE
119	PF3	I/O	Z	PU/PD	4 mA	VCC33-PD/VCC18-LVDS-EFUSE
120	PF4	I/O	Z	PU/PD	4 mA	VCC33-PD/VCC18-LVDS-EFUSE
121	PF5	I/O	Z	PU/PD	4 mA	VCC33-PD/VCC18-LVDS-EFUSE

3.1.5.6 Port G

Table 3-10 Port G Pin Characteristics

Ball# ^[1]	Pin Name ^[2]	Type ^[3]	Ball Reset State ^[4]	Pull Up/Down ^[5]	Default Buffer Strength ^[6]	I/O Power Supply ^[7]
29	PG0	I/O	Z	PU/PD	4 mA	VCC33-USB-LDOIN-IO
30	PG1	I/O	Z	PU/PD	4 mA	VCC33-USB-LDOIN-IO
31	PG2	I/O	Z	PU/PD	4 mA	VCC33-USB-LDOIN-IO
32	PG3	I/O	Z	PU/PD	4 mA	VCC33-USB-LDOIN-IO
33	PG4	I/O	Z	PU/PD	4 mA	VCC33-USB-LDOIN-IO
34	PG5	I/O	Z	PU/PD	4 mA	VCC33-USB-LDOIN-IO

3.1.6 USB

Table 3-11 USB Pin Characteristics

Ball# ^[1]	Pin Name ^[2]	Type ^[3]	Ball Reset State ^[4]	Pull Up/Down ^[5]	Default Buffer Strength ^[6]	I/O Power Supply ^[7]
114	USB0-DM	A I/O	N/A	N/A	N/A	VCC33-USB-LDOIN-IO
115	USB0-DP	A I/O	N/A	N/A	N/A	VCC33-USB-LDOIN-IO
112	USB1-DM	A I/O	N/A	N/A	N/A	VCC33-USB-LDOIN-IO
113	USB1-DP	A I/O	N/A	N/A	N/A	VCC33-USB-LDOIN-IO

3.1.7 Audio Codec

Table 3-12 Audio Codec Pin Characteristics

Ball# ^[1]	Pin Name ^[2]	Type ^[3]	Ball Reset State ^[4]	Pull Up/Down ^[5]	Default Buffer Strength ^[6]	I/O Power Supply ^[7]
102	MICIN1P	AI	N/A	N/A	N/A	AVCC
103	MICIN1N	AI	N/A	N/A	N/A	AVCC
99	FMINL	AI	N/A	N/A	N/A	AVCC
106	HPOUTFB	A I/O	N/A	N/A	N/A	VCC-RTC-PLL-HPVCC
107	HPOUTL	AO	N/A	N/A	N/A	VCC-RTC-PLL-HPVCC
105	HPOUTR	AO	N/A	N/A	N/A	VCC-RTC-PLL-HPVCC
100	VRA1	A I/O	N/A	N/A	N/A	AVCC
104	AVCC	P	N/A	N/A	N/A	N/A

Ball# ^[1]	Pin Name ^[2]	Type ^[3]	Ball Reset State ^[4]	Pull Up/Down ^[5]	Default Buffer Strength ^[6]	I/O Power Supply ^[7]
101	AGND	G	N/A	N/A	N/A	N/A

3.1.8 GPADC

Table 3-13 GPADC Pin Characteristics

Ball# ^[1]	Pin Name ^[2]	Type ^[3]	Ball Reset State ^[4]	Pull Up/Down ^[5]	Default Buffer Strength ^[6]	I/O Power Supply ^[7]
98	GPADC0	AI	N/A	N/A	N/A	AVCC

3.1.9 Power

Table 3-14 Power Pin Characteristics

Ball# ^[1]	Pin Name ^[2]	Type ^[3]	Ball Reset State ^[4]	Pull Up/Down ^[5]	Default Buffer Strength ^[6]	I/O Power Supply ^[7]
28	VDD-SYS0	P	N/A	N/A	N/A	N/A
59	VDD-SYS1	P	N/A	N/A	N/A	N/A
88	VDD-SYS2	P	N/A	N/A	N/A	N/A
95	VDD-SYS3	P	N/A	N/A	N/A	N/A
122	VDD-SYS4	P	N/A	N/A	N/A	N/A
24	VCC33-USB-LDOIN-IO	P	N/A	N/A	N/A	N/A

3.2 GPIO Multiplex Function

The following tables provide a description of the GPIO multiplex function.



NOTE

For each GPIO, Function0 is input function; Function1 is output function; Function9 to Function13 are reserved.

3.2.1 Port A

Table 3-15 Port A Multiplex Function

Pin Name	IO Type	Function2	Function3	Function4	Function5	Function6	Function7	Function8	Function14
PA0	I/O	ADC0	PWM-1						PA-EINT0
PA1	I/O	ADC1	PWM-2						PA-EINT1

3.2.2 Port B

Table 3-16 Port B Multiplex Function

Pin Name	IO Type	Function2	Function3	Function4	Function5	Function6	Function7	Function8	Function14
PB1	I/O	LCD0-D0	I2S2-DOUT3		I2S2-DIN3			IR-RX	PB-EINT1
PB2	I/O	LCD0-D1	I2S2-DOUT2	TWI0-SDA	I2S2-DIN2		UART4-TX		PB-EINT2
PB3	I/O	LCD0-D8	I2S2-DOUT1	TWI0-SCK	I2S2-DIN0		UART4-RX		PB-EINT3
PB4	I/O	LCD0-D9	I2S2-DOUT0	TWI1-SCK	I2S2-DIN1		UART5-TX		PB-EINT4
PB5	I/O	LCD0-D16	I2S2-BCLK	TWI1-SDA	PWM-0		UART5-RX		PB-EINT5
PB6	I/O	LCD0-D17	I2S2-LRCK	TWI3-SCK	PWM-1		UART3-TX		PB-EINT6
PB7	I/O	PWM-4	I2S2-MCLK	TWI3-SDA	IR-RX		UART3-RX		PB-EINT7

3.2.3 Port C

Table 3-17 Port C Multiplex Function

Pin Name	IO Type	Function2	Function3	Function4	Function5	Function6	Function7	Function8	Function14
PC0	I/O	SPI0-CLK	SDC2-CLK						PC-EINT0
PC1	I/O	SPI0-CS0	SDC2-CMD						PC-EINT1
PC2	I/O	SPI0-MISO	SDC2-D2	BOOT-SEL0					PC-EINT2
PC3	I/O	SPI0-MOSI	SDC2-D0	BOOT-SEL1					PC-EINT3
PC4	I/O	SPI0-WP	SDC2-D1	UART3-TX	TWI3-SCK				PC-EINT4
PC5	I/O	SPI0-HOLD	SDC2-D3	UART3-RX	TWI3-SDA	TCON-FSYNC			PC-EINT5

3.2.4 Port D

Table 3-18 Port D Multiplex Function

Pin Name	IO Type	Function2	Function3	Function4	Function5	Function6	Function7	Function8	Function14
PD0	I/O	LCD0-D2	LVDS0-D0P	DSI-D0P	TWI0-SCK				PD-EINT0
PD1	I/O	LCD0-D3	LVDS0-D0N	DSI-D0N	UART2-TX				PD-EINT1
PD2	I/O	LCD0-D4	LVDS0-D1P	DSI-D1P	UART2-RX				PD-EINT2
PD3	I/O	LCD0-D5	LVDS0-D1N	DSI-D1N	UART2-RTS				PD-EINT3
PD4	I/O	LCD0-D6	LVDS0-D2P	DSI-CKP	UART2-CTS				PD-EINT4
PD5	I/O	LCD0-D7	LVDS0-D2N	DSI-CKN	UART5-TX				PD-EINT5
PD6	I/O	LCD0-D10	LVDS0-CKP	DSI-D2P	UART5-RX				PD-EINT6
PD7	I/O	LCD0-D11	LVDS0-CKN	DSI-D2N	UART4-TX				PD-EINT7
PD8	I/O	LCD0-D12	LVDS0-D3P	DSI-D3P	UART4-RX				PD-EINT8
PD9	I/O	LCD0-D13	LVDS0-D3N	DSI-D3N	PWM-6				PD-EINT9

Pin Name	IO Type	Function2	Function3	Function4	Function5	Function6	Function7	Function8	Function14
PD10	I/O	LCD0-D14	LVDS1-D0P	SPI1-CS0/DBI-CSX	UART3-TX				PD-EINT10
PD11	I/O	LCD0-D15	LVDS1-D0N	SPI1-CLK/DBI-SCLK	UART3-RX				PD-EINT11
PD12	I/O	LCD0-D18	LVDS1-D1P	SPI1-MOSI/DBI-SDO	TWI0-SDA				PD-EINT12
PD13	I/O	LCD0-D19	LVDS1-D1N	SPI1-MISO/DBI-SDI/DBI-TE/DBI-DCX	UART3-RTS				PD-EINT13
PD14	I/O	LCD0-D20	LVDS1-D2P	SPI1-HOLD/DBI-DCX/DBI-WRX	UART3-CTS				PD-EINT14
PD15	I/O	LCD0-D21	LVDS1-D2N	SPI1-WP/DBI-TE	IR-RX				PD-EINT15
PD16	I/O	LCD0-D22	LVDS1-CKP	DMIC-DATA3	PWM-0				PD-EINT16
PD17	I/O	LCD0-D23	LVDS1-CKN	DMIC-DATA2	PWM-1				PD-EINT17
PD18	I/O	LCD0-CLK	LVDS1-D3P	DMIC-DATA1	PWM-2				PD-EINT18
PD19	I/O	LCD0-DE	LVDS1-D3N	DMIC-DATA0	PWM-3				PD-EINT19
PD20	I/O	LCD0-HSYNC	TWI2-SCK	DMIC-CLK	PWM-4				PD-EINT20
PD21	I/O	LCD0-VSYNC	TWI2-SDA	UART1-TX	PWM-5				PD-EINT21
PD22	I/O	OWA-OUT	IR-RX	UART1-RX	PWM-7				PD-EINT22

3.2.5 Port F

Table 3-19 Port F Multiplex Function

Pin Name	IO Type	Function2	Function3	Function4	Function5	Function6	Function7	Function8	Function14
PF0	I/O	SDC0-D1	DJTAG-MS	RJTAG-MS			LCD0-D0		PF-EINT0
PF1	I/O	SDC0-D0	DJTAG-DI	RJTAG-DI			LCD0-D1		PF-EINT1
PF2	I/O	SDC0-CLK	UART0-TX	TWI0-SCK	LEDC	OWA-IN	LCD0-D8		PF-EINT2
PF3	I/O	SDC0-CMD	DJTAG-DO	RJTAG-DO		TWI1-SCK	LCD0-D9		PF-EINT3
PF4	I/O	SDC0-D3	UART0-RX	TWI0-SDA	PWM-6	IR-TX	LCD0-D16		PF-EINT4
PF5	I/O	SDC0-D2	DJTAG-CK	RJTAG-CK		TWI1-SDA	LCD0-D17		PF-EINT5

3.2.6 Port G

Table 3-20 Port G Multiplex Function

Pin Name	IO Type	Function2	Function3	Function4	Function5	Function6	Function7	Function8	Function14
PG0	I/O	SDC1-D1	UART3-TX		PWM-7	SDC1-D3	SDC1-D1		PG-EINT0
PG1	I/O	SDC1-D0	UART3-RX		PWM-6	SDC1-D1	SDC1-D3		PG-EINT1
PG2	I/O	SDC1-CLK	UART3-RTS		UART4-TX	SDC1-CLK	SDC1-CLK		PG-EINT2
PG3	I/O	SDC1-CMD	UART3-CTS		UART4-RX	SDC1-D0	SDC1-D2		PG-EINT3
PG4	I/O	SDC1-D3	UART5-TX		PWM-5	SDC1-CMD	SDC1-CMD		PG-EINT4
PG5	I/O	SDC1-D2	UART5-RX		PWM-4	SDC1-D2	SDC1-D0		PG-EINT5

3.3 Detailed Signal Description

The following tables show the detailed function description of every signal based on the different interfaces.

[1] **Signal Name:** The name of every signal.

[2] **Description:** The detailed function description of every signal.

[3] **Type:** Denotes the signal direction:

I (Input),

O (Output),

I/O (Input/Output),

OD (Open-Drain),

A (Analog),

AI (Analog Input),

AO (Analog Output),

A I/O (Analog Input/Output),

P (Power),

G (Ground)

3.3.1 SDRAM

Table 3-21 SDRAM Signal Description

Signal Name ^[1]	Description ^[2]	Type ^[3]
SA0	DRAM Address Signal 0	O
SA1	DRAM Address Signal 1	O
SA2	DRAM Address Signal 2	O
SA3	DRAM Address Signal 3	O
SA4	DRAM Address Signal 4	O
SA5	DRAM Address Signal 5	O
SA6	DRAM Address Signal 6	O
SA7	DRAM Address Signal 7	O
SA8	DRAM Address Signal 8	O
SA9	DRAM Address Signal 9	O
SA10	DRAM Address Signal 10	O
SA11	DRAM Address Signal 11	O

Signal Name ^[1]	Description ^[2]	Type ^[3]
SA12	DRAM Address Signal 12	O
SA13	DRAM Address Signal 13	O
SBA0	DRAM Bank Address Signal 0	O
SBA1	DRAM Bank Address Signal 1	O
SBA2	DRAM Bank Address Signal 2	O
SRAS	DRAM Row Address Strobe	O
SCAS	DRAM Column Address Strobe	O
SCKE0	DRAM Clock Enable Signal 0	O
SCKN	DRAM Differential Clock (Negative)	O
SCKP	DRAM Differential Clock (Positive)	O
SCS0	DRAM Chip Select Signal 0	O
SDQ0	DRAM Bidirectional Data Line 0	I/O
SDQ1	DRAM Bidirectional Data Line 1	I/O
SDQ2	DRAM Bidirectional Data Line 2	I/O
SDQ3	DRAM Bidirectional Data Line 3	I/O
SDQ4	DRAM Bidirectional Data Line 4	I/O
SDQ5	DRAM Bidirectional Data Line 5	I/O
SDQ6	DRAM Bidirectional Data Line 6	I/O
SDQ7	DRAM Bidirectional Data Line 7	I/O
SDQ8	DRAM Bidirectional Data Line 8	I/O
SDQ9	DRAM Bidirectional Data Line 9	I/O
SDQ10	DRAM Bidirectional Data Line 10	I/O
SDQ11	DRAM Bidirectional Data Line 11	I/O
SDQ12	DRAM Bidirectional Data Line 12	I/O
SDQ13	DRAM Bidirectional Data Line 13	I/O
SDQ14	DRAM Bidirectional Data Line 14	I/O
SDQ15	DRAM Bidirectional Data Line 15	I/O
SDQM0	DRAM Data Mask Signal	I/O
SDQM1	DRAM Data Mask Signal	I/O
SDQS0N	DRAM Bidirectional Data Strobe 0 (Active Low)	I/O

Signal Name ^[1]	Description ^[2]	Type ^[3]
SDQS0P	DRAM Bidirectional Data Strobe 0 (Active-High)	I/O
SDQS1N	DRAM Bidirectional Data Strobe 1 (Active Low)	I/O
SDQS1P	DRAM Bidirectional Data Strobe 1 (Active-High)	I/O
SODT0	DRAM On-Die Termination Output Signal 0	O
SRST	DRAM Reset Signal	O
SWE	DRAM Write Enable	O
VCC-DRAM	DRAM IO Power Supply	P
VDD18-DRAM	SDRAM Controller Power Supply	P

3.3.2 System Control

Table 3-22 System Control Signal Description

Signal Name ^[1]	Description ^[2]	Type ^[3]
RESET	SoC Reset Signal (Active Low)	I/O, OD
BOOT-SEL[1:0]	Boot Media Select	I

3.3.3 RTC&PLL

Table 3-23 RTC&PLL Signal Description

Signal Name ^[1]	Description ^[2]	Type ^[3]
VCC-RTC-PLL-HPVCC	PLL/RTC/DCXO/LDO-OUT/Headphone Power Supply	P

3.3.4 DCXO

Table 3-24 DCXO Signal Description

Signal Name ^[1]	Description ^[2]	Type ^[3]
DXIN	Digital Compensated Crystal Oscillator Input	AI
DXOUT	Digital Compensated Crystal Oscillator Output	AO

3.3.5 SD Card/SDIO/eMMC

Table 3-25 SD Card/SDIO/eMMC Signal Description

Signal Name ^[1]	Description ^[2]	Type ^[3]
SDC0-CMD	SD Card Command Output/Response Input	I/O, OD
SDC0-CLK	SD Card Clock Output	O

Signal Name ^[1]	Description ^[2]	Type ^[3]
SDC0-D0	SD Card Data Input/ Output 0	I/O
SDC0-D1	SD Card Data Input/ Output 1	I/O
SDC0-D2	SD Card Data Input/ Output 2	I/O
SDC0-D3	SD Card Data Input/ Output 3	I/O
SDC1-CMD	SDIO WIFI Command Output/Response Input	I/O, OD
SDC1-CLK	SDIO WIFI Clock Output	O
SDC1-D0	SDIO WIFI Data Input/ Output 0	I/O
SDC1-D1	SDIO WIFI Data Input/ Output 1	I/O
SDC1-D2	SDIO WIFI Data Input/ Output 2	I/O
SDC1-D3	SDIO WIFI Data Input/ Output 3	I/O
SDC2-CMD	eMMC Command Output/Response Input	I/O, OD
SDC2-CLK	eMMC Clock Output	O
SDC2-D0	eMMC Data Input/ Output 0	I/O
SDC2-D1	eMMC Data Input/ Output 1	I/O
SDC2-D2	eMMC Data Input/ Output 2	I/O
SDC2-D3	eMMC Data Input/ Output 3	I/O

3.3.6 USB

Table 3-26 USB Signal Description

Signal Name ^[1]	Description ^[2]	Type ^[3]
USB0-DM	USB0 Differential Data (Negative)	A I/O
USB0-DP	USB0 Differential Data (Positive)	A I/O
USB1-DM	USB1 Differential Data (Negative)	A I/O
USB1-DP	USB1 Differential Data (Positive)	A I/O

3.3.7 I2S/PCM

Table 3-27 I2S/PCM Signal Description

Signal Name ^[1]	Description ^[2]	Type ^[3]
I2S2-MCLK	I2S2 Master Clock	O
I2S2-LRCK	I2S2/PCM2 Sample Rate Clock/Sync	I/O
I2S2-BCLK	I2S2/PCM2 Bit Rate Clock	I/O

Signal Name ^[1]	Description ^[2]	Type ^[3]
I2S2-DIN0	I2S2/PCM2 Serial Data Input 0	I
I2S2-DIN1	I2S2/PCM2 Serial Data Input 1	I
I2S2-DIN2	I2S2/PCM2 Serial Data Input 2	I
I2S2-DIN3	I2S2/PCM2 Serial Data Input 3	I
I2S2-DOU0	I2S2/PCM2 Serial Data Output 0	O
I2S2-DOU1	I2S2/PCM2 Serial Data Output 1	O
I2S2-DOU2	I2S2/PCM2 Serial Data Output 2	O
I2S2-DOU3	I2S2/PCM2 Serial Data Output 3	O

3.3.8 Audio Codec

Table 3-28 Audio Codec Signal Description

Signal Name ^[1]	Description ^[2]	Type ^[3]
MICIN1P	Microphone Differential Positive Input 1	AI
MICIN1N	Microphone Differential Negative Input 1	AI
FMINL	FMIN Left Input	AI
HPOUTFB	Pseudo Differential Headphone Ground Reference	A I/O
HPOUTL	Headphone Left Output	AO
HPOUTR	Headphone Right Output	AO
AVCC	Power Supply for Analog Part	P
VRA1	Internal Reference Voltage	A I/O
AGND	Analog Ground	G

3.3.9 DMIC

Table 3-29 DMIC Signal Description

Signal Name ^[1]	Description ^[2]	Type ^[3]
DMIC-CLK	Digital Microphone Clock Output	O
DMIC-DATA0	Digital Microphone Data Input 0	I
DMIC-DATA1	Digital Microphone Data Input 1	I
DMIC-DATA2	Digital Microphone Data Input 2	I
DMIC-DATA3	Digital Microphone Data Input 3	I

3.3.10 OWA

Table 3-30 OWA Signal Description

Signal Name ^[1]	Description ^[2]	Type ^[3]
OWA-IN	One Wire Audio Input	I
OWA-OUT	One Wire Audio Output	O

3.3.11 GPADC

Table 3-31 GPADC Signal Description

Signal Name ^[1]	Description ^[2]	Type ^[3]
GPADC0	General Purpose ADC Input 0	AI

3.3.12 GPIO_ADC

Table 3-32 GPIO_ADC Signal Description

Signal Name ^[1]	Description ^[2]	Type ^[3]
ADC0	GPIO_ADC Input 0	AI
ADC1	GPIO_ADC Input 1	AI

3.3.13 LCD

Table 3-33 LCD Signal Description

Signal Name ^[1]	Description ^[2]	Type ^[3]
LCD0-CLK	LCD Clock	O
LCD0-VSYNC	LCD Vertical Synchronization	O
LCD0-HSYNC	LCD Horizontal Synchronization	O
TCON-FSYNC	Frame Synchronization Signal for TCON and Sensor	O
LCD0-DE	LCD Data Enable	O
LCD0-D0	LCD Data Input/Output 0	I/O
LCD0-D1	LCD Data Input/Output 1	I/O
LCD0-D2	LCD Data Input/Output 2	I/O
LCD0-D3	LCD Data Input/Output 3	I/O
LCD0-D4	LCD Data Input/Output 4	I/O
LCD0-D5	LCD Data Input/Output 5	I/O
LCD0-D6	LCD Data Input/Output 6	I/O

Signal Name ^[1]	Description ^[2]	Type ^[3]
LCD0-D7	LCD Data Input/Output 7	I/O
LCD0-D8	LCD Data Input/Output 8	I/O
LCD0-D9	LCD Data Input/Output 9	I/O
LCD0-D10	LCD Data Input/Output 10	I/O
LCD0-D11	LCD Data Input/Output 11	I/O
LCD0-D12	LCD Data Input/Output 12	I/O
LCD0-D13	LCD Data Input/Output 13	I/O
LCD0-D14	LCD Data Input/Output 14	I/O
LCD0-D15	LCD Data Input/Output 15	I/O
LCD0-D16	LCD Data Input/Output 16	I/O
LCD0-D17	LCD Data Input/Output 17	I/O
LCD0-D18	LCD Data Input/Output 18	I/O
LCD0-D19	LCD Data Input/Output 19	I/O
LCD0-D20	LCD Data Input/Output 20	I/O
LCD0-D21	LCD Data Input/Output 21	I/O
LCD0-D22	LCD Data Input/Output 22	I/O
LCD0-D23	LCD0 Data Input/Output 23	I/O

3.3.14 LVDS

Table 3-34 LVDS Signal Description

Signal Name ^[1]	Description ^[2]	Type ^[3]
LVDS0-CKP	LVDS0 Differential Clock (Positive)	AO
LVDS0-CKN	LVDS0 Differential Clock (Negative)	AO
LVDS0-D0P	LVDS0 Differential Data 0 (Positive)	AO
LVDS0-D0N	LVDS0 Differential Data 0 (Negative)	AO
LVDS0-D1P	LVDS0 Differential Data 1 (Positive)	AO
LVDS0-D1N	LVDS0 Differential Data 1 (Negative)	AO
LVDS0-D2P	LVDS0 Differential Data 2 (Positive)	AO
LVDS0-D2N	LVDS0 Differential Data 2 (Negative)	AO
LVDS0-D3P	LVDS0 Differential Data 3 (Positive)	AO
LVDS0-D3N	LVDS0 Differential Data 3 (Negative)	AO

Signal Name ^[1]	Description ^[2]	Type ^[3]
LVDS1-CKP	LVDS1 Differential Clock (Positive)	AO
LVDS1-CKN	LVDS1 Differential Clock (Negative)	AO
LVDS1-D0P	LVDS1 Differential Data 0 (Positive)	AO
LVDS1-D0N	LVDS1 Differential Data 0 (Negative)	AO
LVDS1-D1P	LVDS1 Differential Data 1 (Positive)	AO
LVDS1-D1N	LVDS1 Differential Data 1 (Negative)	AO
LVDS1-D2P	LVDS1 Differential Data 2 (Positive)	AO
LVDS1-D2N	LVDS1 Differential Data 2 (Negative)	AO
LVDS1-D3P	LVDS1 Differential Data 3 (Positive)	AO
LVDS1-D3N	LVDS1 Differential Data 3 (Negative)	AO
VCC18-LVDS-EFUSE	Power Supply for LVDS0/1, and eFuse	P

3.3.15 MIPI DSI

Table 3-35 MIPI DSI Signal Description

Signal Name ^[1]	Description ^[2]	Type ^[3]
DSI-CKP	DSI Differential Clock (Positive)	AO
DSI-CKN	DSI Differential Clock (Negative)	AO
DSI-D0P	DSI Differential Data Line 0 (Positive)	A I/O
DSI-D0N	DSI Differential Data Line 0 (Negative)	A I/O
DSI-D1P	DSI Differential Data Line 1 (Positive)	AO
DSI-D1N	DSI Differential Data Line 1 (Negative)	AO
DSI-D2P	DSI Differential Data Line 2 (Positive)	AO
DSI-D2N	DSI Differential Data Line 2 (Negative)	AO
DSI-D3P	DSI Differential Data Line 3 (Positive)	AO
DSI-D3N	DSI Differential Data Line 3 (Negative)	AO

3.3.16 SPI&SPI DBI

Table 3-36 SPI&SPI DBI Signal Description

Signal Name ^[1]	Description ^[2]	Type ^[3]
SPI0-CS0	SPI0 Chip Select 0 (Active Low)	I/O
SPI0-CLK	SPI0 Clock	I/O

Signal Name ^[1]	Description ^[2]	Type ^[3]
SPI0-MOSI	SPI0 Master Data Out, Slave Data In	I/O
SPI0-MISO	SPI0 Master Data In, Slave Data Out	I/O
SPI0-WP	SPI0 Write Protection (Active Low)/ Serial Data Input and Output for Quad Input or Quad Output	I/O
SPI0-HOLD	SPI0 Hold Signal/ Serial Data Input and Output for Quad Input or Quad Output	I/O
SPI1-CS0	SPI1 Chip Select 0 (Active Low)	I/O
SPI1-CLK	SPI1 Clock	I/O
SPI1-MOSI	SPI1 Master Data Out, Slave Data In	I/O
SPI1-MISO	SPI1 Master Data In, Slave Data Out	I/O
SPI1-WP	SPI1 Write Protection (Active Low)/ Serial Data Input and Output for Quad Input or Quad Output	I/O
SPI1-HOLD	SPI1 Hold Signal/ Serial Data Input and Output for Quad Input or Quad Output	I/O
DBI-CSX	Chip Select Signal (Active Low)	I/O
DBI-SCLK	Serial Clock Signal	I/O
DBI-SDO	Data Output Signal	I/O
DBI-SDI	Data Input Signal The data is sampled on the rising edge and the falling edge.	I/O
DBI-TE	Tearing Effect Input It is used to capture the external TE signal edge. The rising and falling edge is configurable.	I/O
DBI-DCX	DCX pin is the select output signal of data and command. DCX = 0: register command; DCX = 1: data or parameter.	I/O
DBI-WRX	When DBI operates in dual data lane format, the RGB666 format 2 can use WRX to transfer data	I/O

3.3.17 UART

Table 3-37 UART Signal Description

Signal Name ^[1]	Description ^[2]	Type ^[3]
UART0-RX	UART0 Data Receiver	I
UART0-TX	UART0 Data Transmitter	O

Signal Name ^[1]	Description ^[2]	Type ^[3]
UART1-RX	UART1 Data Receiver	I
UART1-TX	UART1 Data Transmitter	O
UART2-CTS	UART2 Clear to Send	I
UART2-RTS	UART2 Request to Send	O
UART2-RX	UART2 Data Receiver	I
UART2-TX	UART2 Data Transmitter	O
UART3-CTS	UART3 Clear to Send	I
UART3-RTS	UART3 Request to Send	O
UART3-RX	UART3 Data Receiver	I
UART3-TX	UART3 Data Transmitter	O
UART4-RX	UART4 Data Receiver	I
UART4-TX	UART4 Data Transmitter	O
UART5-RX	UART5 Data Receiver	I
UART5-TX	UART5 Data Transmitter	O

3.3.18 PWM

Table 3-38 PWM Signal Description

Signal Name ^[1]	Description ^[2]	Type ^[3]
PWM-0	PWM Wave Output /Capture Wave Input 0	I/O
PWM-1	PWM Wave Output /Capture Wave Input 1	I/O
PWM-2	PWM Wave Output /Capture Wave Input 2	I/O
PWM-3	PWM Wave Output /Capture Wave Input 3	I/O
PWM-4	PWM Wave Output /Capture Wave Input 4	I/O
PWM-5	PWM Wave Output /Capture Wave Input 5	I/O
PWM-6	PWM Wave Output /Capture Wave Input 6	I/O
PWM-7	PWM Wave Output /Capture Wave Input 7	I/O

3.3.19 TWI

Table 3-39 TWI Signal Description

Signal Name ^[1]	Description ^[2]	Type ^[3]
TWI0-SCK	TWI0 Serial Clock Signal	I/O

Signal Name ^[1]	Description ^[2]	Type ^[3]
TWI0-SDA	TWI0 Serial Data Signal	I/O
TWI1-SCK	TWI1 Serial Clock Signal	I/O
TWI1-SDA	TWI1 Serial Data Signal	I/O
TWI2-SCK	TWI2 Serial Clock Signal	I/O
TWI2-SDA	TWI2 Serial Data Signal	I/O
TWI3-SCK	TWI3 Serial Clock Signal	I/O
TWI3-SDA	TWI3 Serial Data Signal	I/O

3.3.20 IR RX

Table 3-40 IR RX Signal Description

Signal Name ^[1]	Description ^[2]	Type ^[3]
IR-RX	Consumer Infrared Receiver	I

3.3.21 IR TX

Table 3-41 IR TX Signal Description

Signal Name ^[1]	Description ^[2]	Type ^[3]
IR-TX	Consumer Infrared Transmitter	O

3.3.22 LEDC

Table 3-42 LEDC Signal Description

Signal Name ^[1]	Description ^[2]	Type ^[3]
LEDC	Intelligent Control LED Signal Output	O

3.3.23 JTAG

Table 3-43 JTAG Signal Description

Signal Name ^[1]	Description ^[2]	Type ^[3]
RJTAG-MS	RISC-V JTAG Mode Selection	I
RJTAG-CK	RISC-V JTAG Clock Signal	I
RJTAG-DI	RISC-V JTAG Data Input	I
RJTAG-DO	RISC-V JTAG Data Output	O
DJTAG-MS	DAP JTAG Mode Selection	I

Signal Name ^[1]	Description ^[2]	Type ^[3]
DJTAG-CK	DAP JTAG Clock Signal	I
DJTAG-DI	DAP JTAG Data Input	I
DJTAG-DO	DAP JTAG Data Output	O

3.3.24 Interrupt

Table 3-44 Interrupt Signal Description

Signal Name ^[1]	Description ^[2]	Type ^[3]
PA-EINT[1:0]	Port A Interrupt	I
PB-EINT [7:1]	Port B Interrupt	I
PC-EINT[5:0]	Port C Interrupt	I
PD-EINT[22:0]	Port D Interrupt	I
PF-EINT[5:0]	Port F Interrupt	I
PG-EINT[5:0]	Port G Interrupt	I

4 Electrical characteristics

4.1 Parameter Conditions

4.1.1 Minimum and Maximum Values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage, and frequencies by tests in production on 100% of the devices with ambient temperature at $T_a = 25\text{ }^{\circ}\text{C}$ and $T_a = T_a \text{ max}$.

Data based on characterization results, design simulation, and/or technology characteristics are indicated in the table footnotes and are not tested in production.

4.1.2 Typical Values

Unless otherwise specified, the typical data are based on $T_a = 25\text{ }^{\circ}\text{C}$. They are given only as design guidelines.

4.1.3 Temperature Definitions

- Ambient Temperature(T_a) the temperature of the surrounding environment.
- Junction Temperature(T_j) the hottest temperature of the silicon chip inside the package.
- Absolute Maximum Junction Temperature(T_{jmax}) the temperature beyond which damage occurs to the device. The device may not function or meet expected performance at this temperature.
- Recommended Operating Temperature(T_{ro}) the junction temperature at which the device operates continuously at the designated performance over the designed lifetime. The reliability of the device may be degraded if the device operates above this temperature. Some devices will not function electrically above this temperature.

4.2 Absolute Maximum Ratings

Absolute Maximum Ratings are those values beyond which damage to the device may occur. The following table specifies the absolute maximum ratings.



CAUTION

Stresses beyond those listed under Table 4-1 may affect reliability or cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under section 4.3 Recommended Operating Conditions is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

Table 4-1 Absolute Maximum Ratings

Supply Name	Description	Min ⁽¹⁾	Max ⁽¹⁾	Unit
AVCC	Audio Codec/PA/GPADC Power Supply	-0.3	2.16	V
VCC-RTC-PLL-HPVCC	PLL/RTC/DCXO/LDO-OUT/Headphone Power Supply	-0.3	2.16	V
VCC18-LVDS-EFUSE	LVDS/PF/eFuse Power Supply	-0.3	2.16	V
VCC33-USB-LDOIN-IO	PC/PG/USB/LDO-IN Power Supply	-0.3	3.96	V
VCC33-PD	Digital Port D Power	-0.3	3.96	V
VDD-SYS0 VDD-SYS1 VDD-SYS2 VDD-SYS3 VDD-SYS4	CPU/SYS 0.9V Power Supply	-0.3	1.05	V
VCC-DRAM0 VCC-DRAM1 VCC-DRAM2	DRAM Power Supply	-0.3	VDDQ+0.3	V
VDD18-DRAM	DRAM Power Supply	-0.3	2.16	V
V _{ESD} ⁽²⁾	Human Body Model (HBM) ⁽³⁾	-2000	2000	V
	Charged Device Model (CDM) ⁽⁴⁾	-250	250	V
I _{Latch-up}	Latch-up I-test performance current-pulse injection on each IO pin ⁽⁵⁾	Pass		
	Latch-up over-voltage performance voltage injection on each IO pin ⁽⁶⁾	Pass		

(1) The min/max voltages of power rails are guaranteed by design, not tested in production.

- (2) Electrostatic discharge (ESD) to measure device sensitivity/immunity to damage caused by electrostatic discharges into the devices.
- (3) Level listed above is the passing level per ESDA/JEDEC JS-001-2017.
- (4) Level listed above is the passing level per ESDA/JEDEC JS-002-2018.
- (5) Based on JESD78E; each device is tested with IO pin injection of ± 150 mA at room temperature.
- (6) Based on JESD78E; each device is tested with a stress voltage of $1.5 \times V_{ddmax}$ at room temperature.

4.3 Recommended Operating Conditions

The following table describes operating conditions of the device.



NOTE

Logic functions and parameter values are not assured out of the range specified in the recommended operating conditions.

Table 4-2 Recommended Operating Conditions

Supply Name	Description	Min	Typ	Max	Unit
AVCC	Audio Codec/PA/GPADC Power Supply	1.782	1.8	1.818	V
VCC-RTC-PLL-HPVCC	PLL/RTC/DCXO/LDO-OUT/Headphone Power Supply	1.764	1.8	1.836	V
VCC33-USB-LDOIN-IO	PB/PC/PG/USB/LDO-IN Power Supply	2.97	3.3	3.63	V
VCC33-PD	Digital Port D Power	2.97	3.3	3.63	V
VDD-SYS0 VDD-SYS1 VDD-SYS2 VDD-SYS3 VDD-SYS4 VDD-SYS5	CPU/SYS Power Supply	0.9	0.98	1.02	V
VCC-DRAM0	DDR3L Power Supply	1.283	1.35	1.45	V
VCC-DRAM1	DDR3 Power Supply	1.425	1.5	1.575	
VCC-DRAM2	DDR2 Power Supply	1.746	1.8	1.854	
VDD18-DRAM	DRAM 1.8V Power Supply	1.7	1.8	1.95	V

4.4 GPIO DC Electrical Characteristics

Table 4-3 summarizes the GPIO DC electrical characteristics of the device.

Table 4-3 GPIO DC Electrical Characteristics⁽¹⁾

(VCC: VCC33-PD/AVCC/VCC33-USB-LDOIN-IO/VCC18-LVDS-EFUSE)

Symbol	Parameter		Min	Typ	Max	Unit
V _{IH}	High-Level Input Voltage		0.7 * VCC	-	1.1 * VCC	V
V _{IL}	Low-Level Input Voltage		-0.3	-	0.25 * VCC	V
R _{PU}	Output Pull-up Resistance	PC1 to PC5, PF3	9	15	21	kΩ
		PG0, PG1, PG3, PG4, PG5	19.8	33	46.2	kΩ
		Other GPIOs	60	100	140	kΩ
R _{PD}	Output Pull-down Resistance	PC1 to PC5, PF3	9	15	21	kΩ
		PG0, PG1, PG3, PG4, PG5	19.8	33	46.2	kΩ
		Other GPIOs	60	100	140	kΩ
I _{IH}	High-Level Input Current		-	-	10	uA
I _{IL}	Low-Level Input Current		-	-	10	uA
V _{OH}	High-Level Output Voltage		VCC (b0.3	-	VCC	V
V _{OL}	Low-Level Output Voltage		0	-	0.2	V
I _{OZ}	Tri-State Output Leakage Current		-10	-	10	uA
C _{IN}	Input Capacitance		-	-	5	pF
C _{OUT}	Output Capacitance		-	-	5	pF

(1) Guaranteed by design.

4.5 SMHC Electrical Characteristics

The SMHC electrical parameters are related to different supply voltage.

Figure 4-1 SMHC Voltage Waveform

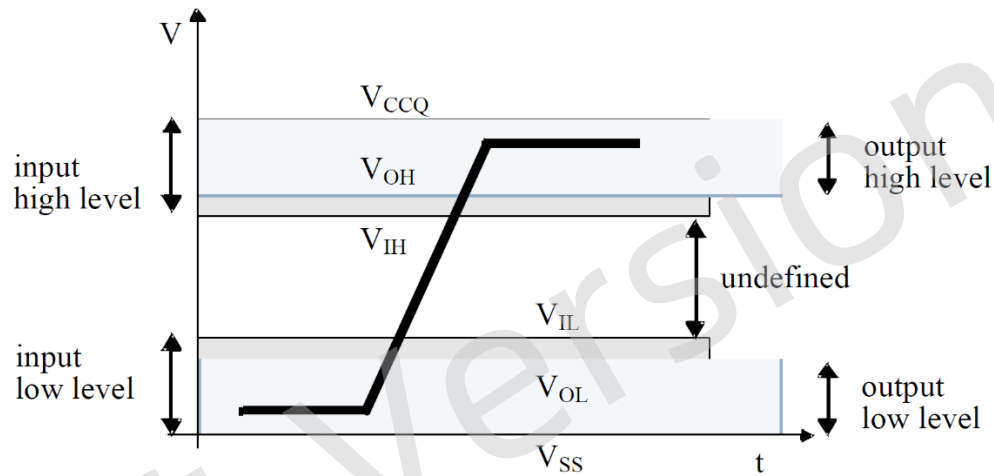


Table 4-4 shows 3.3 V SMHC electrical parameters.

Table 4-4 3.3 V SMHC Electrical Parameters

Symbol	Parameter	Min	Typ	Max	Unit
VDD	Power voltage	2.7	-	3.6	V
V _{CCQ}	I/O voltage	2.7	-	3.6	V
V _{OH}	Output high-level voltage	0.75 * V _{CCQ}	-	-	V
V _{OL}	Output low-level voltage	-	-	0.125 * V _{CCQ}	V
V _{IH}	Input high-level voltage	0.625 * V _{CCQ}	-	V _{CCQ} + 0.3	V
V _{IL}	Input low-level voltage	V _{SS} (b)0.3	-	0.25 * V _{CCQ}	V

Table 4-5 shows 1.8 V SMHC electrical parameters.

Table 4-5 1.8 V SMHC Electrical Parameters

Symbol	Parameter	Min	Typ	Max	Unit
VDD	Power voltage	2.7	-	3.6	V
V _{CCQ}	I/O voltage	1.7	-	1.95	V
V _{OH}	Output high-level voltage	V _{CCQ} (b)0.45	-	-	V
V _{OL}	Output low-level voltage	-	-	0.45	V
V _{IH}	Input high-level voltage	0.65 * V _{CCQ} ⁽¹⁾	-	V _{CCQ} + 0.3	V
V _{IL}	Input low-level voltage	V _{SS} (b)0.3	-	0.35 * V _{CCQ} ⁽²⁾	V

Symbol	Parameter	Min	Typ	Max	Unit
(1).0.7 * V _{CCQ} for MMC4.3 or lower.					
(2).0.3 * V _{CCQ} for MMC4.3 or lower.					

4.6 GPADC Electrical Characteristics

Table 4-6 lists the GPADC electrical characteristics.

Table 4-6 GPADC Electrical Characteristics

Parameter	Min	Typ	Max	Unit
ADC Resolution	-	12	-	bits
Full-scale Input Range	0	-	AVCC	V
Sampling Rate	-	-	1	MHz

4.7 GPIO_ADC Electrical Characteristics

Table 4-7 lists the GPIO_ADC electrical characteristics.

Table 4-7 GPIO_ADC Electrical Characteristics

Parameter	Min	Typ	Max	Unit
ADC Resolution	-	12	-	bits
Full-scale Input Range	0	-	AVCC	V
Sampling Rate	-	-	750	kHz

4.8 Audio Codec Electrical Characteristics

Test Conditions

AVCC = 1.8 V, Ta = 25 °C, 1 kHz sinusoid signal, DAC fs = 48 kHz, ADC fs = 16 kHz, input gain = 0 dB, 16-bit audio data unless otherwise stated.

Table 4-8 Audio Codec Typical Performance Parameters

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
DAC Path	DAC to HPOUTL or HPOUTR(R=100K)					
	Full-scale	0dBFS 1kHz	-	545	-	mVrms
	SNR(A-weighted)	0data	-	99	-	dB
	THD+N	0dBFS 1kHz	-	-85	-	dB
	Crosstalk	R_0dB_L_0data 1kHz L_0dB_R_0data 1kHz	-	-90	-	dB

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
	DAC to HPOUTL or HPOUTR(R=16Ω)					
	Full-scale	0dBFS 1kHz	-	500	-	mVrms
	SNR(A-weighted)	0data	-	99	-	dB
	THD+N(10mW)	1kHz	-	-85	-	dB
	Crosstalk	R_0dB_L_0data 1kHz L_0dB_R_0data 1kHz	-	-90	-	dB
	DAC to HPOUTL or HPOUTR(R=32Ω)					
	Full-scale	0dBFS 1kHz	-	530	-	mVrms
	SNR(A-weighted)	0data	-	99	-	dB
	THD+N(8.8mW)	0dBFS 1kHz	-	-85	-	dB
	Crosstalk	R_0dB_L_0data 1kHz L_0dB_R_0data 1kHz	-	-90	-	dB
ADC Path	MICIN via ADC					
	Output Level	MICP=3.3Vpp/2	-	920	-	mFFS
	SNR(A-weighted)	MICN=3.3Vpp/2	-	95	-	dB
	THD+N	1kHz, 0dB Gain	-	-90	-	dB
	Output Level	MICP=1.65Vpp/2	-	920	-	mFFS
	SNR(A-weighted)	MICN=1.65Vpp/2	-	90	-	dB
	THD+N	1kHz, 6dB Gain	-	-90	-	dB
	Output Level	MICP=0.828Vpp/2	-	920	-	mFFS
	SNR(A-weighted)	MICN=0.828Vpp/2	-	80	-	dB
	THD+N	1kHz, 12dB Gain	-	-90	-	dB
	Output Level	MICP=0.414Vpp/2	-	920	-	mFFS
	SNR(A-weighted)	MICN=0.414Vpp/2	-	80	-	dB
	THD+N	1kHz, 18dB Gain	-	-85	-	dB
	Output Level	MICP=0.208Vpp/2	-	920	-	mFFS
	SNR(A-weighted)	MICN=0.208Vpp/2	-	85	-	dB
	THD+N	1kHz, 24dB Gain	-	-80	-	dB
	Output Level	MICP=0.104Vpp/2	-	920	-	mFFS
	SNR(A-weighted)	MICN=0.104Vpp/2	-	80	-	dB
	THD+N	1kHz, 30dB Gain	-	-75	-	dB

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
	Output Level	MICP=0.053Vpp/2	-	920	-	mFFS
	SNR(A-weighted)	MICN=0.053Vpp/2	-	80	-	dB
	THD+N	1kHz, 36dB Gain	-	-70	-	dB
	FMINL via ADC					
	Output Level	FMINL=1.65Vpp 1kHz 0dB Gain	-	905	-	mFFS
	SNR(A-weighted)		-	95	-	dB
	THD+N		-	-85	-	dB

4.9 MIPI DPHY Electrical Characteristics

This section describes some test parameters for MIPI DPHY based on D-PHY Physical Layer Conformance Test Suite Version 1.00.

Table 4-9 MIPI DPHY CTS Reference

Symbol	Parameters	Min	Typ	Max	Unit
Data Lane HS-TX Parameters					
$V_{OD(0)}$	Data Lane HS-TX Differential Voltages	-	222.4		mV
$V_{OD(1)}$	Data Lane HS-TX Differential Voltages	-	220.6	-	mV
ΔV_{OD}	Data Lane HS-TX Differential Voltage Mismatch	-	3	-	mV
t_R	Data Lane HS-TX 20%-80% Rise Time	-	0.305	-	UI
t_F	Data Lane HS-TX 80%-20% Fall Time		0.301	-	UI
Clock Lane HS-TX Parameters					
$V_{OD(0)}$	Clock Lane HS-TX Differential Voltages	-	264		mV
$V_{OD(1)}$	Clock Lane HS-TX Differential Voltages	-	224	-	mV
ΔV_{OD}	Clock Lane HS-TX Differential Voltage Mismatch	-	40	-	mV
t_R	Clock Lane HS-TX 20%-80% Rise Time	-	0.32	-	UI
t_F	Clock Lane HS-TX 80%-20% Fall Time		0.33	-	UI

4.10 External Clock Source Electrical Characteristics

4.10.1 High-speed Crystal/Ceramic Resonator Characteristics

The high-speed external clock can be supplied with a 24 MHz crystal resonator (oscillation mode). The 24 MHz crystal resonator provides 24 MHz reference clock which is connected to the DXIN and DXOUT terminals.

Table 4-10 High-speed 24 MHz Crystal Requirements

Symbol	Parameter	Min	Typ	Max	Unit
f_{X24M_IN}	Crystal parallel resonance frequency	-	24	-	MHz
	Crystal frequency stability and tolerance at 25 °C ⁽¹⁾	-50	-	+50	ppm
	Oscillation mode	Fundamental			-
C_0	Shunt capacitance ⁽²⁾	-	6.5	-	pF

1. The 50 ppm frequency stability and tolerance can meet the requirement of the device. We recommend selecting 20 ppm crystal devices.
2. The 6.5 pF is only a simulation value. The crystal shunt capacitance (C_0) is given by the crystal manufacturer.

Table 4-11 Crystal Circuit Parameters

Symbol	Parameter
C_1	C_1 capacitance
C_2	C_2 capacitance
C_L	Equivalent load capacitance, specified by the crystal manufacturer
C_0	Crystal shunt capacitance, specified by the crystal manufacturer
C_{shunt}	Total shunt capacitance

Frequency stability mainly requires that the total load capacitance (C_L) be constant. The crystal manufacturer typically specifies a total load capacitance which is the series combination of C_1 , C_2 , and C_{shunt} .

The total load capacitance is $C_L = [(C_1 * C_2) / (C_1 + C_2)] + C_{shunt}$.

- C_1 and C_2 represent the total capacitance of the respective PCB trace, load capacitor, and other components (excluding the crystal) connected to each crystal terminal. C_1 and C_2 are usually the same size.
- C_{shunt} is the crystal shunt capacitance (C_0) plus any mutual capacitance ($C_{pkg} + C_{PCB}$) seen across the DXIN and DXOUT signals.

In the application, the crystal resonator and the load capacitors must be placed close to the oscillator pins in order to minimize output distortion and the startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics.

4.11 Interface Timing Characteristics

4.11.1 SMHC Interface Timing

4.11.1.1 HS-SDR Mode



NOTE

IO voltage is 1.8V or 3.3V.

Figure 4-2 SMHC HS-SDR Mode Output Timing Diagram

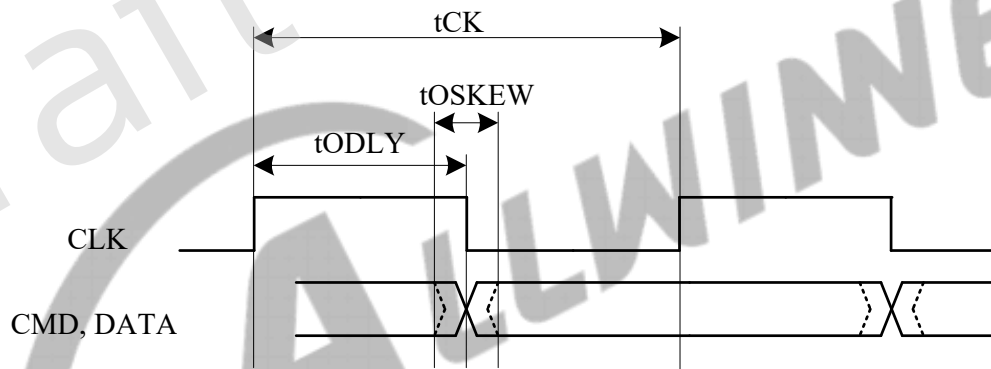


Table 4-12 SMHC HS-SDR Mode Output Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
CLK					
Clock frequency	tCK	0	50	50	MHz
Duty Cycle	DC	45	50	55	%
Output CMD, DATA(referenced to CLK)					
CMD, Data output delay time	tODLY	-	0.25	0.5	UI
Data output delay skew time	tOSKEW	-	-	0.884	ns
(1) The Unit Interval (UI) is 1-bit nominal time. For example, UI=20 ns at 50 MHz.					
(2) The driver strength level of GPIO is 2 for test.					

Figure 4-3 SMHC HS-SDR Mode Input Timing Diagram

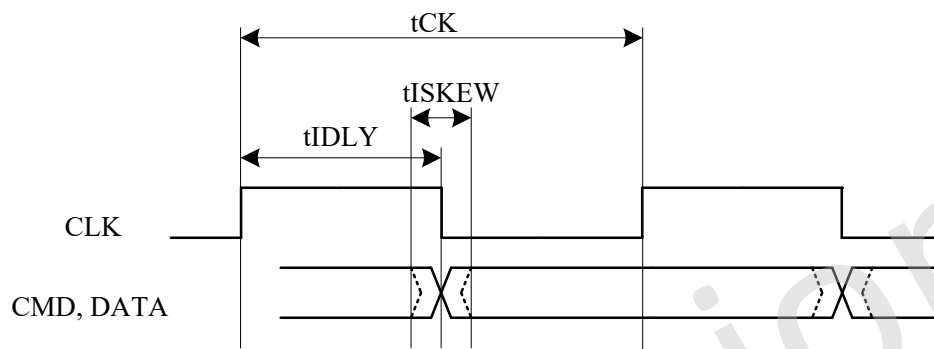


Table 4-13 SMHC HS-SDR Mode Input Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
CLK					
Clock frequency	tCK	0	50	50	MHz
Duty Cycle	DC	45	50	55	%
Input CMD, DATA(referenced to CLK 50MHz)					
Data input delay in SDR mode. It includes the PCB delay time of Clock, the PCB delay time of Data and the data output delay of Device	tIDLY	-	-	20	ns
Data input skew time in SDR mode	tISKEW	-	-	0.858	ns
The driver strength level of GPIO is 2 for test.					

4.11.1.2 HS-DDR Mode

Figure 4-4 SMHC HS-DDR Mode Output Timing Diagram

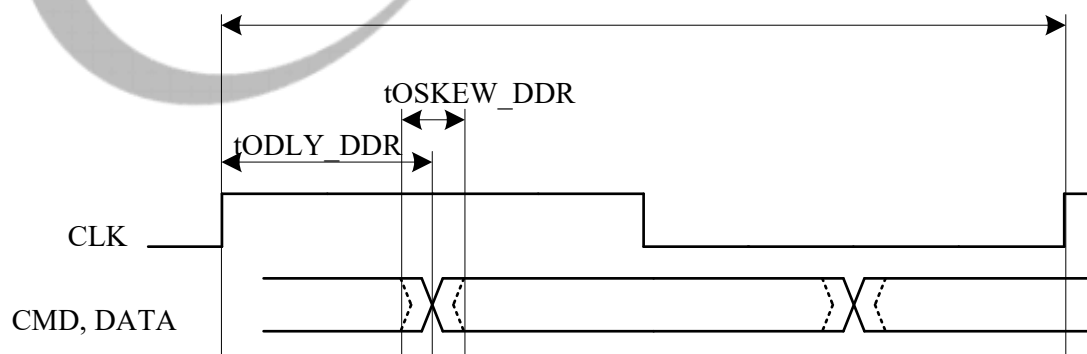


Table 4-14 SMHC HS-DDR Mode Output Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
-----------	--------	-----	-----	-----	------

Parameter	Symbol	Min	Typ	Max	Unit
CLK					
Clock frequency	tCK	0	50	50	MHz
Duty Cycle	DC	45	50	55	%
Output CMD, DATA(referenced to CLK)					
CMD, Data output delay time in DDR mode	tODLY-DDR	-	0.25	0.25	UI
Data output delay skew time	tOSKEW	-	-	0.884	ns
(1) The Unit Interval (UI) is 1-bit nominal time. For example, UI=20 ns at 50 MHz. (2) The driver strength level of GPIO is 2 for test.					

Figure 4-5 SMHC HS-DDR Mode Input Timing Diagram

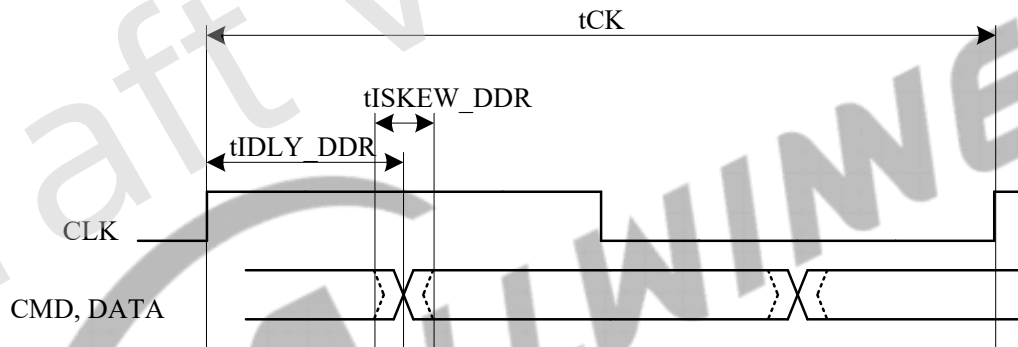


Table 4-15 SMHC HS-DDR Mode Input Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
CLK					
Clock frequency	tCK	0	50	50	MHz
Duty Cycle	DC	45	50	55	%
Input CMD, DATA(referenced to CLK 50MHz)					
Data input delay in DDR mode. It includes the PCB delay time of Clock, the PCB delay time of Data and the data output delay of Device	tIDLY-DDR	-	-	8.3	ns
Data input skew time in DDR mode	tISKEW-DDR	-	-	0.858	ns
The driver strength level of GPIO is 2 for test.					

4.11.1.3 SDR104 Mode

Figure 4-6 SMHC SDR104 Mode Host Output and Device Input Timing Diagram

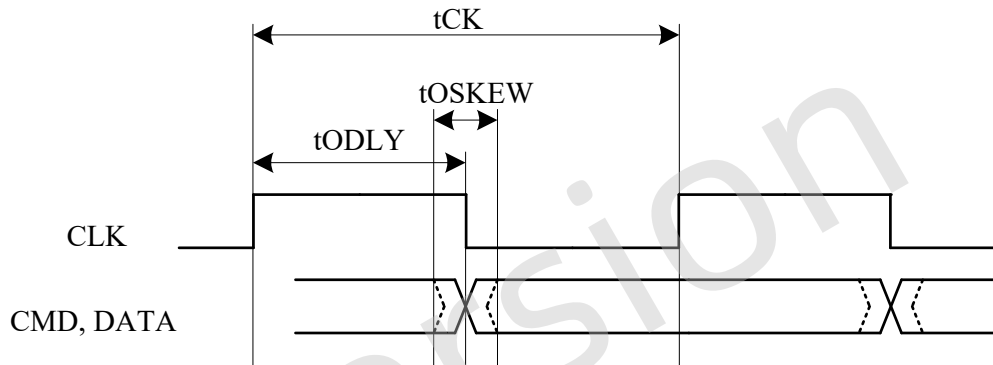


Table 4-16 SMHC SDR104 Mode Host Output and Device Input Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
CLK					
Clock frequency	t_{CK}	-	-	150	MHz
Duty Cycle	DC	45	50	55	%
Rise time, fall time	t_{TLH} , t_{THL}	-	-	0.2	UI
Host Output CMD, DATA (referenced to CLK)					
Host CMD, Data output delay time	t_{ODLY}	-	0.25	0.5	UI
Host Data output delay skew time	t_{OSKEW}	-	-	0.884	ns
(1) The Unit Interval (UI) is 1-bit nominal time. For example, UI=10 ns at 100 MHz.					
(2) The driver strength level of GPIO is 3 for test.					

Figure 4-7 SMHC SDR104 Mode Host Input and Device Output Timing Diagram

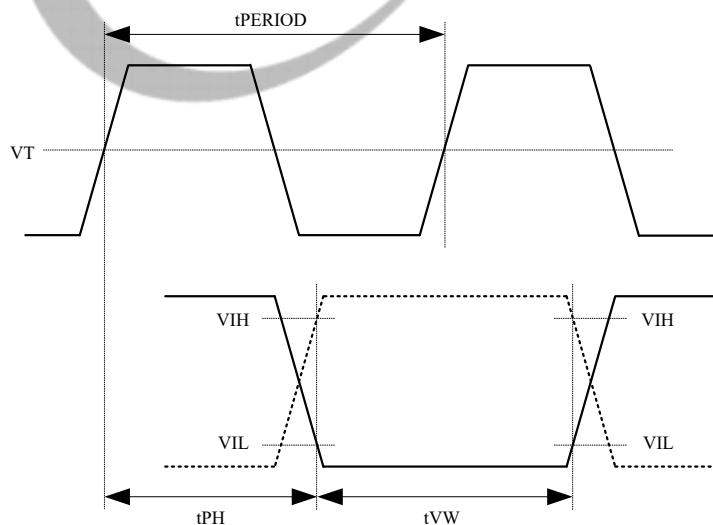


Table 4-17 SMHC SDR104 Mode Host Input and Device Output Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit	Remark
CLK						
Clock Period	tPERIOD	6.66	-	-	ns	Max: 150 MHz
Duty Cycle	DC	45	50	55	%	
Rise time, fall time	tTLH, tTHL	-	-	0.2	UI	
Host Input CMD, DATA (referenced to CLK)						
Device Output delay	tPH	0	-	2	UI	
Device Output delay variation due to temperature change after tuning	dPH	-350 ⁽³⁾	-	1550 ⁽⁴⁾	ps	
Device CMD, Data valid window	tVW	0.575	-	-	UI	
(1) The Unit Interval (UI) is 1-bit nominal time. For example, UI=10 ns at 100 MHz. (2) The driver strength level of GPIO is 3 for test. (3) Temperature variation: -20 °C. (4) Temperature variation: 90 °C.						

4.11.2 LCD Interface Timing

Figure 4-8 HV_IF Vertical Timing

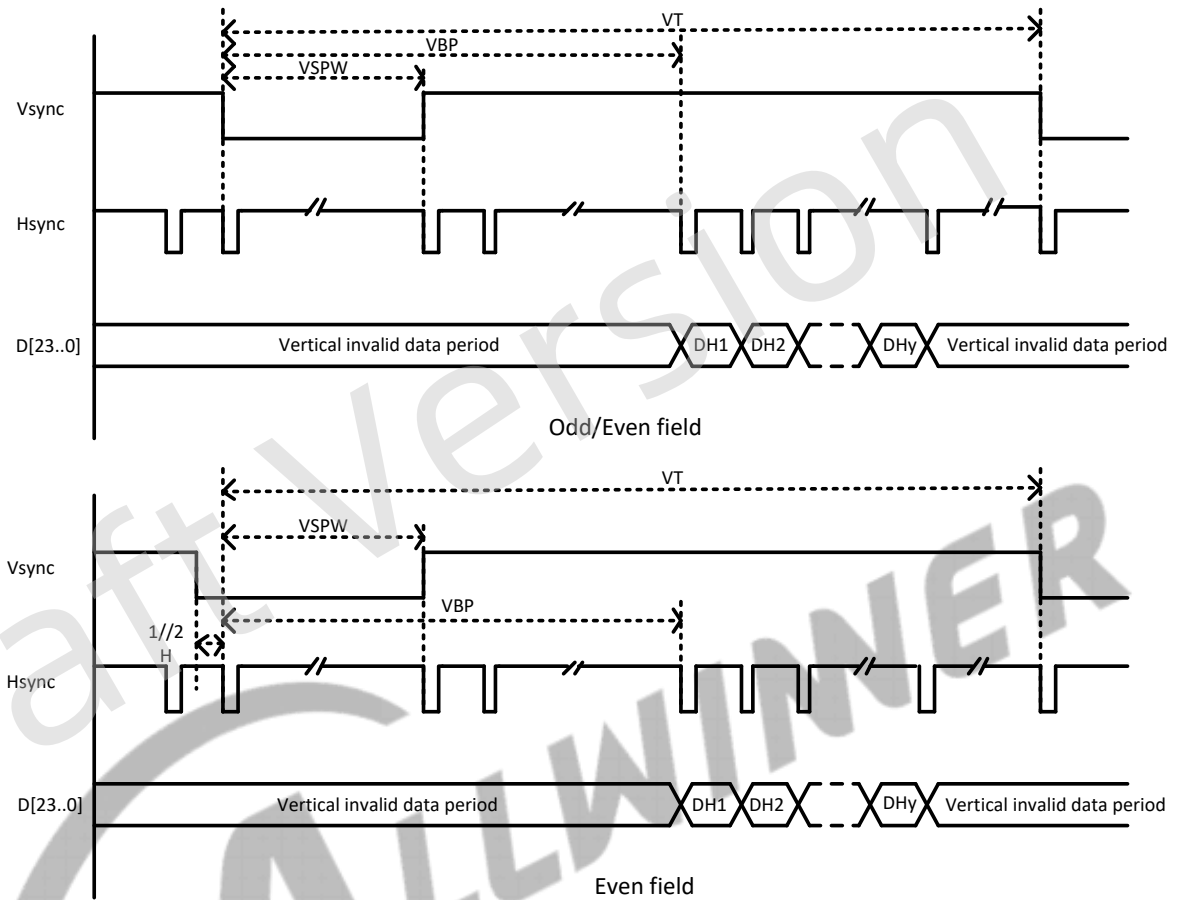


Figure 4-9 HV_IF Horizontal Timing

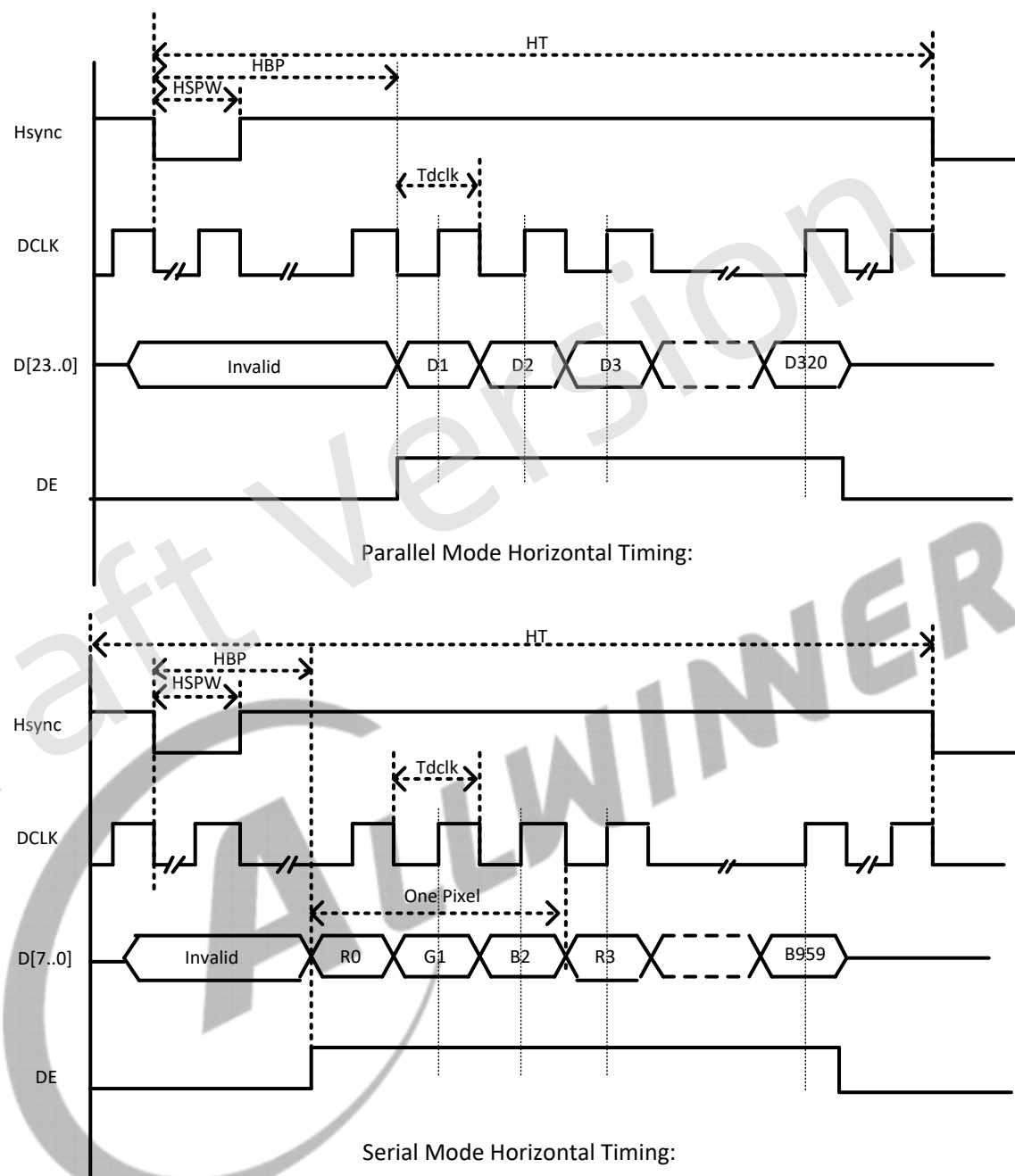


Table 4-18 LCD HV_IF Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
DCLK Cycle Time	tDCLK	5.9	-	-	ns
Hsync Period Time	tHT	-	HT+1	-	tDCLK
Hsync Width	tHSPW	-	HSPW+1	-	tDCLK
Hsync Back Porch	tHBP	-	HBP+1	-	tDCLK
Vsync Period Time	tVT	-	VT/2	-	tHT
Vsync Width	tVSPW	-	VSPW+1	-	tHT

Parameter	Symbol	Min	Typ	Max	Unit
Vsync Back Porch	tVBP	-	VBP+1	-	tHT
(1) Vsync: Vertical sync, indicates one new frame. (2) Hsync: Horizontal sync, indicate one new scan line. (3) DCLK: Dot clock, pixel data are sync by this clock. (4) LDE: LCD data enable. (5) LD[23..0]: 24Bit RGB/YUV output from input FIFO for panel.					

4.11.3 MIPI DPHY Interface Timing

Figure 4-10 MIPI DPHY Timing

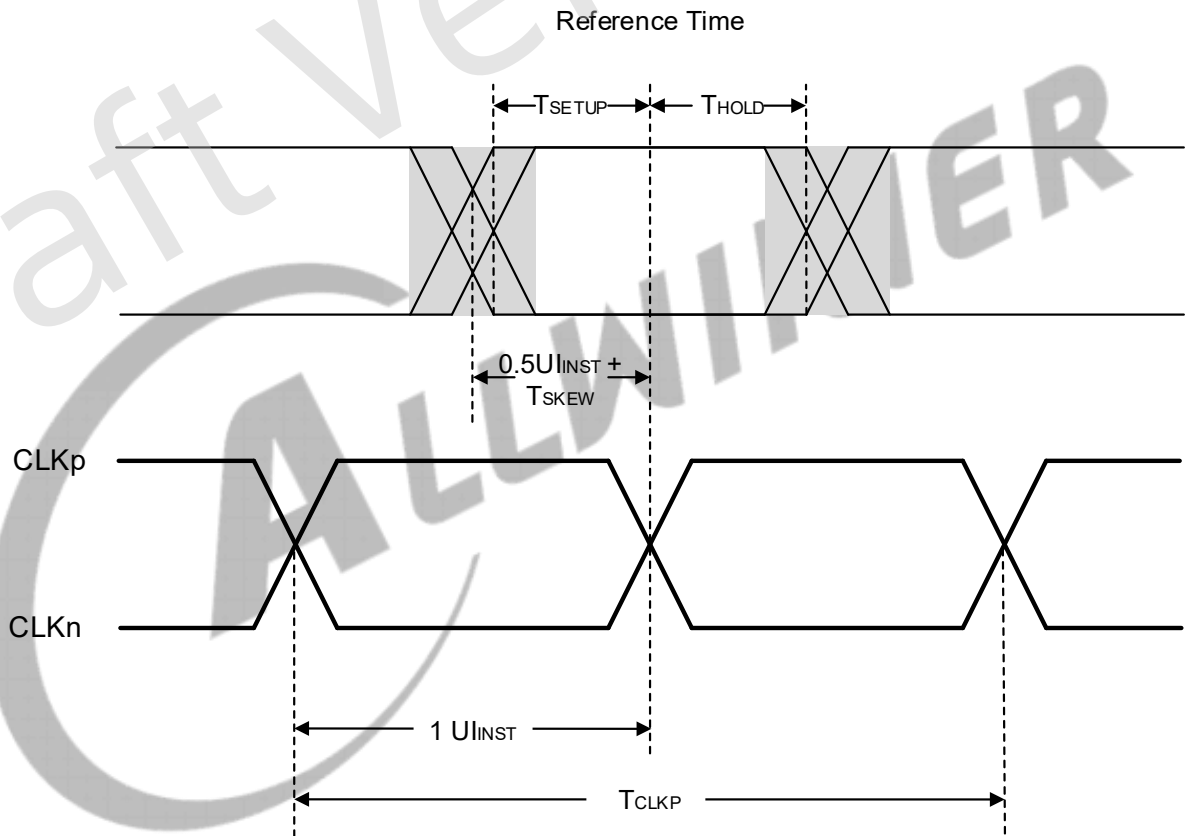


Table 4-19 MIPI DPHY Timing Constants

Parameter	Symbol	Units in Uinst			Operational Frequency in Gbps	
		Min	Max	Total	Min	Max
Data to Clock Skew	$T_{skew[tx]}$	-0.15	0.15	0.3	0.08	1.0
		-0.20	0.20	0.4	>1.0	1.5
Data to Clock Setup Time	$T_{setup[rx]}$	0.15	-	-	0.08	1.0

Parameter	Symbol	Units in Ulnst			Operational Frequency in Gbps	
		Min	Max	Total	Min	Max
		0.20			>1.0	1.5
Clock to Data Hold Time	$T_{hold[rx]}$	0.15	-	-	0.08	1.0
		0.20			>1.0	1.5

4.11.4 SPI Interface Timing

Figure 4-11 SPI Writing Timing

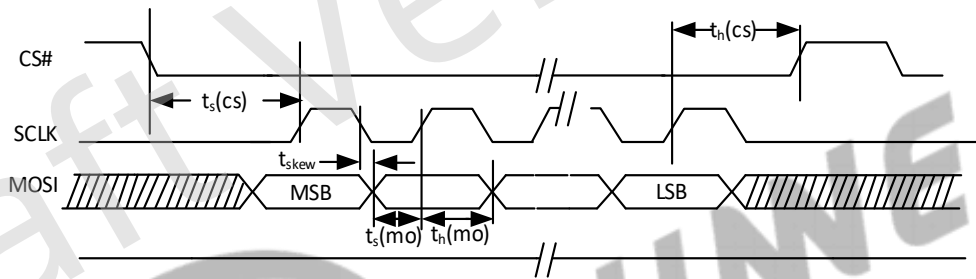


Figure 4-12 SPI Reading Timing

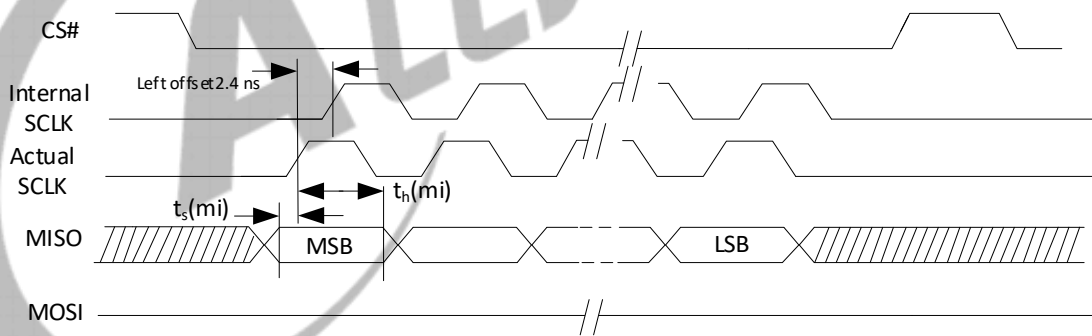


Table 4-20 SPI Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
CS# Active Setup Time	$t_s(cs)$	-	$2T^{(1)}$	-	ns
CS# Active Hold Time	$t_h(cs)$	-	$2T^{(1)}$	-	ns
CLK/Data output skew time	$t_{skew}^{(2)}$	-	-	1	ns
Data output Delay Time	$t_v(mo)$	-	$T^{(1)}/2-3$	-	ns
Data output Hold Time	$t_h(mo)$	-	$T^{(1)}/2-3$	-	ns
Data In Setup Time	$t_s(mi)$	0.2	-	-	ns

Parameter	Symbol	Min	Typ	Max	Unit
Data In Hold Time	$t_{h(mi)}$	0.2	-	-	ns
(1) T is the cycle of clock. (2) t_{skew} is the output skew time between SCLK and MOSI. SCLK may be either faster or slower than MOSI.					

4.11.5 SPI-DBI Interface Timing

Figure 4-13 DBI 3-line Serial Interface Timing

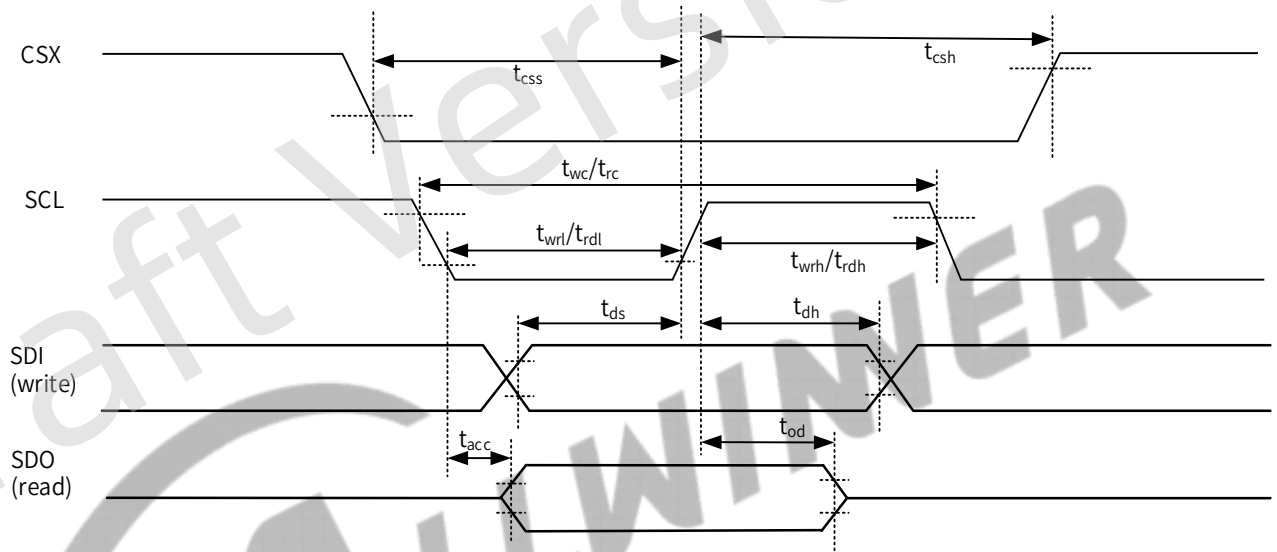


Table 4-21 DBI 3-line Serial Interface Write Timing Parameters

Signal	Parameter	Symbol	Min	Max	Unit
CSX	Chip select setup time	t_{css}	15		ns
SCL	Write cycle	t_{wc}	16		ns
	Control pulse H duration	t_{wrh}	7		ns
	Control pulse L duration	t_{wrl}	7		ns
SDI/SDO	Data setup time	t_{ds}	7 ⁽¹⁾		ns
	Data hold time	t_{dt}	7 ⁽¹⁾		ns
Note: Range of required clock frequency: 0-60 MHz.					

Table 4-22 DBI 3-line Serial Interface Read Timing Parameters

Signal	Parameter	Symbol	Min	Max	Unit
CSX	Chip select setup time	t_{csh}	60		ns

Signal	Parameter	Symbol	Min	Max	Unit
SCL	Read cycle	t_{rc}	150		ns
	Control pulse H duration	t_{rdh}	60		ns
	Control pulse L duration	t_{rdl}	60		ns
SDI/SDO	Read access time	t_{racc}	10 ⁽¹⁾	50	ns
	Output disable time	t_{od}	15 ⁽¹⁾	50	ns
Note: Range of required clock frequency: 0-6.67 MHz.					

Figure 4-14 DBI 4-line Serial Interface Timing

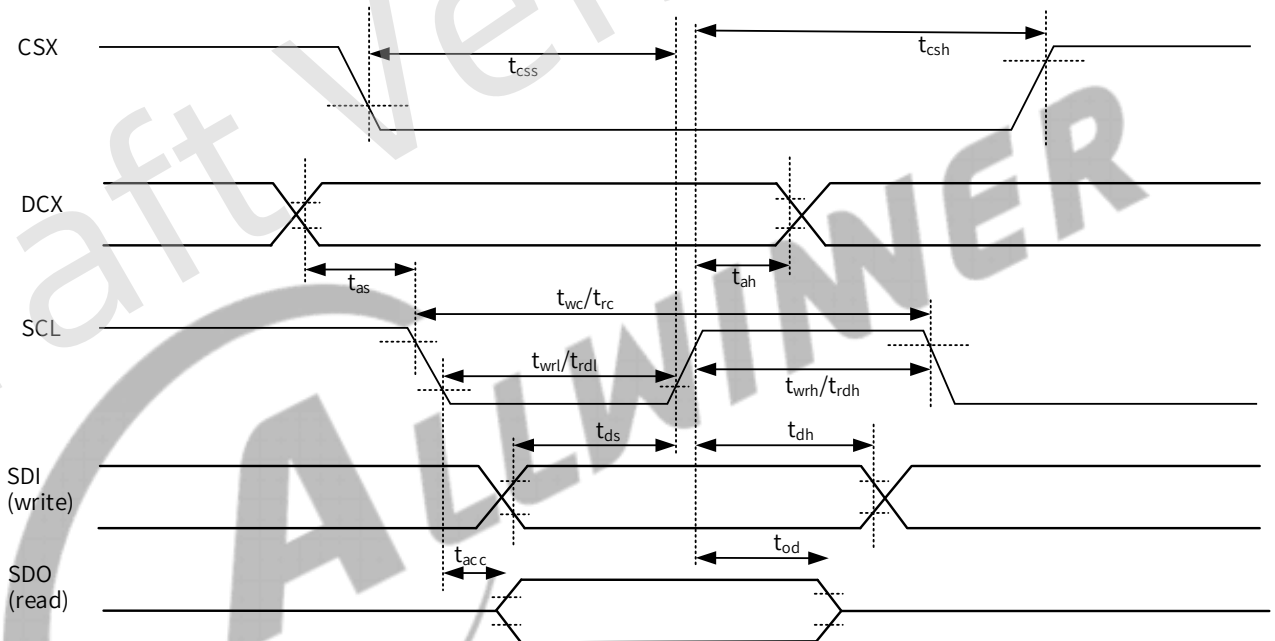


Table 4-23 DBI 4-line Serial Interface Write Timing Parameters

Signal	Parameter	Symbol	Min	Max	Unit
CSX	Chip select setup time	t_{css}	15		ns
DCX	Address setup time	t_{as}	10		ns
	Address hold time	t_{ah}	10		ns
SCL	Write cycle	t_{wc}	16		ns
	Control pulse H duration	t_{wrh}	7		ns
	Control pulse L duration	t_{wrl}	7		ns
SDI/SDO	Data setup time	t_{ds}	7 ⁽¹⁾		ns
	Data hold time	t_{dt}	7 ⁽¹⁾		ns

Signal	Parameter	Symbol	Min	Max	Unit
	Output disable time	t_{od}	15 ⁽¹⁾	50	ns
Note: Range of required clock frequency: 0-60 MHz.					

Table 4-24 DBI 4-line Serial Interface Read Timing Parameters

Signal	Parameter	Symbol	Min	Max	Unit
CSX	Chip select setup time	t_{csh}	60		ns
DCX	Address setup time	t_{as}	10		ns
	Address hold time	t_{ah}	10		ns
SCL	Read cycle	t_{rc}	150		ns
	Control pulse H duration	t_{rdh}	60		ns
	Control pulse L duration	t_{rdl}	60		ns
SDI/SDO	Read access time	t_{racc}	-	50	ns
	Output disable time	t_{od}	15 ⁽¹⁾	50	ns
Note: Range of required clock frequency: 0-6.67 MHz.					

4.11.6 UART Interface Timing

Figure 4-15 UART RX Timing

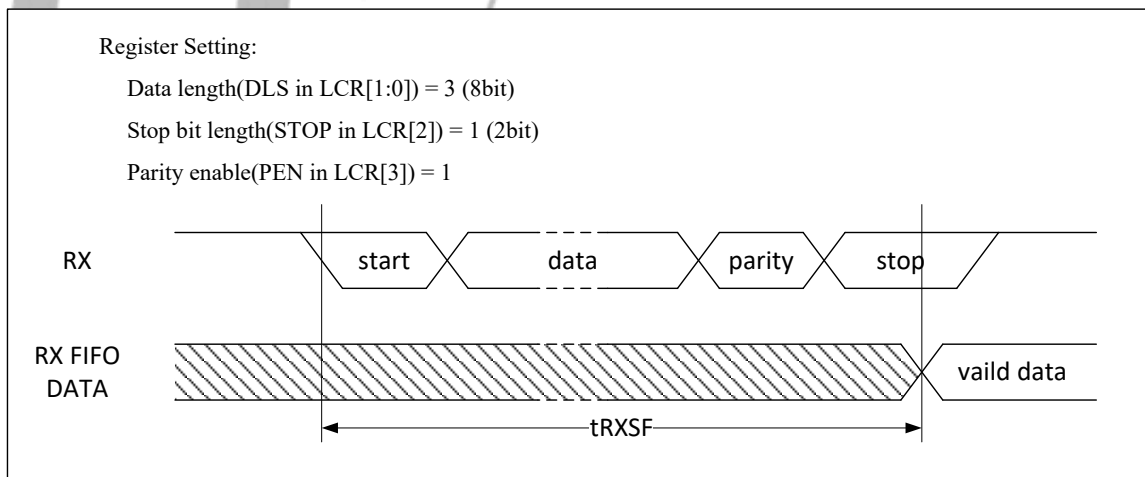


Figure 4-16 UART nCTS Timing

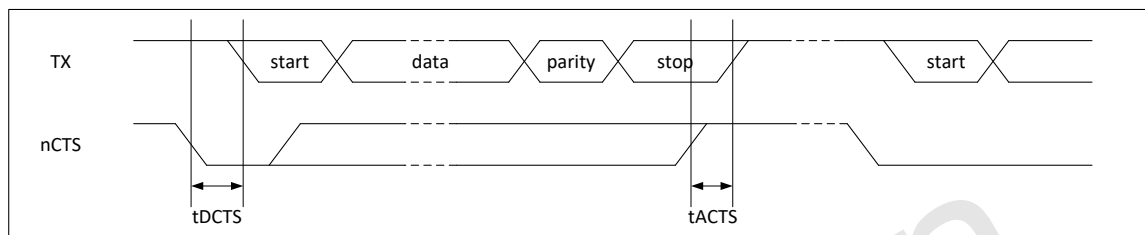


Figure 4-17 UART nRTS Timing

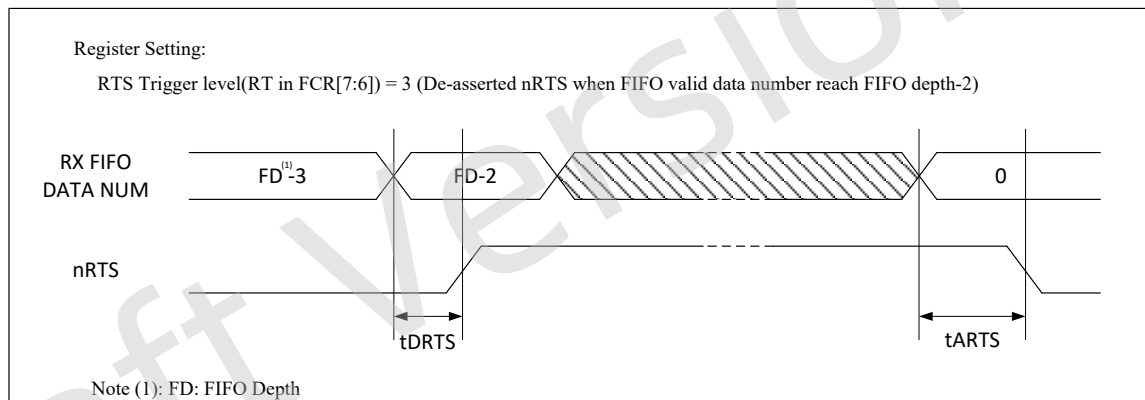


Table 4-25 UART Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
RX start to RX FIFO	tRXSF	$10.5 \cdot \text{BRP}^{(1)}$	-	$11 \cdot \text{BRP}^{(1)}$	ns
Delay time of de-asserted nCTS to TX strat	tDCTS	-	-	$\text{BRP}^{(1)}$	ns
Step time of asserted nCTS to stop next transmission	tACTS	$\text{BRP}^{(1)} / 4$	-	-	ns
Delay time of de-asserted nRTS	tDRTS	-	-	$\text{BRP}^{(1)}$	ns
Delay time of asserted nRTS	tARTS	-	-	$\text{BRP}^{(1)}$	ns

(1) BRP: Baud-Rate Period.

4.11.7 TWI Interface Timing

Figure 4-18 TWI Timing

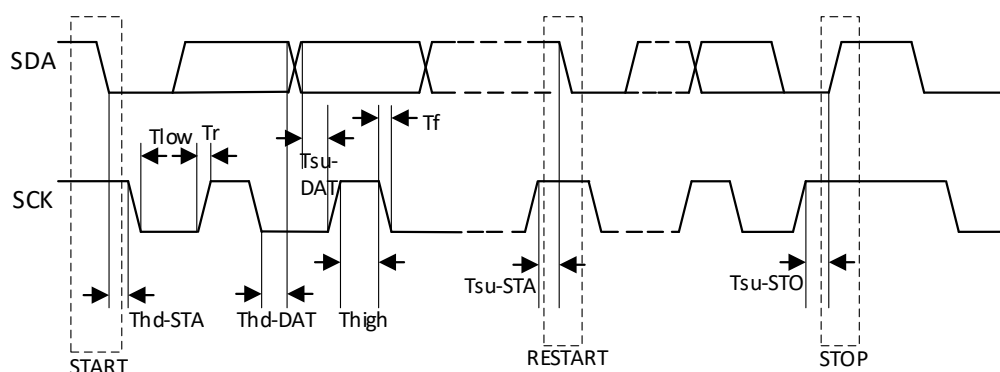


Table 4-26 TWI Timing Parameters

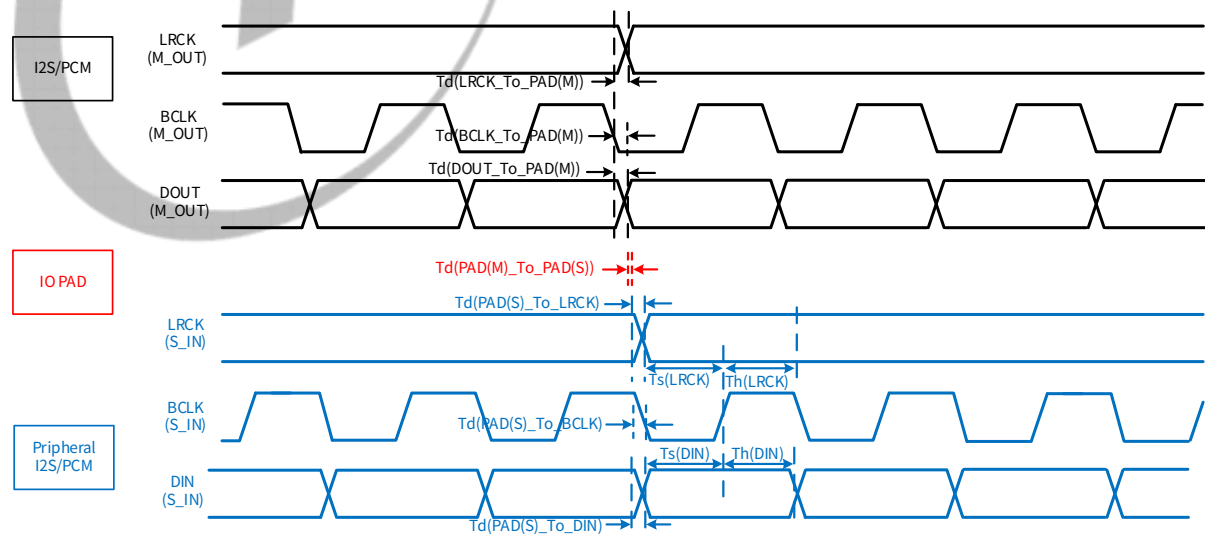
Parameter	Symbol	Standard mode		Fast mode		Unit
		Min	Max	Min	Max	
SCK clock frequency	Fsck	0	100	0	400	kHz
Setup Time In Start	Tsu-STA	4.7	-	0.6	-	us
Hold Time In Start	Thd-STA	4.0	-	0.6	-	us
Setup Time In Data	Tsu-DAT	250	-	100	-	ns
Hold Time In Data	Thd-DAT	0	-	0	-	us
Setup Time In Stop	Tsu-STO	4.0	-	0.6	-	us
SCK Low level Time	Tlow	4.7	-	1.3	-	us
SCK High level Time	Thigh	4.0	-	0.6	-	us
SCK/SDA Falling Time	Tf	-	300	20	300	ns
SCK/SDA Rising Time	Tr	-	1000	20	300	ns

4.11.8 I2S/PCM Interface Timing

4.11.8.1 Data Output timing of I2S/PCM in Master mode

The Data Output timing of I2S/PCM in Master mode and the Data Input timing of Peripheral I2S/PCM in Slave mode show in Figure 4-19.

Figure 4-19 Data Output Timing of I2S/PCM in Master Mode



The Data Output timing parameters of I2S/PCM in Master mode and The Data Input timing parameters of Peripheral I2S/PCM in Slave mode show in Table 4-27.

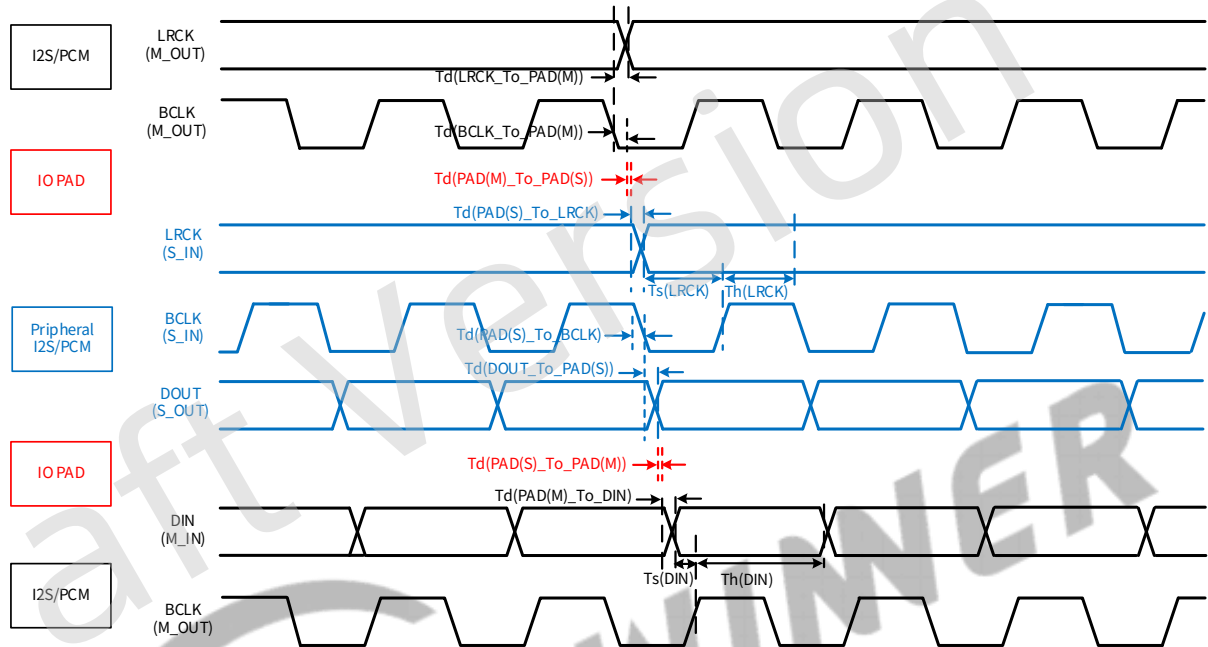
Table 4-27 Data Output Timing Parameters of I2S/PCM in Master Mode

Parameter		Min	Max	Skew	Units
Sequence requirement of internal signal of I2S/PCM in Master mode					
T _d (LRCK_To_PA D(M))	LRCK to PAD(M) Delay	/	T1<6.5 (restriction)	T _{w1} <2.5(require ment)	ns
T _d (BCLK_To_PA D(M))	BCLK to PAD(M) Delay	/	T2<6.5(restricti on)		
T _d (DOUT_To_PA D(M))	DOUT to PAD(M) Delay	/	T3<6.5(restricti on)		
Sequence requirement of the IO pad of I2S/PCM in Master mode connecting to the external IO pad of Peripheral I2S/PCM in Slave mode					
T _d (PAD(M)_To_P AD(S))	LRCK PAD(M) to LRCK PAD(S) Delay	/	T4*<7.0(estimat ion)	T _{w2} *<1.0(requir ement)	ns
	BCLK PAD(M) to BCLK PAD(S) Delay	/	T5*<7.0(estimat ion)		
	DOUT PAD(M) to DIN PAD(S) Delay	/	T6*<7.0(estimat ion)		
Sequence requirement of internal signal of Peripheral I2S/PCM in Slave mode					
T _d (PAD(S)_To_L RCK)	PAD(S) to LRCK Delay	/	T7*<6.5(assum ption)	T _{w3} *<2.5(requir ement)	ns
T _d (PAD(S)_To_B CLK)	PAD(S) to BCLK Delay	/	T8*<6.5(assum ption)		
T _d (PAD(S)_To_DI N)	PAD(S) to DIN Delay	/	T9*<6.5(assum ption)	/	/
T _s (LRCK)	LRCK Setup Slack	T10*(anal ysis)	/	/	ns
T _h (LRCK)	LRCK Hold Slack	T11*(anal ysis)	/	/	ns
T _s (DIN)	DIN Setup Slack	T12*(anal ysis)	/	/	ns
T _h (DIN)	DIN Hold Slack	T13*(anal ysis)	/	/	ns

4.11.8.2 Data Input timing of I2S/PCM in Master mode

The Data Input timing of I2S/PCM in Master mode and the Data Output timing of Peripheral I2S/PCM in Slave mode show in Figure 4-20.

Figure 4-20 Data Input Timing of I2S/PCM in Master Mode



The Data Input timing parameters of I2S/PCM in Master mode and The Data Output timing parameters of Peripheral I2S/PCM in Slave mode are shown in Table 4-28.

Table 4-28 Data Input Timing Parameters of I2S/PCM in Master Mode

Parameter		Min	Max	Skew	Units
Sequence requirement of internal signal of I2S/PCM in Master mode					
Td(LRCK_To_PAD(M))	LRCK to PAD(M) Delay	/	T1<6.5(requirement)	Tw1<2.5	ns
Td(BCLK_To_PAD(M))	BCLK to PAD(M) Delay	/	T2<6.5(requirement)	(estimation)	ns
Sequence requirement of the IO pad of I2S/PCM in Master mode connecting to the external IO pad of Peripheral I2S/PCM in Slave mode					
Td(PAD(M)_To_PAD(S))	LRCK PAD(M) to LRCK PAD(S) Delay	/	T3*<7.0(requirement)	Tw2*<1.0	ns
	BCLK PAD(M) to BCLK PAD(S) Delay		T4*<7.0(requirement)	(estimation)	

Parameter		Min	Max	Skew	Units
Sequence requirement of internal signal of Peripheral I2S/PCM in Slave mode					
Td(PAD(S)_To_LRCK)	PAD(S) to LRCK Delay	/	$T5^* < 6.5$ (requirement)	$Tw3^* < 2.5$ (estimation)	ns
Td(PAD(S)_To_BCLK)	PAD(S) to BCLK Delay	/	$T6^* < 6.5$ (requirement)		ns
Td(DOUT_To_PAD(S))	DOUT to PAD(S) Delay	/	$T7^* < 6.5$ (requirement)	/	ns
Ts(LRCK)	LRCK Setup Slack	$T8^*$ (analysis)	/	/	ns
Th(LRCK)	LRCK Hold Slack	$T9^*$ (analysis)	/	/	ns
Sequence requirement of the IO pad of I2S/PCM in Master mode connecting to the external IO pad of Peripheral I2S/PCM in Slave mode					
Td(PAD(S)_To_PAD(M))	DOUT PAD(S) to DIN PAD(M) Delay	/	$T10^* < 7.0$ (requirement)	/	ns
Sequence requirement of internal signal of I2S/PCM in Master mode					
Td(PAD(M)_To_DIN)	PAD(M) to DIN Delay	/	$T11 < 6.5$ (requirement)	/	ns
Ts(DIN)	DIN Setup Slack	$T12^*$ (analysis)	/	/	ns
Th(DIN)	DIN Hold Slack	$T13^*$ (analysis)	/	/	ns

4.11.9 DMIC Interface Timing

Figure 4-21 DMIC Timing

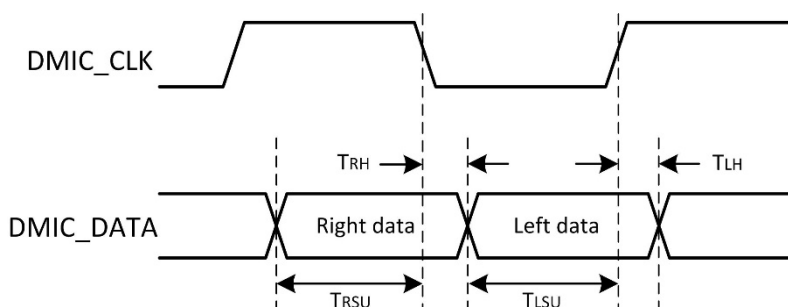


Table 4-29 DMIC Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
DMIC_DATA(Right) Setup Time to Falling Edge of DMIC_CLK	T_{RSU}	15	-	-	ns
DMIC_DATA(Right) Hold Time from Falling Edge of DMIC_CLK	T_{RH}	0	-	-	ns
DMIC_DATA(Left) Setup Time to Rising Edge of DMIC_CLK	T_{LSU}	15	-	-	ns
DMIC_DATA(Left) Hold Time From Rising edge of DMIC_CLK	T_{LH}	0	-	-	ns

4.11.10 OWA Interface Timing

Figure 4-22 OWA Timing

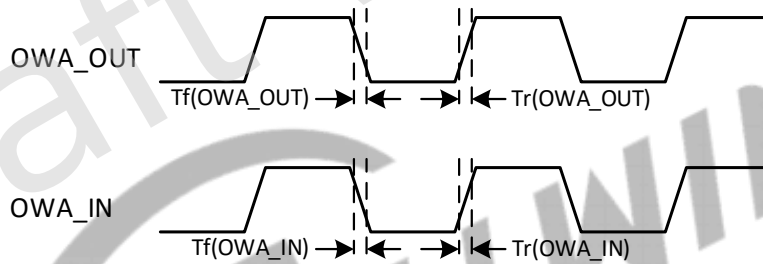


Table 4-30 OWA Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
OWA_OUT Rise Time	$Tr(OWA_OUT)$	-	-	8	ns
OWA_OUT Fall Time	$Tf(OWA_OUT)$	-	-	8	ns
OWA_IN Rise Time	$Tr(OWA_IN)$	-	-	4	ns
OWA_IN Fall Time	$Tf(OWA_IN)$	-	-	4	ns

4.12 Power-Up and Power-Down Sequence

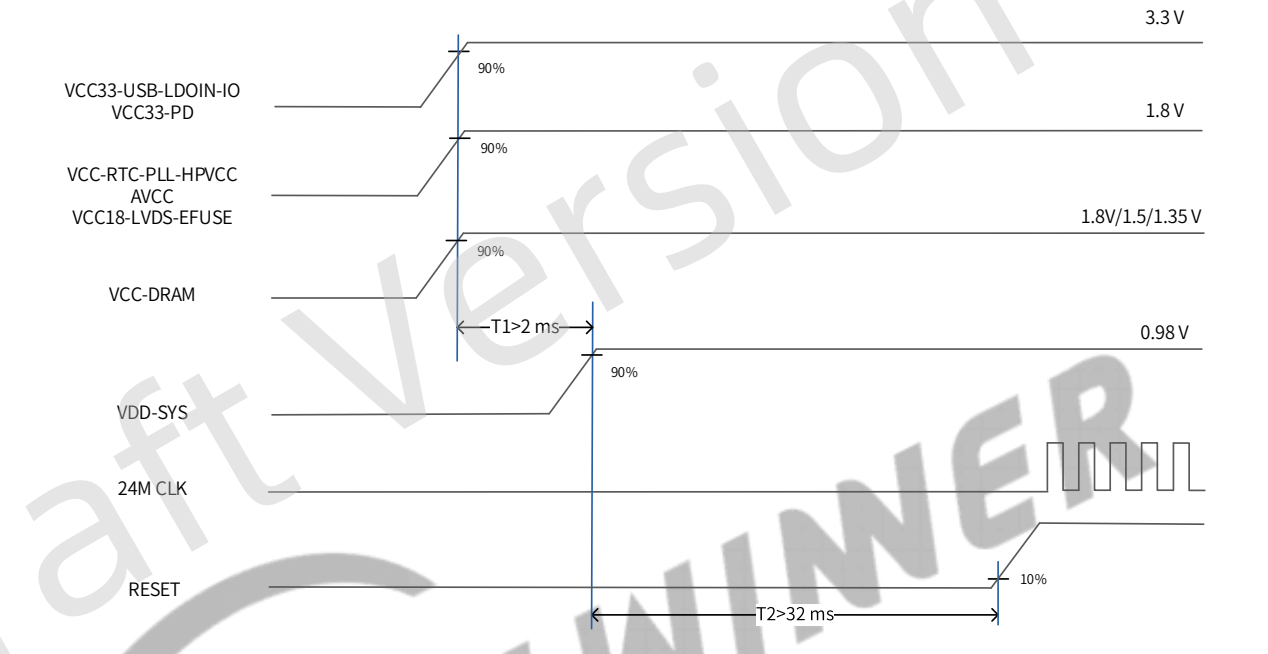
4.12.1 Power-Up Sequence

The following figure shows an example of the power-up sequence for the SoC. The description of the power-up sequence is as follows.

- The consequent steps in power-on sequence should not start before the previous step supplies have been stabilized within 90%~110% of their nominal voltage, unless stated otherwise.
- VCC33-USB-LDOIN-IO must be ramped before VDD-SYS with a minimum delay of 2 ms.

- VCC-DRAM needs be stable before SDRAM driver initialization.
- During the entire power on sequence, the RESET signal must be held on low until all other power rails (except 24 MHz CLK) are stable for more than 32 ms.
- 24MHz clock starts oscillating after the RESET signal is released.

Figure 4-23 Power-Up Sequence



NOTE

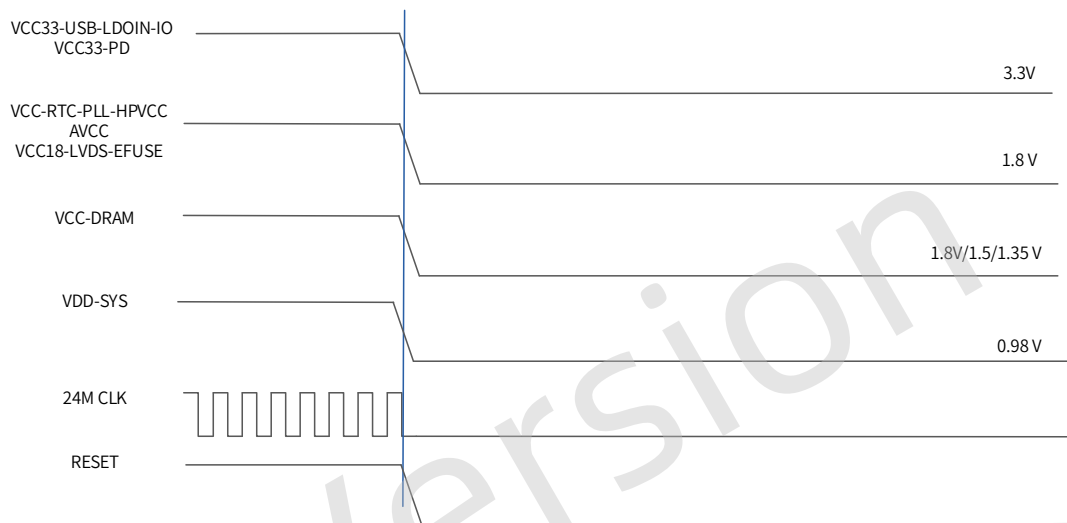
When some of PD0-PD19 I/Os are used as LVDS or DSI, and some are used as GPIO, the power-up sequence of VCC18-LVDS-EFUSE should be advanced to that of VCC33-PD, or the power-up sequence of VCC33-PD should be delayed after that of VCC18-LVDS-EFUSE.

4.12.2 Power-Down Sequence

The power-down requirements are as follows.

- After the RESET signal goes low, the 24 MHz clock starts to stop oscillating.
- No special restrictions for other power rails.

Figure 4-24 Power-Down Sequence



5 Temperature and Thermal Characteristics

5.1.1 Temperature

The following tables describe the temperature of the device

Table 5-1 Operating and Storage Temperature

Symbol	Parameter	Min	Max	Unit
T_a	Ambient Operating Temperature	-25	75	°C
T_{STG}	Storage Temperature	-40	150	°C

Table 5-2 Junction Temperature

Chip	Recommended Operating Temperature (T_j)		Absolute Maximum Junction Temperature	Unit
	Min	Max		
F135	-25	115	125	°C

5.1.2 Package Thermal Characteristics

The maximum chip junction temperature (T_{jmax}) must never exceed the values given in Table 5-2 Junction Temperature.

Failure to maintain a junction temperature within the range specified reduces operating lifetime, reliability, and performance, and may cause irreversible damage to the system. It is useful to calculate the exact power consumption and junction temperature to determine which the temperature will be best suited to the application. Therefore, the product should include thermal analysis and thermal design to ensure the operating junction temperature of the device is within functional limits.

The following tables show the thermal resistance characteristics of the device. These data are based on JEDEC JESD51 standard, because the actual system design and temperature could be different from JEDEC JESD51, these simulating data are a reference only and may not represent actual use-case values, please prevail in the actual application condition test.

Table 5-3 Package Thermal Characteristics

Symbol	Parameter	Min	Typ ⁽¹⁾⁽²⁾	Max	Unit
θ_{JA}	Junction-to-Ambient Thermal Resistance	-	23.65	-	°C/W
θ_{JB}	Junction-to-Board Thermal Resistance	-	18.5	-	°C/W
θ_{JC}	Junction-to-Case Thermal Resistance	-	3.98	-	°C/W

- (1) Reference document: JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions (b) Natural Convection (Still Air). Available from www.jedec.org.
- (2) The testing PCB is 4 layers, 114.5 mm x 76.2 mm body, and 1.6 mm thickness. Ambient temperature is 25 °C.

Draft Version

The Allwinner logo, featuring a stylized grey 'A' inside a circle, followed by the word 'ALLWINNER' in grey capital letters.

6 Pin Assignment

6.1.1 Pin Map

The following shows the QFP 128 pins, 14 mm x 14 mm pin map.

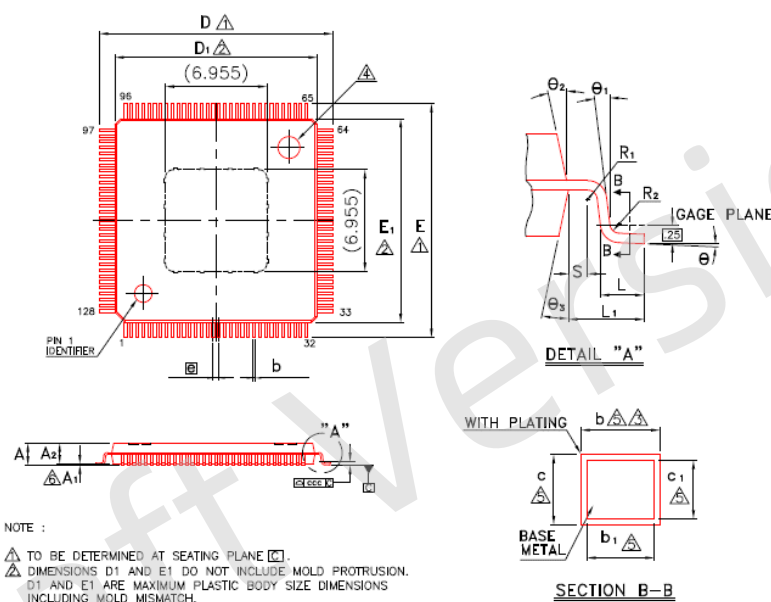
Figure 6-1 Pin Map

--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--

6.1.2 Package Dimension

The following figure shows the top, bottom, and side views of the package.

Figure 6-2 Package Dimension



Symbol	Dimension in mm			Dimension in inch		
	Min	Norm	Max	Min	Norm	Max
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.13	0.18	0.23	0.005	0.007	0.009
b1	0.13	0.16	0.19	0.005	0.006	0.007
c	0.09	—	0.20	0.004	—	0.008
c1	0.09	—	0.16	0.004	—	0.006
D	15.85	16.00	16.15	0.624	0.630	0.636
D1	13.90	14.00	14.10	0.547	0.551	0.555
E	15.85	16.00	16.15	0.624	0.630	0.636
E1	13.90	14.00	14.10	0.547	0.551	0.555
□	0.40 BSC			0.016 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
R1	0.08	—	—	0.003	—	—
R2	0.08	—	0.20	0.003	—	0.008
S	0.20	—	—	0.008	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	—	—	0°	—	—
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°
ccc	0.08			0.003		

TITLE : 128UD E-PAD LQFP (14x14x1.4 mm) PACKAGE OUTLINE-Cu L/FEFOOTPRINT 2.0mm			
APPR.			
PE.		DWG NO.	PCO2035
PD.		REV NO.	A
QM.		DATE	05/22/'15
CHK.		DWG.	Leo Deng

7 Carrier, Storage and Backing Information

7.1 Carrier

The following table shows matrix tray carrier information.

Table 7-1 Matrix Tray Carrier Information

Item	Color	Size	Note
Tray	Black	322.6 mm x 135.9 mm x 7.62 mm	90 Qty/Tray
Aluminum foil bags	Silvery white	540 mm x 300 mm x 0.14 mm	Vacuum packing Including HIC and desiccant Printing: RoHS symbol
Pearl cotton cushion (Vacuum bag)	White	12 mm x 680 mm x 185 mm	
Pearl cotton cushion (The Gap between vacuum bag and inner box)	White	Left-Right: 12 mm x 180 mm x 85 mm Front-Back: 12 mm x 350 mm x 70 mm	
Inner Box	White	396 mm x 196 mm x 96 mm	Printing: RoHS symbol 10 Tray/Inner box
Carton	White	420 mm x 410 mm x 320 mm	6 Inner box/Carton

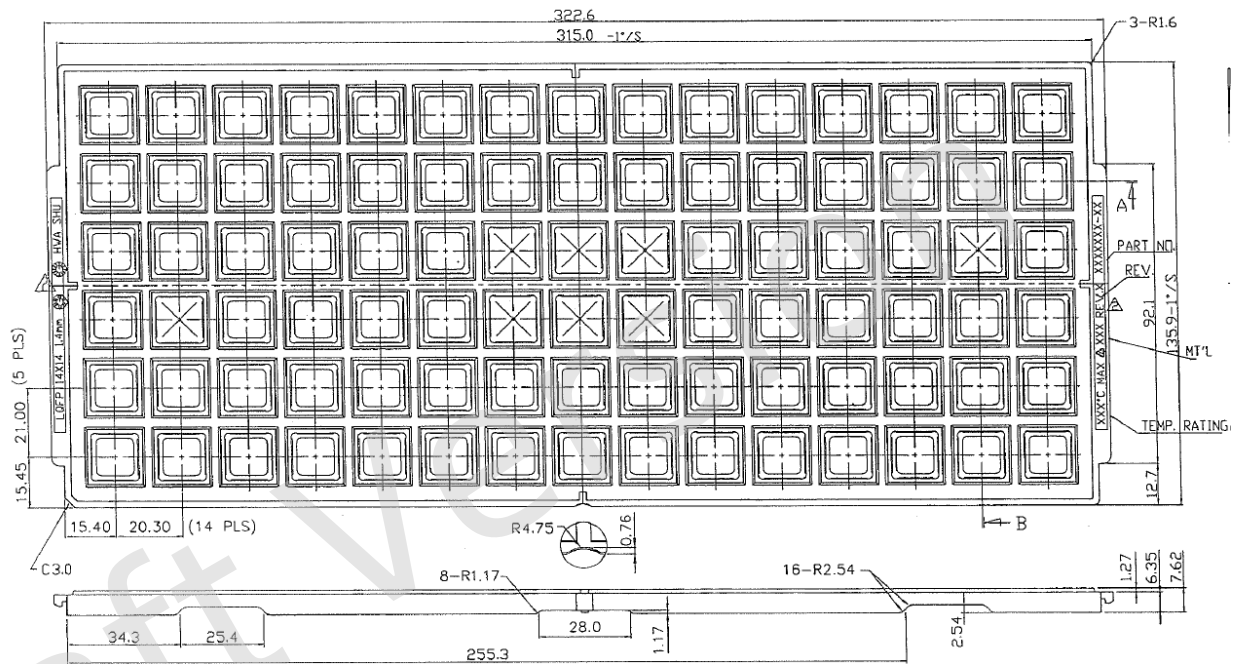
The following table shows packing quantity.

Table 7-2 Packing Quantity Information

Sample	Size	Qty/Tray	Tray/Inner Box	Full Inner Box Qty	Inner Box/Carton	Full Carton Qty
F135	14 mm x 14 mm	90	10	900	6	5400

The following figure shows tray dimension drawing.

Figure 7-1 Tray Dimension Drawing



7.2 Storage

Reliability is affected if any condition specified in section 7.2.2 and section 7.2.3 has been exceeded.

7.2.1 Moisture Sensitivity Level (MSL)

A package's MSL indicates its ability to withstand exposure after it is removed from its shipment bag, a low MSL device sample can be exposed on the factory floor longer than a high MSL device sample. Table 7-3 defines all MSL.

Table 7-3 MSL Summary

MSL	Out-of-bag floor life	Comments
1	Unlimited	30°C / 85%RH
2	1 year	30°C / 60%RH
2a	4 weeks	30°C / 60%RH
3	168 hours	30°C / 60%RH
4	72 hours	30°C / 60%RH
5	48 hours	30°C / 60%RH
5a	24 hours	30°C / 60%RH
6	Time on Label (TOL)	30°C / 60%RH

**NOTE**

The F135 device samples are classified as MSL3.

7.2.2 Bagged Storage Conditions

The following table defines the shelf life.

Table 7-4 Bagged Storage Conditions

Packing Mode	Vacuum packing
Storage Temperature	20(±2)°C
Storage Humidity	40%(±10%)RH
Shelf Life	12 months

7.2.3 Out-of-bag Duration

It is defined by the device MSL rating. The out-of-bag duration is as follows.

Table 7-5 Out-of-bag Duration

Storage Temperature	20(±2)°C
Storage Humidity	40%(±10%)RH
Moisture Sensitive Level (MSL)	3
Floor Life	168 hours

For no mention of storage rules in this document, refer to the latest *IPC/JEDEC J-STD-020C*.

7.3 Baking

It is not necessary to bake chips if the conditions specified in section 7.2.2 and section 7.2.3 have not been exceeded. It is necessary to bake chips if any condition specified in section 7.2.2 and section 7.2.3 has been exceeded.

It is necessary to bake chips if the storage humidity condition has been exceeded, we recommend that the device sample removed from its shipment bag for more than 2 days shall be baked to guarantee production.

Baking conditions: 125°C, 8 hours, nitrogen protection. Note that the baking should not exceed 1 times due to a risk of deformation.

8 Reflow Profile

All Allwinner chips provided for clients are lead-free RoHS-compliant products.

The reflow profile recommended in this document is a lead-free reflow profile that is suitable for pure lead-free technology or lead-free solder paste. If customers need to use lead solder paste, contact Allwinner FAE.

The following figure shows the appropriate reflow profile.

Figure 8-1 Lead-free Reflow Profile

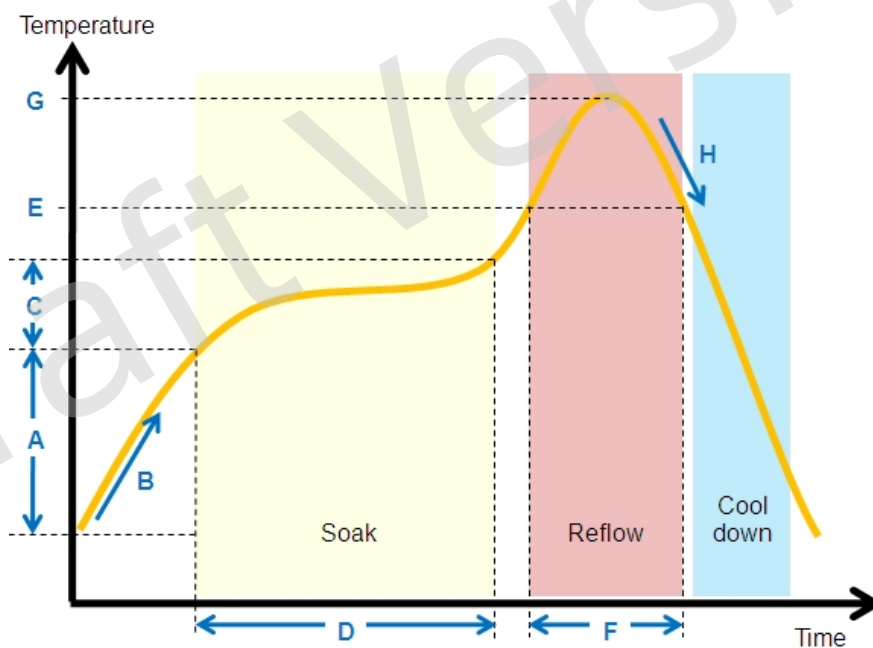


Table 8-1 Lead-free Reflow Profile Conditions

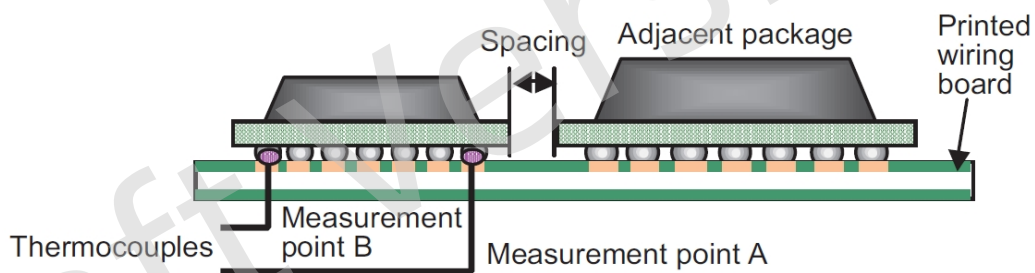
	QTI typical SMT reflow profile conditions (for reference only)	
	Step	Reflow condition
Environment	N2 purge reflow usage (yes/no)	Yes, N2 purge used
	If yes, O2 ppm level	O2 < 1500 ppm
A	Preheat ramp up temperature range	25 °C -> 150 °C
B	Preheat ramp up rate	1.5(2.5) °C/s
C	Soak temperature range	150 °C -> 190 °C
D	Soak time	80(110) s
E	Liquidus temperature	217°C
F	Time above liquidus	60(120) s
G	Peak temperature	240(250) °C

	QTI typical SMT reflow profile conditions (for reference only)	
	Step	Reflow condition
H	Cool down temperature rate	4°C/s

The method of measuring the reflow soldering process is as follows.

Fix the thermocouple probe of the temperature measuring line at the connection point between the pin (solderable end) of the packaged device and the pad by using high-temperature solder wire or high-temperature tape, fix the packaged device at the pad by using high-temperature tape or other methods, and cover over the thermocouple probe. See Figure 10 2.

Figure 8-2 Measuring the Reflow Soldering Process



NOTE

To measure the temperature of the QFP-packaged chip, place the temperature probe directly at the pin.

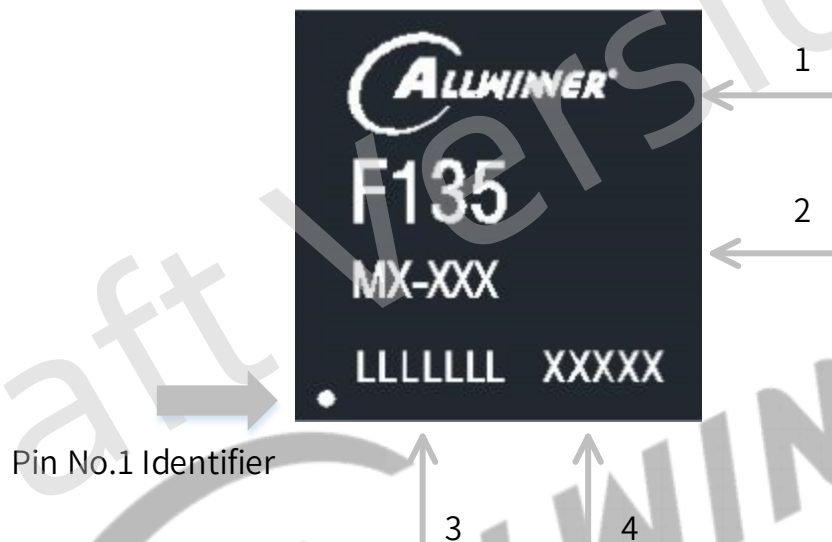
If possible, the more accurate measuring way is to drill the packaged device, or drill the PCB, and fix the thermocouple probe through the drilled hole at the pad.

9 Part Marking

9.1 F135MX-XXX

The following figure shows the F135MX-XXX marking.

Figure 9-1 F135MX-XXX Marking



The following table describes the F135MX-XXX marking definitions.

Table 9-1 F135MX-XXX Marking Definitions

No.	Marking	Description	Fixed/Dynamic
1	ALLWINNER	Allwinner logo or name	Fixed
2	F135MX-XXX	Product name	Fixed
3	LLLLLLL	Lot number	Dynamic
4	XXXXX	Date code	Dynamic

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

This documentation is the original work and copyrighted property of Allwinner Technology Co.,Ltd (Allwinner). No part of this document may be reproduced, modify, publish or transmitted in any form or by any means without prior written consent of Allwinner.

Trademarks and Permissions

Allwinner and the Allwinner logo (incomplete enumeration) are trademarks of Allwinner Technology Co.,Ltd. All other trademarks, trade names, product or service names mentioned in this document are the property of their respective owners.

Important Notice and Disclaimer

The purchased products, services and features are stipulated by the contract made between Allwinner Technology Co.,Ltd (Allwinner) and the customer. All or part of the products, services and features described in this document may not be within the purchase scope or the usage scope. Please read the terms and conditions of the contract and relevant instructions carefully before using, and follow the instructions in this documentation strictly. Allwinner assumes no responsibility for the consequences of improper use (including but not limited to overvoltage, overclock, or excessive temperature).

The information in this document is provided just as a reference or typical applications, and is subject to change without notice. Every effort has been made in the preparation of this document to ensure accuracy of the contents. Allwinner is not responsible for any damage (including but not limited to indirect, incidental or special loss) or any infringement of third party rights arising from the use of this document. All statements, information, and recommendations in this document do not constitute a warranty or commitment of any kind, express or implied.

No license is granted by Allwinner herein express or implied or otherwise to any patent or intellectual property of Allwinner. Third party licences may be required to implement the solution/product. Customers shall be solely responsible to obtain all appropriately required third party licences. Allwinner shall not be liable for any licence fee or royalty due in respect of any required third party licence. Allwinner shall have no warranty, indemnity or other obligations with respect to third party licences.

Draft Version

ALLWINNER

Copyright © 2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Allwinner Technology Co.,Ltd.

No.9 Technology Road 2, High-Tech Zone,
Zhuhai, Guangdong Province, China

Contact US:

Service@allwinnertech.com

www.allwinnertech.com