

MT7981 Reference Manual

Version: 1.2
Release date: 2022-10-14

- ☐ Reference Manual **part 1**
- ☐ Reference Manual **part 2**
- ☒ Reference Manual **part 3**

MediaTek Confidential
For thangtm22@viettel.com.vn Use Only

Document Revision History

Revision	Date	Author/Integrator	Description
1.0	2022-2-15	Yi-Tao.Tsai	Initial Release
1.1	2022-5-24	Yi-Tao.Tsai	Update Part-1: chapter-3 Update Part-2: chapter-4 and chapter-5.3 GPHY Update Part-3: chapter-6 Frame Engine
1.2	2022-5-25	Yi-Tao.Tsai	Update Part-3: chapter-6.4

Table of Contents

Document Revision History.....	3
Table of Contents.....	4
6 Frame Engine.....	6
6.1 Introduction.....	6
6.2 Features.....	6
6.2.1 PSE Features	6
6.2.2 PPE Features	6
6.2.3 ADMA Features.....	7
6.2.4 QDMA Features	7
6.2.5 WDMA Features.....	8
6.2.6 Block Diagram	8
6.3 WiFi / Ethernet Dispatcher (WED).....	9
6.3.1 Indroduction.....	9
6.3.2 Features	10
6.4 Giga bit-Media Access Controller (GMAC).....	10
6.4.1 Introduction.....	10
6.4.2 Features	11
6.4.3 Block Diagram	11
6.4.4 Register Definition.....	12
6.5 Programming Guide	813
6.5.1 ADMA Programming Guide.....	813
6.5.2 QDMA Programming Guide.....	818

Lists of Tables and Figures

No table of figures entries found.

Figure 6-1: Block Diagram of Frame Engine in NETSYS	9
Figure 6-2: Block diagram of GMAC (per port)	12
Figure 6-3: ADMA Tx DMA Descriptor format (TX DMAD)	813
Figure 6-4: ADMA Rx DMA Descriptor format (RX DMAD).....	814
Figure 6-5: DMA descriptor ring	814
Figure 6-6: Operating flow of DMA TX.....	815
Figure 6-7: Operating flow of DMA RX.....	816

Figure 6-8: QDMA Tx descriptor format	819
Figure 6-9: QDMA Rx descriptor format	820
Figure 6-10: QDMA Traffic Shaper Architecture	823

MediaTek Confidential
For thangtm22@viettel.com.vn Use Only

6 Frame Engine

6.1 Introduction

Frame engine is a high-performance network processing engine for network protocol layer 2 to layer 4, provides a DMA interface to transfer Ethernet packets between CPU and GMACs. Frame engine includes ADMA, QDMA, PSE and PPE. It also support Wi-Fi to/from Ethernet hardware offload which is composed of WED/WDMA.

6.2 Features

The main features of these functions are list below.

6.2.1 PSE Features

- Wire-speed (2.5Gbps) Ethernet LAN/WAN NAT/NAPT routing
- Egress rate limiting/shaping
- Flow control for no-packet-loss guarantee
- Emulated multicast support for keep-alive (can mirror a Tx packet to CPU)
- IP/TCP/UDP Checksum offload
- IP/TCP/UDP Checksum Generation
- VLAN & PPPOE header insertion
- TCP Segmentation Offload
- Auto-Padding for sub-64 B packets

6.2.2 PPE Features

- IPv4 NAT/NAPT and IPv6 Routing
- IPv4/IPv6 transition mechanism:
 - Tunneling (DS-Lite, 6RD, MAPE/MAPT)
 - Transition (464XLAT)
- Support 1/2/4/8/16/32 K session/flows

- Virtual server, port-triggering & port forwarding
- All types of IPv4 NAT(NAPT, Twice NAT)
- All types of MAC/VLAN/PPPOE/IP/TCP/UDP binding
- 4 VLAN tagging (Q-in-Q)
- VID Swapping
- Support for 65536 PPPOE sessions
- PPPOE pass-through
- Cone-NAT, port-restricted NAT & Symmetric NAT
- Per flow accounting or rate limiting
- Flow offloading technology for flexible/high performance packet L3/L4 packet processing
- Multi-WAN load balancing with hardware and software cooperation
- QoS for multimedia traffic
- Support NAT/NAPT wire-speed within 128 flows for any packet size

NOTE: All PPE features mentioned above require software porting to function.

6.2.3 ADMA Features

- Supports 4 Tx descriptor rings and 4 Rx descriptor rings
- Scatter/Gather DMA
- Delayed interrupt
- Configurable 4/8/16/32 32-bit word burst length
- Support LRO(Large Receive Offload) with 4 normal RX ring and 4 LRO RX ring
- Support RSS (Receive Side Scaling)
- Support TSO(TCP Segmentation Offload)

6.2.4 QDMA Features

- Supports 1 Tx descriptor link list from software
- Supports directly Tx packet hardware forwarding from PPE
- Supports 1 Rx descriptor rings
- Configurable 4/8/16/32 32-bit word burst length

- Delayed interrupt
- Supports 128 Tx queues
- Per Tx queue forward/drop packet accounting
- Per Tx queue forward byte accounting
- Per Tx queue minimum/maximum rate control
- Strict priority arbitration between 16 Tx queues, for under MIN rate traffic
- Either Strict priority or Weighted Fair Queuing arbitration between 128 Tx queues, for over MIN rate traffic
- 128 Tx queues can be separated into 4 scheduling group
- Supports Random Early Drop with configurable dropping probability
- 8 Tx queues support SFQ and DRR scheduling, with virtual queue capability
- Supports up to 1024 virtual queues, those are shared by 8 Tx queues
- Supports SFQ/DRR hash perturb
- Per virtual queue forward packet/byte and drop packet accounting

6.2.5 WDMA Features

- Support Wi-Fi <-> Ethernet hardware offload with WED

6.2.6 Block Diagram

Frame Engine comprises DMA masters, configuration register bus slave, packet processor and switch element.

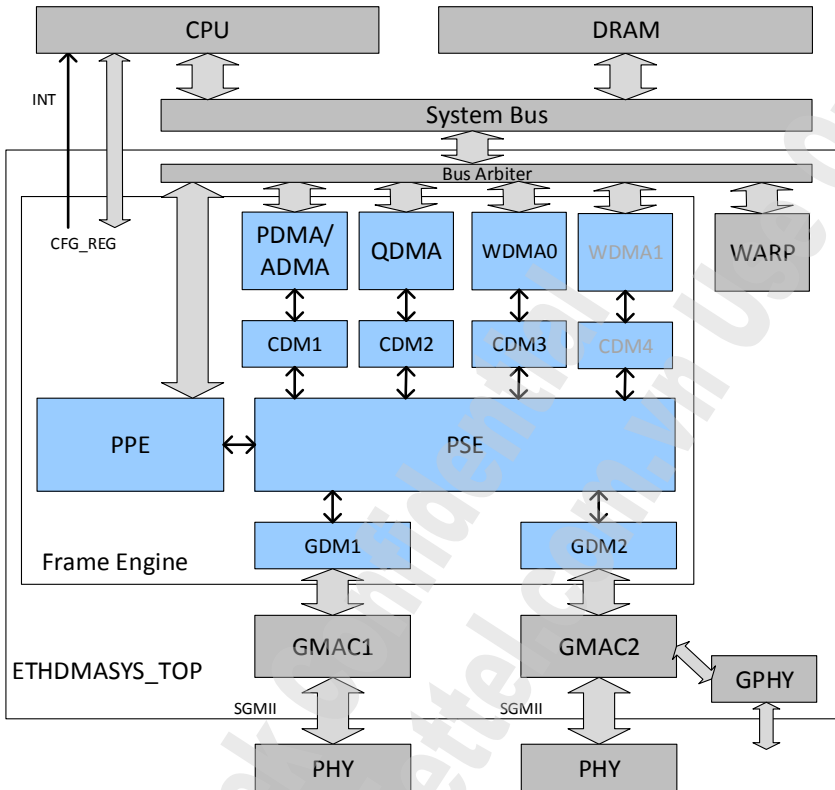


Figure 6-1: Block Diagram of Frame Engine in NETSYS

6.3 WiFi / Ethernet Dispatcher (WED)

6.3.1 Indroduction

WED is WiFi / Ethernet Dispatcher, co-working with Frame Engine to accelerate WiFi traffic. WED forwarding packets from Frame Engine to WiFi, and receiving WiFi packets then dispatching to Frame Engine. Those packets' source/destination are Ethernet, and AP CPU, and routing decision by PPE.

As a bridge between Frame Engine and WiFi DMA, WED parsing/translating DMA descriptor of each other. WED also have buffer management unit, to provide/re-cycle packet buffer for WiFi.

6.3.2 Features

- Support MAC layer functions of IEEE 802.3 and Ethernet
- Support 10/100/1000/2500 Mbps bit rates
- Support Half/Full duplex supported (1000/2500Mbps Half Duplex Mode is not support)
- Support per port SGMII interface
- Automatic 32-bit CRC generation and checking
- Support inter-Frame Gap Shrink (96bits-->64bits)
- Report packet status (good, CRC error, alignment, oversize, undersize, other MIBs information)
- Support flow control and automatic generation of control frames in full duplex mode (IEEE 802.3x)
- Support collision detection and auto retransmission on collisions in half duplex mode (CSMA/CD protocol)
- Support EEE(Energy Efficient Ethernet) capability for full duplex mode (IEEE 802.3az)
- Support packet length up to 15K for jumbo frames application
- 2 port GMAC (port 1 for LAN, port 2 for WAN)
- Support PHY indirect-access by MDIO

6.4 Giga bit-Media Access Controller (GMAC)

6.4.1 Introduction

The MAC sub-layer defines a medium-independent facility, built on the medium-dependent physical facility provided by the Physical Layer, and under the access-layer-independent LAN LLC sub-layer (or other MAC client). It is applicable to a general class of local area broadcast

media suitable for use with the media access discipline known as Carrier Sense Multiple Access with Collision Detection (CSMA/CD).

6.4.2 Features

- Support MAC layer functions of IEEE 802.3 and Ethernet
- Support 10/100/1000/2500 Mbps bit rates
- Support Half/Full duplex supported (1000/2500Mbps Half Duplex Mode is not support)
- Support per port SGMII interface
- Automatic 32-bit CRC generation and checking
- Support inter-Frame Gap Shrink (96bits-->64bits)
- Report packet status (good, CRC error, alignment, oversize, undersize, other MIBs information)
- Support flow control and automatic generation of control frames in full duplex mode (IEEE 802.3x)
- Support collision detection and auto retransmission on collisions in half duplex mode (CSMA/CD protocol)
- Support EEE(Energy Efficient Ethernet) capability for full duplex mode (IEEE 802.3az)
- Support packet length up to 15K for jumbo frames application
- 2 port GMAC (port 1 for LAN, port 2 for WAN)

6.4.3 Block Diagram

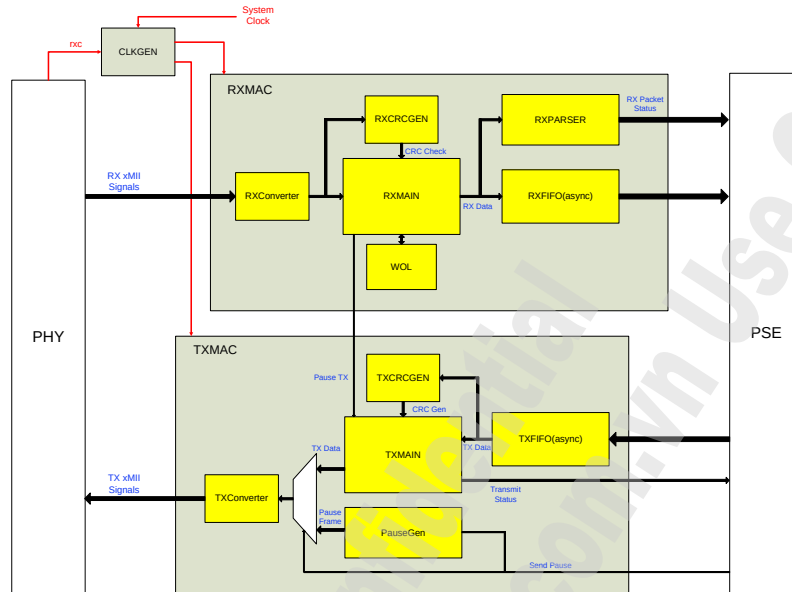


Figure 6-2: Block diagram of GMAC (per port)

6.4.4 Register Definition

Address	Name	Width	Register Function
15000000	CHIPID0 3	32	ID Mode 0~3
15000004	CHIPID4 7	32	ID Mode 4~7
1500000C	REVISION ID	32	ETHSYS Revision Identification
15000010	SYSCFG0	32	System Configuration Register 0
15000014	SYSCFG1	32	System Configuration Register 1
15000018	TESTSTAT0	32	Firmware Test Status 0
1500001C	TESTSTAT1	32	Firmware Test Status 1
15000020	CDM_TXFIFO_CNT	32	CDM TX FIFO Count Status
15000024	BOOT_RELEASE	32	Release CPU's Command to Boot from SRAM
15000028	FE_RST_CHK_IDLE_EN	32	Frame Engine Check IDLE Enable
1500002C	CLKCFG0	32	Clock Configuration Register 0
15000030	CLKCFG1	32	Clock Configuration Register 1
15000034	RSTCTL	32	Reset Control Register
15000038	RSTSTAT	32	Reset Status Register
1500003C	RSTCTL_WARP	32	Reset Control Register
15000040	GPIO0_MODE	32	GPIO0 Purpose Selection
15000044	GPIO1_MODE	32	GPIO1 Purpose Selection
15000048	MEMO0	32	Memory0
1500004C	MEMO1	32	Memory1
15000050	MEMO2	32	Memory2
15000054	MEMO3	32	Memory3
15000058	MEMO4	32	Memory4

1500005C	<u>MEMO5</u>	32	Memory5
15000060	<u>IOC_EN</u>	32	NETSYS IO Coherence Enable Register
15000064	<u>BIST_CTRL</u>	32	NETSYS Global BIST Configuration Register
15000068	<u>BIST_NETSYS2EMI0</u>	32	NETSYS2EMI_M0 BIST Configuration Register 0
1500006C	<u>BIST_NETSYS2EMI1</u>	32	NETSYS2EMI_M0 BIST Configuration Register 1
15000070	<u>BIST_NETSYS2EMI2</u>	32	NETSYS2EMI_M1 BIST Configuration Register 0
15000074	<u>BIST_NETSYS2EMI3</u>	32	NETSYS2EMI_M1 BIST Configuration Register 1
15000078	<u>BIST_NETSYS2INFRA0</u>	32	NETSYS2INFRA BIST Configuration Register 0
1500007C	<u>BIST_NETSYS2INFRA1</u>	32	NETSYS2INFRA BIST Configuration Register 1
15000080	<u>AXICFG0</u>	32	AXI Sideband Configuration Register 0
15000084	<u>AXICFG1</u>	32	AXI Sideband Configuration Register 1
15000088	<u>GALSCFG0</u>	32	GALS Configuration Register 0
1500008C	<u>GALSCFG1</u>	32	GALS Configuration Register 1
15000090	<u>MISTAT</u>	32	NETSYS Bus MI Status Register
15000094	<u>SI0STAT0</u>	32	NETSYS Bus SI Status Register 0
15000098	<u>SI0STAT1</u>	32	NETSYS Bus SI Status Register 1
1500009C	<u>SI0STAT2</u>	32	NETSYS Bus SI Status Register 2
150000A0	<u>S2PSTAT0</u>	32	NETSYS Bus S2P Status Register 0
150000A4	<u>S2PSTAT1</u>	32	NETSYS Bus S2P Status Register 1
150000A8	<u>X2SSTAT0</u>	32	NETSYS Bus X2S Status Register 0
150000AC	<u>X2SSTAT1</u>	32	NETSYS Bus X2S Status Register 1
150000B0	<u>R2XCFG0</u>	32	R2X Configuration Register 0
150000B4	<u>R2XCFG1</u>	32	R2X Configuration Register 1
150000B8	<u>R2XSTAT0</u>	32	R2X Status Register 0
150000BC	<u>R2XSTAT1</u>	32	R2X Status Register 1
150000C0	<u>APBCFG</u>	32	NETSYS_APB Configuration Register
150000C4	<u>APBSTAT</u>	32	NETSYS_APB Status Register
150000CC	<u>NETSYS_DVFS_CFG0</u>	32	NETSYS DVFS Configuration0
150000D0	<u>NETSYS_DVFS_CFG1</u>	32	NETSYS DVFS Configuration1
150000D4	<u>NETSYS_DVFS_CFG2</u>	32	NETSYS DVFS Configuration2
150000D8	<u>NETSYS_DVFS_TH1</u>	32	NETSYS DVFS ThresHold1
150000DC	<u>NETSYS_DVFS_TH2</u>	32	NETSYS DVFS ThresHold2
150000E0	<u>NETSYS_DVFS_TH3</u>	32	NETSYS DVFS ThresHold3
150000E4	<u>NETSYS_LP_CFG0</u>	32	NETSYS Low Power Configuration0
150000E8	<u>NETSYS_LP_CFG1</u>	32	NETSYS Low Power Configuration1
150000EC	<u>NETSYS_IDLE_CFG0</u>	32	NETSYS Low Power Idle Configuration0
150000F0	<u>NETSYS_IDLE_CFG1</u>	32	NETSYS Low Power Idle Configuration1
150000F4	<u>NETSYS_INT_STATUS</u>	32	NETSYS interrupt status
150000F8	<u>NETSYS_INT_ENABLE</u>	32	NETSYS interrupt enable
150000FC	<u>NETSYS_MISC</u>	32	NETSYS MISC
15001000	<u>MBIST_GCTRL</u>	32	MBIST Global Control Register
15001004	<u>MBIST_BKG</u>	32	MBIST Background Control Register
15001008	<u>MBIST_BSEL</u>	32	MBIST bsel Control Register
1500100C	<u>MBIST_MISC</u>	32	MBIST Misc. Control Register
15001010	<u>MBIST_GSTS</u>	32	MBIST Global Status Register
15001020	<u>MBIST_STS_GO</u>	32	MBIST Status Register Group 0

15001024	<u>MBIST_STS_G1</u>	32	MBIST Status Register Group 1
15001028	<u>MBIST_STS_G2</u>	32	MBIST Status Register Group 2
15001040	<u>MBIST_FINISH_G0</u>	32	MBIST Finish Register Group 0
15001044	<u>MBIST_FINISH_G1</u>	32	MBIST Finish Register Group 1
15001048	<u>MBIST_FINISH_G2</u>	32	MBIST Finish Register Group 2
15001060	<u>MBIST_DELSEL_G0</u>	32	MBIST DELSEL Register Group 0
15001064	<u>MBIST_DELSEL_G1</u>	32	MBIST DELSEL Register Group 1
15001068	<u>MBIST_DELSEL_G2</u>	32	MBIST DELSEL Register Group 2
150010F0	<u>RG_SPARE_G0</u>	32	RG Spare Register Group 0
150010F4	<u>RG_SPARE_G1</u>	32	RG Spare Register Group 1
15001100	<u>ETH_MEM_DELSEL_GRP0</u>	32	ETHSYS SRAM DELSEL Group 0
15001104	<u>ETH_MEM_DELSEL_GRP1</u>	32	ETHSYS SRAM DELSEL Group 1
15001108	<u>ETH_MEM_BKG_GRP0</u>	32	ETHSYS SRAM MBIST Background Group 0
1500110C	<u>ETH_MEM_BSEL_GRP0</u>	32	ETHSYS SRAM BSEL Group 0
15001110	<u>WED0_MBIST_GCTRL</u>	32	WED0 MBIST Global Control Register
15001114	<u>WED0_MBIST_GSTS</u>	32	WED0 MBIST Global Status Register
15001118	<u>WED0_MEM_DELSEL</u>	32	WED0 Memory DELSEL
1500111C	<u>WED0_MBIST_BKG</u>	32	WED0 MBIST Background
15001120	<u>WED0_MBIST_BSEL</u>	32	WED0 MBIST BSEL
15001124	<u>WED1_MBIST_GCTRL</u>	32	WED1 MBIST Global Control Register
15001128	<u>WED1_MBIST_GSTS</u>	32	WED1 MBIST Global Status Register
1500112C	<u>WED1_MEM_DELSEL</u>	32	WED1 Memory DELSEL
15001130	<u>WED1_MBIST_BKG</u>	32	WED1 MBIST Background
15001134	<u>WED1_MBIST_BSEL</u>	32	WED1 MBIST BSEL
15001800	<u>TMBIST_DESEL_0</u>	32	MEM_BIST_DESEL_REG_0
15001804	<u>TMBIST_USE_DEFAULT_DESEL_0</u>	32	MRM_BIST_USE_DEFAULT_DESEL_0
15001808	<u>TMBIST_DESEL_1</u>	32	MEM_BIST_DESEL_REG_1
1500180C	<u>TMBIST_USE_DEFAULT_DESEL_1</u>	32	MRM_BIST_USE_DEFAULT_DESEL_1
15001810	<u>TMBIST_DESEL_2</u>	32	MEM_BIST_DESEL_REG_2
15001814	<u>TMBIST_USE_DEFAULT_DESEL_2</u>	32	MRM_BIST_USE_DEFAULT_DESEL_2
15001818	<u>TMBIST_DESEL_3</u>	32	MEM_BIST_DESEL_REG_3
1500181C	<u>TMBIST_USE_DEFAULT_DESEL_3</u>	32	MRM_BIST_USE_DEFAULT_DESEL_3
15001820	<u>TMBIST_DESEL_4</u>	32	MEM_BIST_DESEL_REG_4
15001824	<u>TMBIST_USE_DEFAULT_DESEL_4</u>	32	MRM_BIST_USE_DEFAULT_DESEL_4
15001828	<u>TMBIST_DESEL_5</u>	32	MEM_BIST_DESEL_REG_5
1500182C	<u>TMBIST_USE_DEFAULT_DESEL_5</u>	32	MRM_BIST_USE_DEFAULT_DESEL_5
15001830	<u>TMBIST_DESEL_6</u>	32	MEM_BIST_DESEL_REG_6
15001834	<u>TMBIST_USE_DEFAULT_DESEL_6</u>	32	MRM_BIST_USE_DEFAULT_DESEL_6
15001838	<u>TMBIST_DESEL_7</u>	32	MEM_BIST_DESEL_REG_7

1500183C	<u>TMBIST USE DEFAULT DESEL_7</u>	32	MRM_BIST_USE_DEFAULT_DELSEL_7
15001840	<u>TMBIST DESEL_8</u>	32	MEM_BIST_DESEL_REG_8
15001844	<u>TMBIST USE DEFAULT DESEL_8</u>	32	MRM_BIST_USE_DEFAULT_DELSEL_8
15001848	<u>TMBIST DESEL_9</u>	32	MEM_BIST_DESEL_REG_9
1500184C	<u>TMBIST USE DEFAULT DESEL_9</u>	32	MRM_BIST_USE_DEFAULT_DELSEL_9
15001850	<u>TMBIST DESEL_10</u>	32	MEM_BIST_DESEL_REG_10
15001854	<u>TMBIST USE DEFAULT DESEL_10</u>	32	MRM_BIST_USE_DEFAULT_DELSEL_10
15001858	<u>TMBIST DESEL_11</u>	32	MEM_BIST_DESEL_REG_11
1500185C	<u>TMBIST USE DEFAULT DESEL_11</u>	32	MRM_BIST_USE_DEFAULT_DELSEL_11
15001860	<u>TMBIST DESEL_12</u>	32	MEM_BIST_DESEL_REG_12
15001864	<u>TMBIST USE DEFAULT DESEL_12</u>	32	MRM_BIST_USE_DEFAULT_DELSEL_12
15001868	<u>TMBIST DESEL_13</u>	32	MEM_BIST_DESEL_REG_13
1500186C	<u>TMBIST USE DEFAULT DESEL_13</u>	32	MRM_BIST_USE_DEFAULT_DELSEL_13
15001870	<u>TMBIST DESEL_14</u>	32	MEM_BIST_DESEL_REG_14
15001874	<u>TMBIST USE DEFAULT DESEL_14</u>	32	MRM_BIST_USE_DEFAULT_DELSEL_14
15001878	<u>TMBIST CLK CG_EN</u>	32	MEM_BIST_CLK.CG_EN
15001A00	<u>TMBIST PREFUSE_LOAD</u>	32	MEM_PREFUSE_LOAD_REG
15001A04	<u>TMBIST PREFUSE_SEL</u>	32	MEM_PREFUSE_SEL_REG
15001A08	<u>TMBIST PREFUSE_CONFIG0</u>	32	MEM_PREFUSE_CONFIG0_REG
15001A0C	<u>TMBIST PREFUSE_CONFIG1</u>	32	MEM_PREFUSE_CONFIG1_REG
15001A10	<u>TMBIST PREFUSE_CONFIG2</u>	32	MEM_PREFUSE_CONFIG2_REG
15001A14	<u>TMBIST PREFUSE_CONFIG3</u>	32	MEM_PREFUSE_CONFIG3_REG
15001A18	<u>TMBIST PREFUSE_CONFIG4</u>	32	MEM_PREFUSE_CONFIG4_REG
15001A1C	<u>TMBIST PREFUSE_CONFIG5</u>	32	MEM_PREFUSE_CONFIG5_REG
15001A20	<u>TMBIST PREFUSE_CONFIG6</u>	32	MEM_PREFUSE_CONFIG6_REG
15004000	<u>PMTR MAIN_CTL</u>	32	Main control and total cntnr overflow
15004004	<u>PMTR PRD</u>	32	Sampling period
15004008	<u>PMTR INT</u>	32	Interrupt control
15004010	<u>PMTR DT0_MASTER_ID</u>	32	Request DT0 Master ID selection
15004014	<u>PMTR DT0_MASTER_ID_MASK</u>	32	Request DT0 SRAM Master ID Mask
15004018	<u>PMTR DT1_MASTER_ID</u>	32	Request DT1 Master ID selection
1500401C	<u>PMTR DT1_MASTER_ID_MASK</u>	32	Request DT1 SRAM Master ID Mask
15004080	<u>PMTR 10U_PRD</u>	32	10 us counter limit
15004084	<u>PMTR SW_RST</u>	32	PMTR SW Reset
15004088	<u>PMTR CLK_CON</u>	32	PMTR Clock Control
15004090	<u>PMTR INT_STA</u>	32	Interrupt Status
15004094	<u>PMTR INT_CLR</u>	32	Interrupt Status clear

15004120	<u>PMTR DTO WR CNTR</u>	32	DTO WR REQ NUMBER
15004124	<u>PMTR DTO RD CNTR</u>	32	DTO RD REQ NUMBER
15004128	<u>PMTR DTO WR TOTAL CNTR</u>	32	DTO WR REQ TOTAL NUMBER
1500412C	<u>PMTR DTO RD TOTAL CNTR</u>	32	DTO RD REQ TOTAL NUMBER
15004130	<u>PMTR DTO WDT CNTR</u>	32	DTO WR DATA NUMBER
15004134	<u>PMTR DTO RDT CNTR</u>	32	DTO RD DATA NUMBER
15004138	<u>PMTR DTO WDT TOTAL CNT R</u>	32	DTO WR DATA TOTAL NUMBER
1500413C	<u>PMTR DTO RDT TOTAL CNT R</u>	32	DTO RD DATA TOTAL NUMBER
15004140	<u>PMTR DT1 WR CNTR</u>	32	DT1 WR REQ NUMBER
15004144	<u>PMTR DT1 RD CNTR</u>	32	DT1 RD REQ NUMBER
15004148	<u>PMTR DT1 WR TOTAL CNTR</u>	32	DT1 WR REQ TOTAL NUMBER
1500414C	<u>PMTR DT1 RD TOTAL CNTR</u>	32	DT1 RD REQ TOTAL NUMBER
15004150	<u>PMTR DT1 WDT CNTR</u>	32	DT1 WR DATA NUMBER
15004154	<u>PMTR DT1 RDT CNTR</u>	32	DT1 RD DATA NUMBER
15004158	<u>PMTR DT1 WDT TOTAL CNT R</u>	32	DT1 WR DATA TOTAL NUMBER
1500415C	<u>PMTR DT1 RDT TOTAL CNT R</u>	32	DT1 RD DATA TOTAL NUMBER
15004200	<u>PMTR DLY PRD</u>	32	Delay function counter period
15004204	<u>PMTR PT SLAVE SEL</u>	32	PMTR Pattern Mode Request Target selection
15004208	<u>PMTR PT ADDR BEG</u>	32	PMTR Pattern Mode Request Trigger Begin Address
1500420C	<u>PMTR PT ADDR END</u>	32	PMTR Pattern Mode Request Trigger End Address
15004210	<u>PMTR PT PRD ST</u>	32	PMTR Pattern Mode Sampling period counter status
15004214	<u>PMTR PT 10U PRD ST</u>	32	PMTR Pattern Mode 10 us counter status
15004800	<u>LTCY MAIN CTL</u>	32	LTCY Main control and overflow
15004804	<u>LTCY PRD</u>	32	LTCY Sampling period
15004808	<u>LTCY INT</u>	32	LTCY Interrupt control
15004830	<u>LTCY0 ADDR FILTER BEG</u>	32	LTCY0 Request Target Begin Address selection
15004834	<u>LTCY0 ADDR FILTER END</u>	32	LTCY0 Request Target End Address selection
15004838	<u>LTCY1 ADDR FILTER BEG</u>	32	LTCY1 Request Target Begin Address selection
1500483C	<u>LTCY1 ADDR FILTER END</u>	32	LTCY1 Request Target End Address selection
15004880	<u>LTCY 10U PRD</u>	32	LTCY 10 us counter limit
15004890	<u>LTCY INT STA</u>	32	LTCY Interrupt Status
15004894	<u>LTCY INT CLR</u>	32	LTCY Interrupt Status clear
150048A0	<u>LTCY0 MASTER ID</u>	32	LTCY0 Master ID selection
150048A4	<u>LTCY0 MASTER ID MASK</u>	32	LTCY0 Master ID Mask
150048A8	<u>LTCY1 MASTER ID</u>	32	LTCY1 Master ID selection
150048AC	<u>LTCY1 MASTER ID MASK</u>	32	LTCY1 Master ID Mask
15004900	<u>LTCY0 WR REQ CNTR</u>	32	LTCY0 Write Request Number
15004904	<u>LTCY0 RD REQ CNTR</u>	32	LTCY0 Read Request Number
15004908	<u>LTCY0 MIN WR CYCLE</u>	32	LTCY0 Minimum Write latency cycles
1500490C	<u>LTCY0 MIN RD CYCLE</u>	32	LTCY0 Minimum Read latency cycles
15004910	<u>LTCY0 MAX WR CYCLE</u>	32	LTCY0 Maximum Write latency cycles
15004914	<u>LTCY0 MAX RD CYCLE</u>	32	LTCY0 Maximum Read latency cycles
15004918	<u>LTCY0 MAX OST WR COUNT</u>	32	LTCY0 Maximum OST Write Count

1500491C	<u>LTCY0_MAX_OST_RD_COUNT</u>	32	LTCY0 Maximum OST Read Count
15004920	<u>LTCY1_WR_REQ_CNTR</u>	32	LTCY1 Write Request Number
15004924	<u>LTCY1_RD_REQ_CNTR</u>	32	LTCY1 Read Request Number
15004928	<u>LTCY1_MIN_WR_CYCLE</u>	32	LTCY1 Minimum Write latency cycles
1500492C	<u>LTCY1_MIN_RD_CYCLE</u>	32	LTCY1 Minimum Read latency cycles
15004930	<u>LTCY1_MAX_WR_CYCLE</u>	32	LTCY1 Maximum Write latency cycles
15004934	<u>LTCY1_MAX_RD_CYCLE</u>	32	LTCY1 Maximum Read latency cycles
15004938	<u>LTCY1_MAX_OST_WR_COUNT</u>	32	LTCY1 Maximum OST Write Count
1500493C	<u>LTCY1_MAX_OST_RD_COUNT</u>	32	LTCY1 Maximum OST Read Count
15004A00	<u>LTCY_DLY_PRD</u>	32	LTCY Delay function counter period
15004A04	<u>LTCY_PT_MASTER_SEL</u>	32	LTCY Pattern Mode Master selection
15004A08	<u>LTCY_PT_ADDR_BEG</u>	32	LTCY Pattern Mode Request Trigger Begin Address
15004A0C	<u>LTCY_PT_ADDR_END</u>	32	LTCY Pattern Mode Request Trigger End Address
15004A10	<u>LTCY_PT_PRD_ST</u>	32	LTCY Pattern Mode Sampling period counter status
15004A14	<u>LTCY_PT_10U_PRD_ST</u>	32	LTCY Pattern Mode 10 us counter status
15100000	<u>FE_GLO_CFG</u>	32	Frame Engine Global Configuration
15100004	<u>FE_RST_GLO</u>	32	Frame Engine Global Reset
15100008	<u>FE_INT_STATUS</u>	32	Frame Engine Interrupt Status
1510000C	<u>FE_INT_ENABLE</u>	32	Frame Engine Interrupt Enable
15100010	<u>FE_FOE_TS_T</u>	32	Frame Engine Time Stamp
15100014	<u>FE_IPV6_EXT</u>	32	Frame Engine IPv6 Extension Header
15100018	<u>FE_RATE_COMP</u>	32	Frame Engine Rate Limit Compensation
1510001C	<u>LRO_ALT_REFRESH_TIMER</u>	32	Reserved
15100020	<u>FE_INT_GRP</u>	32	Frame Engine Interrupt Group
15100024	<u>FE_GLO_CFG2</u>	32	Frame Engine Global Configuration part2
15100028	<u>FE_INT_STATUS2</u>	32	Frame Engine Interrupt Status part2
1510002C	<u>FE_INT_ENABLE2</u>	32	Frame Engine Interrupt Enable part2
15100100	<u>PSE_FQFC_CFG1</u>	32	PSE Free Queue Flow Control part1
15100104	<u>PSE_FQFC_CFG2</u>	32	PSE Free Queue Flow Control part2
15100110	<u>PSE_PPE0_DROP</u>	32	PPE0 drop packet enable port
15100114	<u>PSE_PPE1_DROP</u>	32	PPE1 drop packet enable port
15100124	<u>FE_GLO_MISC</u>	32	PSE_PATCH
15100130	<u>FE_GDM_RXID1</u>	32	FE GDM RXID Control 1
15100134	<u>FE_GDM_RXID2</u>	32	FE GDM RXID Control 2
15100138	<u>FE_DBG_CFG</u>	32	FE Debug Configure
15100140	<u>PSE_IQ_REV1</u>	32	PSE Input Queue Reservation part1
15100144	<u>PSE_IQ_REV2</u>	32	PSE Input Queue Reservation part2
15100148	<u>PSE_IQ_REV3</u>	32	PSE Input Queue Reservation part3
1510014C	<u>PSE_IQ_REV4</u>	32	PSE Input Queue Reservation part4
15100150	<u>PSE_IQ_REV5</u>	32	PSE Input Queue Reservation part5
15100154	<u>PSE_IQ_REV6</u>	32	PSE Input Queue Reservation part6
15100158	<u>PSE_IQ_REV7</u>	32	PSE Input Queue Reservation part7
1510015C	<u>PSE_IQ_REV8</u>	32	PSE Input Queue Reservation part8
15100160	<u>PSE_OQ_TH1</u>	32	PSE Output Queue Threshold part1
15100164	<u>PSE_OQ_TH2</u>	32	PSE Output Queue Threshold part2
15100168	<u>PSE_OQ_TH3</u>	32	PSE Output Queue Threshold part3

1510016C	<u>PSE_OQ_TH4</u>	32	PSE Output Queue Threshold part4
15100170	<u>PSE_OQ_TH5</u>	32	PSE Output Queue Threshold part5
15100174	<u>PSE_OQ_TH6</u>	32	PSE Output Queue Threshold part6
15100178	<u>PSE_OQ_TH7</u>	32	PSE Output Queue Threshold part7
1510017C	<u>PSE_OQ_TH8</u>	32	PSE Output Queue Threshold part8
15100180	<u>PSE_IQ_STA1</u>	32	PSE Input Queue Status part1
15100184	<u>PSE_IQ_STA2</u>	32	PSE Input Queue Status part2
15100188	<u>PSE_IQ_STA3</u>	32	PSE Input Queue Status part3
1510018C	<u>PSE_IQ_STA4</u>	32	PSE Input Queue Status part4
15100190	<u>PSE_IQ_STA5</u>	32	PSE Input Queue Status part5
15100194	<u>PSE_IQ_STA6</u>	32	PSE Input Queue Status part6
15100198	<u>PSE_IQ_STA7</u>	32	PSE Input Queue Status part7
1510019C	<u>PSE_IQ_STA8</u>	32	PSE Input Queue Status part8
151001A0	<u>PSE_OQ_STA1</u>	32	PSE Output Queue Status part1
151001A4	<u>PSE_OQ_STA2</u>	32	PSE Output Queue Status part2
151001A8	<u>PSE_OQ_STA3</u>	32	PSE Output Queue Status part3
151001AC	<u>PSE_OQ_STA4</u>	32	PSE Output Queue Status part4
151001B0	<u>PSE_OQ_STA5</u>	32	PSE Output Queue Status part5
151001B4	<u>PSE_OQ_STA6</u>	32	PSE Output Queue Status part6
151001B8	<u>PSE_OQ_STA7</u>	32	PSE Output Queue Status part7
151001BC	<u>PSE_OQ_STA8</u>	32	PSE Output Queue Status part8
151001C0	<u>PSE_TDM_TBL0</u>	32	PSE TDM arbiter table0
151001C4	<u>PSE_TDM_TBL1</u>	32	PSE TDM arbiter table1
151001C8	<u>PSE_TDM_TBL2</u>	32	PSE TDM arbiter table2
151001CC	<u>PSE_TDM_TBL3</u>	32	PSE TDM arbiter table3
151001D0	<u>PSE_TDM_TBL4</u>	32	PSE TDM arbiter table4
151001D4	<u>PSE_TDM_TBL5</u>	32	PSE TDM arbiter table5
151001D8	<u>PSE_TDM_TBL6</u>	32	PSE TDM arbiter table6
151001DC	<u>PSE_TDM_TBL7</u>	32	PSE TDM arbiter table7
151001E0	<u>PSE_SP_CFG0</u>	32	PSE Strict Priority Configure0
151001E4	<u>PSE_SP_CFG1</u>	32	PSE Strict Priority Configure1
151001E8	<u>PSE_TDM_CFG</u>	32	PSE TDM arbiter configure
15100200	<u>FE_CDM1_DBG1</u>	32	FE CDM1 Debug part1
15100204	<u>FE_CDM1_DBG2</u>	32	FE CDM1 Debug part2
15100208	<u>FE_CDM2_DBG1</u>	32	FE CDM2 Debug part1
1510020C	<u>FE_CDM2_DBG2</u>	32	FE CDM2 Debug part2
15100210	<u>FE_GDM1_DBG1</u>	32	FE GDM1 Debug part1
15100214	<u>FE_GDM1_DBG2</u>	32	FE GDM1 Debug part2
15100218	<u>FE_GDM2_DBG1</u>	32	FE GDM2 Debug part1
1510021C	<u>FE_GDM2_DBG2</u>	32	FE GDM2 Debug part2
15100220	<u>FE_CDM1_FSM</u>	32	FE CDM1 FSM status
15100224	<u>FE_CDM2_FSM</u>	32	FE CDM2 FSM status
15100228	<u>FE_GDM1_FSM</u>	32	FE GDM1 FSM status
1510022C	<u>FE_GDM2_FSM</u>	32	FE GDM2 FSM status
15100230	<u>FE_CDM3_DBG1</u>	32	FE CDM3 Debug part1
15100234	<u>FE_CDM3_DBG2</u>	32	FE CDM3 Debug part2

15100238	<u>FE_CDM3_FSM</u>	32	FE CDM3 FSM status
15100240	<u>FE_PSE_FREE</u>	32	PSE Free Page Count
15100244	<u>FE_DROP_FQ</u>	32	FE Packet Drop by Free Queue
15100248	<u>FE_DROP_FC</u>	32	FE Packet Drop by Flow Control
1510024C	<u>FE_DROP_PPE1</u>	32	FE Packet Drop by PPE1
15100250	<u>FE_DROP_PD_6</u>	32	FE Packet Drop by Port 6 Disabled
15100254	<u>FE_DROP_PD_5</u>	32	FE Packet Drop by Port 5 Disabled
15100258	<u>FE_DROP_PD_4</u>	32	FE Packet Drop by Port 4 Disabled
1510025C	<u>FE_DROP_PD_3</u>	32	FE Packet Drop by Port 3 Disabled
15100260	<u>FE_DROP_PD_2</u>	32	FE Packet Drop by Port 2 Disabled
15100264	<u>FE_DROP_PD_1</u>	32	FE Packet Drop by Port 1 Disabled
15100268	<u>FE_DROP_PD_0</u>	32	FE Packet Drop by Port 0 Disabled
15100270	<u>FE_DROP_PD_14</u>	32	FE Packet Drop by Port 14 Disabled
15100274	<u>FE_DROP_PD_13</u>	32	FE Packet Drop by Port 13 Disabled
15100278	<u>FE_DROP_PD_12</u>	32	FE Packet Drop by Port 12 Disabled
1510027C	<u>FE_DROP_PD_11</u>	32	FE Packet Drop by Port 11 Disabled
15100280	<u>FE_DROP_PD_10</u>	32	FE Packet Drop by Port 10 Disabled
15100284	<u>FE_DROP_PD_9</u>	32	FE Packet Drop by Port 9 Disabled
15100288	<u>FE_DROP_PD_8</u>	32	FE Packet Drop by Port 8 Disabled
1510028C	<u>FE_DROP_PD_7</u>	32	FE Packet Drop by Port 7 Disabled
15100290	<u>FE_CDM4_DBG1</u>	32	FE CDM4 Debug part1
15100294	<u>FE_CDM4_DBG2</u>	32	FE CDM4 Debug part2
15100298	<u>FE_CDM4_FSM</u>	32	FE CDM4 FSM status
151002A0	<u>FE_DROP_PPE0</u>	32	FE Packet Drop by PPE0
151002A4	<u>FE_DROP_PPE0_P0_R01</u>	32	FE Packet To Port0 Ring 0&1 Drop by PPE0
151002A8	<u>FE_DROP_PPE0_P0_R23</u>	32	FE Packet To Port0 Ring 2&3 Drop by PPE0
151002AC	<u>FE_DROP_PPE0_P5</u>	32	FE Packet To Port5 Drop by PPE0
151002B0	<u>FE_DROP_PPE0_P8</u>	32	FE Packet To Port8 Drop by PPE0
151002B4	<u>FE_DROP_PPE0_P9</u>	32	FE Packet To Port9 Drop by PPE0
151002B8	<u>FE_DROP_PPE0_P10</u>	32	FE Packet To Port10 Drop by PPE0
151002BC	<u>FE_DROP_PPE0_P11</u>	32	FE Packet To Port11 Drop by PPE0
151002C0	<u>FE_DROP_PPE0_P12</u>	32	FE Packet To Port12 Drop by PPE0
151002C4	<u>FE_DROP_PPE1_P0_R01</u>	32	FE Packet To Port0 Ring 0&1 Drop by PPE1
151002C8	<u>FE_DROP_PPE1_P0_R23</u>	32	FE Packet To Port0 Ring 2&3 Drop by PPE1
151002CC	<u>FE_DROP_PPE1_P5</u>	32	FE Packet To Port5 Drop by PPE1
151002D0	<u>FE_DROP_PPE1_P8</u>	32	FE Packet To Port8 Drop by PPE1
151002D4	<u>FE_DROP_PPE1_P9</u>	32	FE Packet To Port9 Drop by PPE1
151002D8	<u>FE_DROP_PPE1_P10</u>	32	FE Packet To Port10 Drop by PPE1
151002DC	<u>FE_DROP_PPE1_P11</u>	32	FE Packet To Port11 Drop by PPE1
151002E0	<u>FE_DROP_PPE1_P12</u>	32	FE Packet To Port12 Drop by PPE1
15100300	<u>FE_ALT_CF8</u>	32	ALT Entry Base Address
15100304	<u>FE_ALT_SGL_CFC</u>	32	ALT Single DW read
15100308	<u>FE_ALT_SEQ_CFC</u>	32	ALT Sequential DW read
1510030C	<u>FE_ALT_SEQ_CFC_OFS</u>	32	ALT Sequential DW read
15100310	<u>FE_CDM5_DBG1</u>	32	FE CDM5 Debug part1
15100314	<u>FE_CDM5_DBG2</u>	32	FE CDM5 Debug part2

15100318	<u>FE_CDM5_FSM</u>	32	FE CDM5 FSM status
15100320	<u>FE_CDM6_DBG1</u>	32	FE CDM6 Debug part1
15100324	<u>FE_CDM6_DBG2</u>	32	FE CDM6 Debug part2
15100328	<u>FE_CDM6_FSM</u>	32	FE CDM6 FSM status
15100330	<u>FE_CDM7_DBG1</u>	32	FE CDM7 Debug part1
15100334	<u>FE_CDM7_DBG2</u>	32	FE CDM7 Debug part2
15100338	<u>FE_CDM7_FSM</u>	32	FE CDM7 FSM status
15100400	<u>CDMP_IG_CTRL</u>	32	CDM Ingress Control
15100404	<u>CDMP_EG_CTRL</u>	32	CDM Egress Control
15100408	<u>CDMP_PPE_GEN</u>	32	CDM PPPoE Generation
15100500	<u>GDM1_IG_CTRL</u>	32	GDM Ingress Control
15100504	<u>GDM1_EG_CTRL</u>	32	GDM Egress Control
15100508	<u>GDM1_MAC_LSB</u>	32	GDM MY_MAC Address LSB
1510050C	<u>GDM1_MAC_MSB</u>	32	GDM MY_MAC Address MSB
15100510	<u>GDM1_VLAN_GEN</u>	32	GDM VLAN Generation
15100520	<u>GDM1_DOS_CFG_0</u>	32	GDM DOS Configuration 0
15100524	<u>GDM1_DOS_CFG_1</u>	32	GDM DOS Configuration 1
15100528	<u>GDM1_DOS_CFG_2</u>	32	GDM DOS Configuration 2
1510052C	<u>GDM1_DOS_CFG_3</u>	32	GDM DOS Configuration 3
15100C00	<u>PFC_CFG_0</u>	32	PFC GMAC1 Input Priority ReMap 0
15100C04	<u>PFC_CFG_1</u>	32	PFC GMAC1 Input Priority ReMap 1
15100C08	<u>PFC_CFG_2</u>	32	PFC GMAC2 Input Priority ReMap 0
15100C0C	<u>PFC_CFG_3</u>	32	PFC GMAC2 Input Priority ReMap 1
15100C10	<u>PFC_CFG_4</u>	32	PFC WDMA0_1 Input Priority ReMap 0
15100C60	<u>PFC_CFG_5</u>	32	PFC QDMA Input Priority ReMap 0
15100C64	<u>PFC_CFG_6</u>	32	PFC QDMA Input Priority ReMap 1
15100C68	<u>PFC_CFG_7</u>	32	PFC QDMA Input Priority ReMap 2
15100C6C	<u>PFC_CFG_8</u>	32	PFC QDMA Input Priority ReMap 3
15100C70	<u>PFC_CFG_9</u>	32	PFC QDMA Input Priority ReMap 4
15100C74	<u>PFC_CFG_10</u>	32	PFC QDMA Input Priority ReMap 5
15100C78	<u>PFC_CFG_11</u>	32	PFC QDMA Input Priority ReMap 6
15100C7C	<u>PFC_CFG_12</u>	32	PFC QDMA Input Priority ReMap 7
15100C80	<u>PFC_CFG_13</u>	32	PFC QDMA Input Priority ReMap 8
15100C84	<u>PFC_CFG_14</u>	32	PFC QDMA Input Priority ReMap 9
15100C88	<u>PFC_CFG_15</u>	32	PFC QDMA Input Priority ReMap 10
15100C8C	<u>PFC_CFG_16</u>	32	PFC QDMA Input Priority ReMap 11
15100C90	<u>PFC_CFG_17</u>	32	PFC QDMA Input Priority ReMap 12
15100C94	<u>PFC_CFG_18</u>	32	PFC QDMA Input Priority ReMap 13
15100C98	<u>PFC_CFG_19</u>	32	PFC QDMA Input Priority ReMap 14
15100C9C	<u>PFC_CFG_20</u>	32	PFC QDMA Input Priority ReMap 15
15100CA0	<u>PFC_CFG_21</u>	32	PFC QDMA Input Priority ReMap 16
15100CA4	<u>PFC_CFG_22</u>	32	PFC QDMA Input Priority ReMap 17
15100CA8	<u>PFC_CFG_23</u>	32	PFC QDMA Input Priority ReMap 18
15100CAC	<u>PFC_CFG_24</u>	32	PFC QDMA Input Priority ReMap 19
15100CB0	<u>PFC_CFG_25</u>	32	PFC QDMA Input Priority ReMap 20
15100CB4	<u>PFC_CFG_26</u>	32	PFC QDMA Input Priority ReMap 21

15100CB8	PFC_CFG_27	32	PFC QDMA Input Priority ReMap 22
15100CBC	PFC_CFG_28	32	PFC QDMA Input Priority ReMap 23
15100CC0	PFC_CFG_29	32	PFC QDMA Input Priority ReMap 24
15100CC4	PFC_CFG_30	32	PFC QDMA Input Priority ReMap 25
15100CC8	PFC_CFG_31	32	PFC QDMA Input Priority ReMap 26
15100CCC	PFC_CFG_32	32	PFC QDMA Input Priority ReMap 27
15100CD0	PFC_CFG_33	32	PFC QDMA Input Priority ReMap 28
15100CD4	PFC_CFG_34	32	PFC QDMA Input Priority ReMap 29
15100CD8	PFC_CFG_35	32	PFC QDMA Input Priority ReMap 30
15100CDC	PFC_CFG_36	32	PFC QDMA Input Priority ReMap 31
15100D60	PFC_CFG_37	32	PFC GMAC1 Output Priority ReMap 0
15100D64	PFC_CFG_38	32	PFC GMAC1 Output Priority ReMap 1
15100D68	PFC_CFG_39	32	PFC GMAC2 Output Priority ReMap 0
15100D6C	PFC_CFG_40	32	PFC GMAC2 Output Priority ReMap 1
15100D70	PFC_CFG_41	32	PFC WDMA0 Output Priority ReMap 0
15100D74	PFC_CFG_42	32	PFC WDMA1 Output Priority ReMap 0
15100DA0	PFC_CFG_43	32	PFC QDMA Output Priority ReMap 0
15100DA4	PFC_CFG_44	32	PFC QDMA Output Priority ReMap 1
15100DA8	PFC_CFG_45	32	PFC QDMA Output Priority ReMap 2
15100DAC	PFC_CFG_46	32	PFC QDMA Output Priority ReMap 3
15100DB0	PFC_CFG_47	32	PFC QDMA Output Priority ReMap 4
15100DB4	PFC_CFG_48	32	PFC QDMA Output Priority ReMap 5
15100DB8	PFC_CFG_49	32	PFC QDMA Output Priority ReMap 6
15100DBC	PFC_CFG_50	32	PFC QDMA Output Priority ReMap 7
15100DC0	PFC_CFG_51	32	PFC QDMA Output Priority ReMap 8
15100DC4	PFC_CFG_52	32	PFC QDMA Output Priority ReMap 9
15100DC8	PFC_CFG_53	32	PFC QDMA Output Priority ReMap 10
15100DCC	PFC_CFG_54	32	PFC QDMA Output Priority ReMap 11
15100DD0	PFC_CFG_55	32	PFC QDMA Output Priority ReMap 12
15100DD4	PFC_CFG_56	32	PFC QDMA Output Priority ReMap 13
15100DD8	PFC_CFG_57	32	PFC QDMA Output Priority ReMap 14
15100DDC	PFC_CFG_58	32	PFC QDMA Output Priority ReMap 15
15100DE0	PFC_CFG_59	32	PFC QDMA Output Priority ReMap 16
15100DE4	PFC_CFG_60	32	PFC QDMA Output Priority ReMap 17
15100DE8	PFC_CFG_61	32	PFC QDMA Output Priority ReMap 18
15100DEC	PFC_CFG_62	32	PFC QDMA Output Priority ReMap 19
15100DF0	PFC_CFG_63	32	PFC QDMA Output Priority ReMap 20
15100DF4	PFC_CFG_64	32	PFC QDMA Output Priority ReMap 21
15100DF8	PFC_CFG_65	32	PFC QDMA Output Priority ReMap 22
15100DFC	PFC_CFG_66	32	PFC QDMA Output Priority ReMap 23
15100E00	PFC_CFG_67	32	PFC QDMA Output Priority ReMap 24
15100E04	PFC_CFG_68	32	PFC QDMA Output Priority ReMap 25
15100E08	PFC_CFG_69	32	PFC QDMA Output Priority ReMap 26
15100E0C	PFC_CFG_70	32	PFC QDMA Output Priority ReMap 27
15100E10	PFC_CFG_71	32	PFC QDMA Output Priority ReMap 28
15100E14	PFC_CFG_72	32	PFC QDMA Output Priority ReMap 29

15100E18	<u>PFC_CFG_73</u>	32	PFC QDMA Output Priority ReMap 30
15100E1C	<u>PFC_CFG_74</u>	32	PFC QDMA Output Priority ReMap 31
15100EA0	<u>PFC_CFG_75</u>	32	PFC Enable Control to GMAC1
15100EA4	<u>PFC_CFG_76</u>	32	PFC Enable Control to GMAC1
15100EA8	<u>PFC_CFG_77</u>	32	PFC Enable Control to GMAC2
15100EAC	<u>PFC_CFG_78</u>	32	PFC Enable Control to GMAC2
15100EB0	<u>PFC_CFG_79</u>	32	PFC Enable Control to WDMA0
15100EB4	<u>PFC_CFG_80</u>	32	PFC Enable Control to WDMA0
15100EB8	<u>PFC_CFG_81</u>	32	PFC Enable Control to WDMA1
15100EBC	<u>PFC_CFG_82</u>	32	PFC Enable Control to WDMA1
15100EC0	<u>PFC_CFG_83</u>	32	PFC Enable Control to QDMA
15100EF0	<u>PFC_CFG_85</u>	32	PFC Debug 0
15100EF4	<u>PFC_CFG_86</u>	32	PFC Debug 1
15100EF8	<u>PFC_CFG_87</u>	32	PFC Debug 2
15100EFC	<u>PFC_CFG_88</u>	32	PFC Debug 3
15100F00	<u>PFC_CFG_89</u>	32	PFC Debug 4
15100F04	<u>PFC_CFG_90</u>	32	PFC Configuration
15101400	<u>CDMQ_IG_CTRL</u>	32	CDM VLAN Control
15101404	<u>CDMQ_EG_CTRL</u>	32	CDM Egress Control
15101408	<u>CDMQ_PPP_GEN</u>	32	CDM PPPoE Generation
15101500	<u>GDM2_IG_CTRL</u>	32	GDM Ingress Control
15101504	<u>GDM2_EG_CTRL</u>	32	GDM Egress Control
15101508	<u>GDM2_MAC_LSB</u>	32	GDM MY_MAC Address LSB
1510150C	<u>GDM2_MAC_MSB</u>	32	GDM MY_MAC Address MSB
15101510	<u>GDM2_VLAN_GEN</u>	32	GDM VLAN Generation
15101514	<u>GDM2_FILTER_CTRL</u>	32	GDM Filter Control
15101518	<u>GDM2_VIDF01</u>	32	GDM VID Filter Control 01
1510151C	<u>GDM2_VIDF23</u>	32	GDM VID Filter Control 23
15101520	<u>GDM2_DOS_CFG_0</u>	32	GDM DOS Configuration 0
15101524	<u>GDM2_DOS_CFG_1</u>	32	GDM DOS Configuration 1
15101528	<u>GDM2_DOS_CFG_2</u>	32	GDM DOS Configuration 2
1510152C	<u>GDM2_DOS_CFG_3</u>	32	GDM DOS Configuration 3
15101530	<u>GDM2_THRES</u>	32	GDM2 Threshold
15101600	<u>CDMW0_IG_CTRL</u>	32	CDM VLAN Control
15101604	<u>CDMW0_EG_CTRL</u>	32	CDM Egress Control
15101608	<u>CDMW0_PPP_GEN</u>	32	CDM PPPoE Generation
15101610	<u>CDMW1_IG_CTRL</u>	32	CDM VLAN Control
15101614	<u>CDMW1_EG_CTRL</u>	32	CDM Egress Control
15101618	<u>CDMW1_PPP_GEN</u>	32	CDM PPPoE Generation
15101620	<u>CDME0_IG_CTRL</u>	32	CDM VLAN Control
15101624	<u>CDME0_EG_CTRL</u>	32	CDM Egress Control
15101628	<u>CDME0_PPP_GEN</u>	32	CDM PPPoE Generation
15101630	<u>CDME1_IG_CTRL</u>	32	CDM VLAN Control
15101634	<u>CDME1_EG_CTRL</u>	32	CDM Egress Control
15101638	<u>CDME1_PPP_GEN</u>	32	CDM PPPoE Generation
15101640	<u>CDMM_IG_CTRL</u>	32	CDM VLAN Control

15101644	<u>CDMM EG_CTRL</u>	32	CDM Egress Control
15101648	<u>CDMM PPP_GEN</u>	32	CDM PPPoE Generation
1510164C	<u>CDM_THRES0</u>	32	CDM Threshold 0
15101650	<u>CDM_THRES1</u>	32	CDM Threshold 1
15101654	<u>CDM_THRES2</u>	32	CDM Threshold 2
15101658	<u>CDM_THRES3</u>	32	CDM Threshold 3
1510165C	<u>CDM_THRES4</u>	32	CDM Threshold 4
15101660	<u>CDM1_TS_DBG_CNT</u>	32	CDM1 TS Debug Counter
15101664	<u>CDM1_FS_DBG_CNT</u>	32	CDM1 FS Debug Counter
15101668	<u>CDM2_TS_DBG_CNT</u>	32	CDM2 TS Debug Counter
1510166C	<u>CDM2_FS_DBG_CNT</u>	32	CDM2 FS Debug Counter
15101670	<u>CDM3_TS_DBG_CNT</u>	32	CDM3 TS Debug Counter
15101674	<u>CDM3_FS_DBG_CNT</u>	32	CDM3 FS Debug Counter
15101678	<u>CDM4_TS_DBG_CNT</u>	32	CDM4 TS Debug Counter
1510167C	<u>CDM4_FS_DBG_CNT</u>	32	CDM4 FS Debug Counter
15102800	<u>RSS_GLO_CFG</u>	32	RSS Global Configuration
15102804	<u>RSS_GLO_CFG2</u>	32	RSS Global Configuration2
15102808	<u>RSS_REV</u>	32	RSS REV
15102818	<u>RSS_DBG_PROBE</u>	32	RSS DEBUG PROBE
1510281C	<u>RSS_FSM</u>	32	RSS FSM
15102820	<u>RSS_HASH_KEY_DW0</u>	32	RSS hash Key DW0
15102824	<u>RSS_HASH_KEY_DW1</u>	32	RSS hash Key DW1
15102828	<u>RSS_HASH_KEY_DW2</u>	32	RSS hash Key DW2
1510282C	<u>RSS_HASH_KEY_DW3</u>	32	RSS hash Key DW3
15102830	<u>RSS_HASH_KEY_DW4</u>	32	RSS hash Key DW4
15102834	<u>RSS_HASH_KEY_DW5</u>	32	RSS hash Key DW5
15102838	<u>RSS_HASH_KEY_DW6</u>	32	RSS hash Key DW6
1510283C	<u>RSS_HASH_KEY_DW7</u>	32	RSS hash Key DW7
15102840	<u>RSS_HASH_KEY_DW8</u>	32	RSS hash Key DW8
15102844	<u>RSS_HASH_KEY_DW9</u>	32	RSS hash Key DW9
15102848	<u>RSS_LFB_CFG0</u>	32	RSS Low Flow Balance Configuration 0
15102850	<u>RSS_INDR_TABLE_DW0</u>	32	RSS Indirection table DW0
15102854	<u>RSS_INDR_TABLE_DW1</u>	32	RSS Indirection table DW1
15102858	<u>RSS_INDR_TABLE_DW2</u>	32	RSS Indirection table DW2
1510285C	<u>RSS_INDR_TABLE_DW3</u>	32	RSS Indirection table DW3
15102860	<u>RSS_INDR_TABLE_DW4</u>	32	RSS Indirection table DW4
15102864	<u>RSS_INDR_TABLE_DW5</u>	32	RSS Indirection table DW5
15102868	<u>RSS_INDR_TABLE_DW6</u>	32	RSS Indirection table DW6
1510286C	<u>RSS_INDR_TABLE_DW7</u>	32	RSS Indirection table DW7
15104400	<u>QTX_CFG_0</u>	32	TX Queue #0, #(16 * n) Configuration
15104404	<u>QTX_SCH_0</u>	32	TX Queue #0, #(16 * n) Schedule
15104408	<u>QTX_HEAD_0</u>	32	TX Queue #0, #(16 * n) Head Pointer
1510440C	<u>QTX_TAIL_0</u>	32	TX Queue #0, #(16 * n) Tail Pointer
15104410	<u>QTX_CFG_1</u>	32	TX Queue #1, #(16 * n + 1) Configuration
15104414	<u>QTX_SCH_1</u>	32	TX Queue #1, #(16 * n + 1) Schedule
15104418	<u>QTX_HEAD_1</u>	32	TX Queue #1, #(16 * n + 1) Head Pointer

1510441C	<u>QTX_TAIL_1</u>	32	TX Queue #1, $\#(16 * n + 1)$ Tail Pointer
15104420	<u>QTX_CFG_2</u>	32	TX Queue #2, $\#(16 * n + 2)$ Configuration
15104424	<u>QTX_SCH_2</u>	32	TX Queue #2, $\#(16 * n + 2)$ Schedule
15104428	<u>QTX_HEAD_2</u>	32	TX Queue #2, $\#(16 * n + 2)$ Head Pointer
1510442C	<u>QTX_TAIL_2</u>	32	TX Queue #2, $\#(16 * n + 2)$ Tail Pointer
15104430	<u>QTX_CFG_3</u>	32	TX Queue #3, $\#(16 * n + 3)$ Configuration
15104434	<u>QTX_SCH_3</u>	32	TX Queue #3, $\#(16 * n + 3)$ Schedule
15104438	<u>QTX_HEAD_3</u>	32	TX Queue #3, $\#(16 * n + 3)$ Head Pointer
1510443C	<u>QTX_TAIL_3</u>	32	TX Queue #3, $\#(16 * n + 3)$ Tail Pointer
15104440	<u>QTX_CFG_4</u>	32	TX Queue #4, $\#(16 * n + 4)$ Configuration
15104444	<u>QTX_SCH_4</u>	32	TX Queue #4, $\#(16 * n + 4)$ Schedule
15104448	<u>QTX_HEAD_4</u>	32	TX Queue #4, $\#(16 * n + 4)$ Head Pointer
1510444C	<u>QTX_TAIL_4</u>	32	TX Queue #4, $\#(16 * n + 4)$ Tail Pointer
15104450	<u>QTX_CFG_5</u>	32	TX Queue #5, $\#(16 * n + 5)$ Configuration
15104454	<u>QTX_SCH_5</u>	32	TX Queue #5, $\#(16 * n + 5)$ Schedule
15104458	<u>QTX_HEAD_5</u>	32	TX Queue #5, $\#(16 * n + 5)$ Head Pointer
1510445C	<u>QTX_TAIL_5</u>	32	TX Queue #5, $\#(16 * n + 5)$ Tail Pointer
15104460	<u>QTX_CFG_6</u>	32	TX Queue #6, $\#(16 * n + 6)$ Configuration
15104464	<u>QTX_SCH_6</u>	32	TX Queue #6, $\#(16 * n + 6)$ Schedule
15104468	<u>QTX_HEAD_6</u>	32	TX Queue #6, $\#(16 * n + 6)$ Head Pointer
1510446C	<u>QTX_TAIL_6</u>	32	TX Queue #6, $\#(16 * n + 6)$ Tail Pointer
15104470	<u>QTX_CFG_7</u>	32	TX Queue #7, $\#(16 * n + 7)$ Configuration
15104474	<u>QTX_SCH_7</u>	32	TX Queue #7, $\#(16 * n + 7)$ Schedule
15104478	<u>QTX_HEAD_7</u>	32	TX Queue #7, $\#(16 * n + 7)$ Head Pointer
1510447C	<u>QTX_TAIL_7</u>	32	TX Queue #7, $\#(16 * n + 7)$ Tail Pointer
15104480	<u>QTX_CFG_8</u>	32	TX Queue #8, $\#(16 * n + 8)$ Configuration
15104484	<u>QTX_SCH_8</u>	32	TX Queue #8, $\#(16 * n + 8)$ Schedule
15104488	<u>QTX_HEAD_8</u>	32	TX Queue #8, $\#(16 * n + 8)$ Head Pointer
1510448C	<u>QTX_TAIL_8</u>	32	TX Queue #8, $\#(16 * n + 8)$ Tail Pointer
15104490	<u>QTX_CFG_9</u>	32	TX Queue #9, $\#(16 * n + 9)$ Configuration
15104494	<u>QTX_SCH_9</u>	32	TX Queue #9, $\#(16 * n + 9)$ Schedule
15104498	<u>QTX_HEAD_9</u>	32	TX Queue #9, $\#(16 * n + 9)$ Head Pointer
1510449C	<u>QTX_TAIL_9</u>	32	TX Queue #9, $\#(16 * n + 9)$ Tail Pointer
151044A0	<u>QTX_CFG_10</u>	32	TX Queue #10, $\#(16 * n + 10)$ Configuration
151044A4	<u>QTX_SCH_10</u>	32	TX Queue #10, $\#(16 * n + 10)$ Schedule
151044A8	<u>QTX_HEAD_10</u>	32	TX Queue #10, $\#(16 * n + 10)$ Head Pointer
151044AC	<u>QTX_TAIL_10</u>	32	TX Queue #10, $\#(16 * n + 10)$ Tail Pointer
151044B0	<u>QTX_CFG_11</u>	32	TX Queue #11, $\#(16 * n + 11)$ Configuration
151044B4	<u>QTX_SCH_11</u>	32	TX Queue #11, $\#(16 * n + 11)$ Schedule
151044B8	<u>QTX_HEAD_11</u>	32	TX Queue #11, $\#(16 * n + 11)$ Head Pointer
151044BC	<u>QTX_TAIL_11</u>	32	TX Queue #11, $\#(16 * n + 11)$ Tail Pointer
151044C0	<u>QTX_CFG_12</u>	32	TX Queue #12, $\#(16 * n + 12)$ Configuration
151044C4	<u>QTX_SCH_12</u>	32	TX Queue #12, $\#(16 * n + 12)$ Schedule
151044C8	<u>QTX_HEAD_12</u>	32	TX Queue #12, $\#(16 * n + 12)$ Head Pointer
151044CC	<u>QTX_TAIL_12</u>	32	TX Queue #12, $\#(16 * n + 12)$ Tail Pointer
151044D0	<u>QTX_CFG_13</u>	32	TX Queue #13, $\#(16 * n + 13)$ Configuration

151044D4	<u>QTX SCH 13</u>	32	TX Queue #13, #(16 * n + 13) Schedule
151044D8	<u>QTX HEAD 13</u>	32	TX Queue #13, #(16 * n + 13) Head Pointer
151044DC	<u>QTX TAIL 13</u>	32	TX Queue #13, #(16 * n + 13) Tail Pointer
151044E0	<u>QTX CFG 14</u>	32	TX Queue #14, #(16 * n + 14) Configuration
151044E4	<u>QTX SCH 14</u>	32	TX Queue #14, #(16 * n + 14) Schedule
151044E8	<u>QTX HEAD 14</u>	32	TX Queue #14, #(16 * n + 14) Head Pointer
151044EC	<u>QTX TAIL 14</u>	32	TX Queue #14, #(16 * n + 14) Tail Pointer
151044F0	<u>QTX CFG 15</u>	32	TX Queue #15, #(16 * n + 15) Configuration
151044F4	<u>QTX SCH 15</u>	32	TX Queue #15, #(16 * n + 15) Schedule
151044F8	<u>QTX HEAD 15</u>	32	TX Queue #15, #(16 * n + 15) Head Pointer
151044FC	<u>QTX TAIL 15</u>	32	TX Queue #15, #(16 * n + 15) Tail Pointer
15104500	<u>QRX BASE PTR 0</u>	32	RX Ring #0 Base Pointer
15104504	<u>QRX MAX CNT 0</u>	32	RX Ring #0 Maximum Count
15104508	<u>QRX CRX IDX 0</u>	32	RX Ring #0 CPU pointer
1510450C	<u>QRX DRX IDX 0</u>	32	RX Ring #0 DMA pointer
15104510	<u>QRX BASE PTR 1</u>	32	RX Ring #1 Base Pointer
15104514	<u>QRX MAX CNT 1</u>	32	RX Ring #1 Maximum Count
15104518	<u>QRX CRX IDX 1</u>	32	RX Ring #1 CPU pointer
1510451C	<u>QRX DRX IDX 1</u>	32	RX Ring #1 DMA pointer
15104580	<u>VQTX TB BASE 0</u>	32	TX Virtual Queue Table #0 Base Address
15104584	<u>VQTX TB BASE 1</u>	32	TX Virtual Queue Table #1 Base Address
15104588	<u>VQTX TB BASE 2</u>	32	TX Virtual Queue Table #2 Base Address
1510458C	<u>VQTX TB BASE 3</u>	32	TX Virtual Queue Table #3 Base Address
15104590	<u>VQTX TB BASE 4</u>	32	TX Virtual Queue Table #4 Base Address
15104594	<u>VQTX TB BASE 5</u>	32	TX Virtual Queue Table #5 Base Address
15104598	<u>VQTX TB BASE 6</u>	32	TX Virtual Queue Table #6 Base Address
1510459C	<u>VQTX TB BASE 7</u>	32	TX Virtual Queue Table #7 Base Address
151045F0	<u>QDMA PAGE</u>	32	QDMA Configuration Page
15104600	<u>QDMA INFO</u>	32	QDMA Information
15104604	<u>QDMA GLO CFG</u>	32	QDMA Global Configuration
15104608	<u>QDMA RST IDX</u>	32	QDMA Reset Index
1510460C	<u>QDMA DELAY INT</u>	32	Delay Interrupt Configuration
15104610	<u>QDMA FC THRES</u>	32	Flow Control Threshold
15104614	<u>QDMA FC MODE</u>	32	QDMA Flow Control Mode
15104618	<u>QDMA INT STS</u>	32	Interrupt Status
1510461C	<u>QDMA INT MASK</u>	32	Interrupt Mask
15104620	<u>QDMA INT GRP1</u>	32	QDMA Interrupt Group 1 Control
15104624	<u>QDMA INT GRP2</u>	32	QDMA Interrupt Group 2 Control
15104628	<u>QDMA DROP PREC</u>	32	QDMA Drop by FFA Percentage Control
1510462C	<u>QDMA DEBUG</u>	32	Debug Mode
15104630	<u>QDMA TEST</u>	32	Test Mode
15104634	<u>QDMA DMA</u>	32	QDMA DMA FSM
15104638	<u>QDMA BMU</u>	32	QDMA BMU FSM
1510463C	<u>QDMA MON</u>	32	QDMA Monitor for Error Interrupt Event
15104640	<u>QDMA HRED1</u>	32	QDMA HW RED Distribution - I
15104644	<u>QDMA HRED2</u>	32	QDMA HW RED Distribution - II

15104648	<u>QDMA SRED1</u>	32	QDMA SW RED Distribution - I
1510464C	<u>QDMA SRED2</u>	32	QDMA SW RED Distribution - II
15104650	<u>QTX Q0MIN BK</u>	32	QDMA Queue #0 Min. Bucket
15104654	<u>QTX Q1MIN BK</u>	32	QDMA Queue #1 Min. Bucket
15104658	<u>QTX Q2MIN BK</u>	32	QDMA Queue #2 Min. Bucket
1510465C	<u>QTX Q3MIN BK</u>	32	QDMA Queue #3 Min. Bucket
15104660	<u>QTX Q0MAX BK</u>	32	QDMA Queue #0 Max. Bucket
15104664	<u>QTX Q1MAX BK</u>	32	QDMA Queue #1 Max. Bucket
15104668	<u>QTX Q2MAX BK</u>	32	QDMA Queue #2 Max. Bucket
1510466C	<u>QTX Q3MAX BK</u>	32	QDMA Queue #3 Max. Bucket
15104670	<u>QDMA INT STS G0</u>	32	QDMA Interrupt Status Group 0
15104674	<u>QDMA INT STS G1</u>	32	QDMA Interrupt Status Group 1
15104678	<u>QDMA INT STS G2</u>	32	QDMA Interrupt Status Group 2
15104680	<u>VQTX GLO</u>	32	TX Virtual Queue Global Configuration
1510468C	<u>VQTX INVLD PTR</u>	32	TX Virtual Queue Invalid Pointer
15104690	<u>VQTX NUM</u>	32	Number of TX Virtual Queue Configuration
15104698	<u>VQTX SCH</u>	32	TX Virtual Queue Schedule Configuration
151046A0	<u>VQTX HASH CFG</u>	32	TX Virtual Queue Hash Configuration
151046A4	<u>VQTX HASH SD</u>	32	TX Virtual Queue Hash Seed
151046B0	<u>VQTX VLD CFG</u>	32	TX Virtual Queue Valid Configuration
151046BC	<u>QTX MIB IF</u>	32	TX Queue MIB Interface
151046C0	<u>VQTX MIB PCNT</u>	32	TX Virtual Queue MIB Packet Count
151046C4	<u>VQTX MIB BCNTL</u>	32	TX Virtual Queue MIB Byte Count Low Bytes
151046C8	<u>VQTX MIB BCNTH</u>	32	TX Virtual Queue MIB Byte Count High Bytes
151046CC	<u>VQTX MIB DPCNT</u>	32	TX Virtual Queue MIB Drop Packet Count
151046D0	<u>QTX MIB PCNT</u>	32	TX Physical Queue MIB Forward Packet Count
151046D4	<u>QTX MIB DPCNT</u>	32	TX Physical Queue MIB Dropped Packet Count
151046D8	<u>QTX MIB BCNTL</u>	32	TX Physical Queue MIB Byte Count Low Bytes
151046DC	<u>QTX MIB BCNTH</u>	32	TX Physical Queue MIB Byte Count High Bytes
15104700	<u>QTX CTX PTR</u>	32	TX Forward CPU Pointer
15104704	<u>QTX DTX PTR</u>	32	TX Forward DMA Pointer
15104708	<u>QTX FWD CNT</u>	32	TX Forward DMA Counter
15104710	<u>QTX CRX PTR</u>	32	TX Release CPU Pointer
15104714	<u>QTX DRX PTR</u>	32	TX Release DMA Pointer
15104718	<u>QTX RLS CNT</u>	32	TX Release DMA Counter
1510471C	<u>QTX RLS DBASE</u>	32	TX Release Descriptor Base
15104720	<u>QDMA FQ HEAD</u>	32	Free Page Head Pointer
15104724	<u>QDMA FQ TAIL</u>	32	Free Page Tail Pointer
15104728	<u>QDMA FQ CNT</u>	32	Free Page Counter
1510472C	<u>QDMA FQ BLEN</u>	32	Free Page Buffer Length
15104780	<u>QDMA RATE EXP0</u>	32	QDMA Scheduler Rate Exponent 0
15104784	<u>QDMA RATE EXP1</u>	32	QDMA Scheduler Rate Exponent 1
15104788	<u>QDMA RATE EXP2</u>	32	QDMA Scheduler Rate Exponent 2
1510478C	<u>QDMA RATE EXP3</u>	32	QDMA Scheduler Rate Exponent 3
15104790	<u>QDMA RATE EXP4</u>	32	QDMA Scheduler Rate Exponent 4
15104794	<u>QDMA RATE EXP5</u>	32	QDMA Scheduler Rate Exponent 5

15104798	<u>QDMA TX SCH1 SCH2</u>	32	TX Scheduler1 and Scheduler2 Rate Control
1510479C	<u>QDMA TX SCH3 SCH4</u>	32	TX Scheduler3 and Scheduler4 Rate Control
151047A0	<u>VQTX DEP TH 0 3</u>	32	QDMA Virtual Queue Group #0~3 Depth Threshold
151047A4	<u>VQTX DEP TH 4 7</u>	32	QDMA Virtual Queue Group #4~7 Depth Threshold
151047C0	<u>VQTX 0 3 BIND QID</u>	32	QDMA Virtual Queue Group #0~3 to Physical Queue Binding
151047C4	<u>VQTX 4 7 BIND QID</u>	32	QDMA Virtual Queue Group #4~7 to Physical Queue Binding
151047E0	<u>QTX FC SW STS 0 15</u>	32	TX Queue#0~15 Software Path Flow Control Status
151047EC	<u>QDMA ULTRA CFG</u>	32	QDMA AXI ULTRA Configuration
151047F0	<u>QDMA BUS CFG</u>	32	QDMA AXI BUS Configuration
151047F4	<u>QDMA RBUS CFG</u>	32	QDMA RBUS Configuration
151047F8	<u>QDMA RBUS STAT 0</u>	32	R2X Status Register 0
151047FC	<u>QDMA RBUS STAT 1</u>	32	R2X Status Register 1
15104800	<u>WDMA0 TX BASE PTR 0</u>	32	TX Ring #0 Base Pointer
15104804	<u>WDMA0 TX MAX CNT 0</u>	32	TX Ring #0 Maximum Count
15104808	<u>WDMA0 TX CTX IDX 0</u>	32	TX Ring #0 CPU pointer
1510480C	<u>WDMA0 TX DTX IDX 0</u>	32	TX Ring #0 DMA pointer
15104810	<u>WDMA0 TX BASE PTR 1</u>	32	TX Ring #1 Base Pointer
15104814	<u>WDMA0 TX MAX CNT 1</u>	32	TX Ring #1 Maximum Count
15104818	<u>WDMA0 TX CTX IDX 1</u>	32	TX Ring #1 CPU pointer
1510481C	<u>WDMA0 TX DTX IDX 1</u>	32	TX Ring #1 DMA pointer
15104820	<u>WDMA0 TX BASE PTR 2</u>	32	TX Ring #2 Base Pointer
15104824	<u>WDMA0 TX MAX CNT 2</u>	32	TX Ring #2 Maximum Count
15104828	<u>WDMA0 TX CTX IDX 2</u>	32	TX Ring #2 CPU pointer
1510482C	<u>WDMA0 TX DTX IDX 2</u>	32	TX Ring #2 DMA pointer
15104830	<u>WDMA0 TX BASE PTR 3</u>	32	TX Ring #3 Base Pointer
15104834	<u>WDMA0 TX MAX CNT 3</u>	32	TX Ring #3 Maximum Count
15104838	<u>WDMA0 TX CTX IDX 3</u>	32	TX Ring #3 CPU pointer
1510483C	<u>WDMA0 TX DTX IDX 3</u>	32	TX Ring #3 DMA pointer
15104900	<u>WDMA0 RX BASE PTR 0</u>	32	RX Ring #0 Base Pointer
15104904	<u>WDMA0 RX MAX CNT 0</u>	32	RX Ring #0 Maximum Count
15104908	<u>WDMA0 RX CRX IDX 0</u>	32	RX Ring #0 CPU pointer
1510490C	<u>WDMA0 RX DRX IDX 0</u>	32	RX Ring #0 DMA pointer
15104910	<u>WDMA0 RX BASE PTR 1</u>	32	RX Ring #1 Base Pointer
15104914	<u>WDMA0 RX MAX CNT 1</u>	32	RX Ring #1 Maximum Count
15104918	<u>WDMA0 RX CRX IDX 1</u>	32	RX Ring #1 CPU pointer
1510491C	<u>WDMA0 RX DRX IDX 1</u>	32	RX Ring #1 DMA pointer
15104A00	<u>WDMA0 INFO</u>	32	WDMA Information
15104A04	<u>WDMA0 GLO CFG</u>	32	WDMA Global Configuration
15104A08	<u>WDMA0 RST IDX</u>	32	WDMA Reset Index
15104A10	<u>WDMA0 FREEQ THRES</u>	32	WDMA Free Queue Threshold
15104A20	<u>WDMA0 INT STATUS</u>	32	WDMA Interrupt Status
15104A28	<u>WDMA0 INT MASK</u>	32	WDMA Interrupt Mask
15104A30	<u>WDMA0 TX DBG MON0</u>	32	WDMA TX Debug Monitor 0
15104A34	<u>WDMA0 TX DBG MON1</u>	32	WDMA TX Debug Monitor 1
15104A38	<u>WDMA0 RX DBG MON0</u>	32	WDMA RX Debug Monitor 0

15104A3C	<u>WDMA0 RX DBG MON1</u>	32	WDMA RX Debug Monitor 1
15104A40	<u>WDMA0 INT STS GRP0</u>	32	WDMA Interrupt Status Group 0
15104A44	<u>WDMA0 INT STS GRP1</u>	32	WDMA Interrupt Status Group 1
15104A48	<u>WDMA0 INT STS GRP2</u>	32	WDMA Interrupt Status Group 2
15104A4C	<u>WDMA0 INT STS GRP3</u>	32	WDMA Interrupt Status Group 3
15104A50	<u>WDMA0 INT GRP1</u>	32	WDMA Interrupt Group 1 Control
15104A54	<u>WDMA0 INT GRP2</u>	32	WDMA Interrupt Group 2 Control
15104A58	<u>WDMA0 INT GRP3</u>	32	WDMA Interrupt Group 3 Control
15104A60	<u>WDMA0 BUS CFG</u>	32	WDMA AXI BUS Configuration
15104A64	<u>WDMA0 ULTRA CFG</u>	32	WDMA AXI ULTRA Configuration
15104A68	<u>WDMA0 PREF CFG</u>	32	WDMA Prefetch Configuration
15104A70	<u>WDMA0 SDL CFG</u>	32	WDMA SDL Configuration
15104A74	<u>WDMA0 IDLE MASK</u>	32	WDMA IDLE MASK
15104A80	<u>WDMA0 SCH Q01 CFG</u>	32	WDMA Scheduler Configuration for Q0&Q1
15104A84	<u>WDMA0 SCH Q23 CFG</u>	32	WDMA Scheduler Configuration for Q2&Q3
15104A90	<u>WDMA0 INT STATUS 0</u>	32	WDMA Interrupt Status 0
15104A94	<u>WDMA0 INT MASK 0</u>	32	WDMA Interrupt Mask 0
15104A98	<u>WDMA0 INT STATUS 1</u>	32	WDMA Interrupt Status 1
15104A9C	<u>WDMA0 INT MASK 1</u>	32	WDMA Interrupt Mask 1
15104AA0	<u>WDMA0 INT STATUS 2</u>	32	WDMA Interrupt Status 2
15104AA4	<u>WDMA0 INT MASK 2</u>	32	WDMA Interrupt Mask 2
15104AA8	<u>WDMA0 INT STATUS 3</u>	32	WDMA Interrupt Status 3
15104AAC	<u>WDMA0 INT MASK 3</u>	32	WDMA Interrupt Mask 3
15104AB0	<u>WDMA0 TX DELAY INT CFG _0</u>	32	WDMA Tx Delay Interrupt Configuration 0
15104AB4	<u>WDMA0 TX DELAY INT CFG _1</u>	32	WDMA Tx Delay Interrupt Configuration 1
15104AC0	<u>WDMA0 RX DELAY INT CFG _0</u>	32	WDMA Rx Delay Interrupt Configuration 0
15104AC8	<u>WDMA0 RX FC CFG 0</u>	32	WDMA Rx Flow Control Configuration 0
15104ACC	<u>WDMA0 RX FC CFG 1</u>	32	WDMA Rx Flow Control Configuration 1
15104C00	<u>WDMA1 TX BASE PTR 0</u>	32	TX Ring #0 Base Pointer
15104C04	<u>WDMA1 TX MAX CNT 0</u>	32	TX Ring #0 Maximum Count
15104C08	<u>WDMA1 TX CTX IDX 0</u>	32	TX Ring #0 CPU pointer
15104C0C	<u>WDMA1 TX DTX IDX 0</u>	32	TX Ring #0 DMA pointer
15104C10	<u>WDMA1 TX BASE PTR 1</u>	32	TX Ring #1 Base Pointer
15104C14	<u>WDMA1 TX MAX CNT 1</u>	32	TX Ring #1 Maximum Count
15104C18	<u>WDMA1 TX CTX IDX 1</u>	32	TX Ring #1 CPU pointer
15104C1C	<u>WDMA1 TX DTX IDX 1</u>	32	TX Ring #1 DMA pointer
15104C20	<u>WDMA1 TX BASE PTR 2</u>	32	TX Ring #2 Base Pointer
15104C24	<u>WDMA1 TX MAX CNT 2</u>	32	TX Ring #2 Maximum Count
15104C28	<u>WDMA1 TX CTX IDX 2</u>	32	TX Ring #2 CPU pointer
15104C2C	<u>WDMA1 TX DTX IDX 2</u>	32	TX Ring #2 DMA pointer
15104C30	<u>WDMA1 TX BASE PTR 3</u>	32	TX Ring #3 Base Pointer
15104C34	<u>WDMA1 TX MAX CNT 3</u>	32	TX Ring #3 Maximum Count
15104C38	<u>WDMA1 TX CTX IDX 3</u>	32	TX Ring #3 CPU pointer
15104C3C	<u>WDMA1 TX DTX IDX 3</u>	32	TX Ring #3 DMA pointer

15104D00	<u>WDMA1 RX BASE PTR 0</u>	32	RX Ring #0 Base Pointer
15104D04	<u>WDMA1 RX MAX CNT 0</u>	32	RX Ring #0 Maximum Count
15104D08	<u>WDMA1 RX CRX IDX 0</u>	32	RX Ring #0 CPU pointer
15104D0C	<u>WDMA1 RX DRX IDX 0</u>	32	RX Ring #0 DMA pointer
15104D10	<u>WDMA1 RX BASE PTR 1</u>	32	RX Ring #1 Base Pointer
15104D14	<u>WDMA1 RX MAX CNT 1</u>	32	RX Ring #1 Maximum Count
15104D18	<u>WDMA1 RX CRX IDX 1</u>	32	RX Ring #1 CPU pointer
15104D1C	<u>WDMA1 RX DRX IDX 1</u>	32	RX Ring #1 DMA pointer
15104E00	<u>WDMA1 INFO</u>	32	WDMA Information
15104E04	<u>WDMA1 GLO CFG</u>	32	WDMA Global Configuration
15104E08	<u>WDMA1 RST IDX</u>	32	WDMA Reset Index
15104E10	<u>WDMA1 FREEQ THRES</u>	32	WDMA Free Queue Threshold
15104E20	<u>WDMA1 INT STATUS</u>	32	WDMA Interrupt Status
15104E28	<u>WDMA1 INT MASK</u>	32	WDMA Interrupt Mask
15104E30	<u>WDMA1 TX DBG MON0</u>	32	WDMA TX Debug Monitor 0
15104E34	<u>WDMA1 TX DBG MON1</u>	32	WDMA TX Debug Monitor 1
15104E38	<u>WDMA1 RX DBG MON0</u>	32	WDMA RX Debug Monitor 0
15104E3C	<u>WDMA1 RX DBG MON1</u>	32	WDMA RX Debug Monitor 1
15104E40	<u>WDMA1 INT STS GRP0</u>	32	WDMA Interrupt Status Group 0
15104E44	<u>WDMA1 INT STS GRP1</u>	32	WDMA Interrupt Status Group 1
15104E48	<u>WDMA1 INT STS GRP2</u>	32	WDMA Interrupt Status Group 2
15104E4C	<u>WDMA1 INT STS GRP3</u>	32	WDMA Interrupt Status Group 3
15104E50	<u>WDMA1 INT GRP1</u>	32	WDMA Interrupt Group 1 Control
15104E54	<u>WDMA1 INT GRP2</u>	32	WDMA Interrupt Group 2 Control
15104E58	<u>WDMA1 INT GRP3</u>	32	WDMA Interrupt Group 3 Control
15104E60	<u>WDMA1 BUS CFG</u>	32	WDMA AXI BUS Configuration
15104E64	<u>WDMA1 ULTRA CFG</u>	32	WDMA AXI ULTRA Configuration
15104E68	<u>WDMA1 PREF CFG</u>	32	WDMA Prefetch Configuration
15104E70	<u>WDMA1 SDL CFG</u>	32	WDMA SDL Configuration
15104E74	<u>WDMA1 IDLE MASK</u>	32	WDMA IDLE MASK
15104E80	<u>WDMA1 SCH Q01 CFG</u>	32	WDMA Scheduler Configuration for Q0&Q1
15104E84	<u>WDMA1 SCH Q23 CFG</u>	32	WDMA Scheduler Configuration for Q2&Q3
15104E90	<u>WDMA1 INT STATUS 0</u>	32	WDMA Interrupt Status 0
15104E94	<u>WDMA1 INT MASK 0</u>	32	WDMA Interrupt Mask 0
15104E98	<u>WDMA1 INT STATUS 1</u>	32	WDMA Interrupt Status 1
15104E9C	<u>WDMA1 INT MASK 1</u>	32	WDMA Interrupt Mask 1
15104EA0	<u>WDMA1 INT STATUS 2</u>	32	WDMA Interrupt Status 2
15104EA4	<u>WDMA1 INT MASK 2</u>	32	WDMA Interrupt Mask 2
15104EA8	<u>WDMA1 INT STATUS 3</u>	32	WDMA Interrupt Status 3
15104EAC	<u>WDMA1 INT MASK 3</u>	32	WDMA Interrupt Mask 3
15104EB0	<u>WDMA1 TX DELAY INT CFG _0</u>	32	WDMA Tx Delay Interrupt Configuration 0
15104EB4	<u>WDMA1 TX DELAY INT CFG _1</u>	32	WDMA Tx Delay Interrupt Configuration 1
15104EC0	<u>WDMA1 RX DELAY INT CFG _0</u>	32	WDMA Rx Delay Interrupt Configuration 0
15104EC8	<u>WDMA1 RX FC CFG 0</u>	32	WDMA Rx Flow Control Configuration 0

15104ECC	<u>WDMA1 RX FC CFG 1</u>	32	WDMA Rx Flow Control Configuration 1
15106000	<u>ADMA TX BASE PTR 0</u>	32	TX Ring #0 Base Pointer
15106004	<u>ADMA TX MAX CNT 0</u>	32	TX Ring #0 Maximum Count
15106008	<u>ADMA TX CTX IDX 0</u>	32	TX Ring #0 CPU pointer
1510600C	<u>ADMA TX DTX IDX 0</u>	32	TX Ring #0 DMA pointer
15106010	<u>ADMA TX BASE PTR 1</u>	32	TX Ring #1 Base Pointer
15106014	<u>ADMA TX MAX CNT 1</u>	32	TX Ring #1 Maximum Count
15106018	<u>ADMA TX CTX IDX 1</u>	32	TX Ring #1 CPU pointer
1510601C	<u>ADMA TX DTX IDX 1</u>	32	TX Ring #1 DMA pointer
15106020	<u>ADMA TX BASE PTR 2</u>	32	TX Ring #2 Base Pointer
15106024	<u>ADMA TX MAX CNT 2</u>	32	TX Ring #2 Maximum Count
15106028	<u>ADMA TX CTX IDX 2</u>	32	TX Ring #2 CPU pointer
1510602C	<u>ADMA TX DTX IDX 2</u>	32	TX Ring #2 DMA pointer
15106030	<u>ADMA TX BASE PTR 3</u>	32	TX Ring #3 Base Pointer
15106034	<u>ADMA TX MAX CNT 3</u>	32	TX Ring #3 Maximum Count
15106038	<u>ADMA TX CTX IDX 3</u>	32	TX Ring #3 CPU pointer
1510603C	<u>ADMA TX DTX IDX 3</u>	32	TX Ring #3 DMA pointer
15106100	<u>ADMA RX BASE PTR 0</u>	32	RX Ring #0 Base Pointer
15106104	<u>ADMA RX MAX CNT 0</u>	32	RX Ring #0 Maximum Count
15106108	<u>ADMA RX CRX IDX 0</u>	32	RX Ring #0 CPU pointer
1510610C	<u>ADMA RX DRX IDX 0</u>	32	RX Ring #0 DMA pointer
15106110	<u>ADMA RX BASE PTR 1</u>	32	RX Ring #1 Base Pointer
15106114	<u>ADMA RX MAX CNT 1</u>	32	RX Ring #1 Maximum Count
15106118	<u>ADMA RX CRX IDX 1</u>	32	RX Ring #1 CPU pointer
1510611C	<u>ADMA RX DRX IDX 1</u>	32	RX Ring #1 DMA pointer
15106120	<u>ADMA RX BASE PTR 2</u>	32	RX Ring #2 Base Pointer
15106124	<u>ADMA RX MAX CNT 2</u>	32	RX Ring #2 Maximum Count
15106128	<u>ADMA RX CRX IDX 2</u>	32	RX Ring #2 CPU pointer
1510612C	<u>ADMA RX DRX IDX 2</u>	32	RX Ring #2 DMA pointer
15106130	<u>ADMA RX BASE PTR 3</u>	32	RX Ring #3 Base Pointer
15106134	<u>ADMA RX MAX CNT 3</u>	32	RX Ring #3 Maximum Count
15106138	<u>ADMA RX CRX IDX 3</u>	32	RX Ring #3 CPU pointer
1510613C	<u>ADMA RX DRX IDX 3</u>	32	RX Ring #3 DMA pointer
15106140	<u>ADMA RX BASE PTR 4</u>	32	RX Ring #4 Base Pointer
15106144	<u>ADMA RX MAX CNT 4</u>	32	RX Ring #4 Maximum Count
15106148	<u>ADMA RX CRX IDX 4</u>	32	RX Ring #4 CPU pointer
1510614C	<u>ADMA RX DRX IDX 4</u>	32	RX Ring #4 DMA pointer
15106150	<u>ADMA RX BASE PTR 5</u>	32	RX Ring #5 Base Pointer
15106154	<u>ADMA RX MAX CNT 5</u>	32	RX Ring #5 Maximum Count
15106158	<u>ADMA RX CRX IDX 5</u>	32	RX Ring #5 CPU pointer
1510615C	<u>ADMA RX DRX IDX 5</u>	32	RX Ring #5 DMA pointer
15106160	<u>ADMA RX BASE PTR 6</u>	32	RX Ring #6 Base Pointer
15106164	<u>ADMA RX MAX CNT 6</u>	32	RX Ring #6 Maximum Count
15106168	<u>ADMA RX CRX IDX 6</u>	32	RX Ring #6 CPU pointer
1510616C	<u>ADMA RX DRX IDX 6</u>	32	RX Ring #6 DMA pointer
15106170	<u>ADMA RX BASE PTR 7</u>	32	RX Ring #7 Base Pointer

15106174	<u>ADMA RX MAX CNT 7</u>	32	RX Ring #7 Maximum Count
15106178	<u>ADMA RX CRX IDX 7</u>	32	RX Ring #7 CPU pointer
1510617C	<u>ADMA RX DRX IDX 7</u>	32	RX Ring #7 DMA pointer
15106200	<u>ADMA INFO</u>	32	ADMA Information
15106204	<u>ADMA GLO CFG</u>	32	ADMA Global Configuration
15106208	<u>ADMA RST IDX</u>	32	ADMA Reset Index
15106210	<u>ADMA RX CFG</u>	32	ADMA Rx DMA Configuration
15106220	<u>ADMA INT STATUS</u>	32	ADMA Interrupt Status
15106228	<u>ADMA INT MASK</u>	32	ADMA Interrupt Mask
15106230	<u>ADMA TX DBG MON0</u>	32	ADMA TX Debug Monitor 0
15106234	<u>ADMA TX DBG MON1</u>	32	ADMA TX Debug Monitor 1
15106238	<u>ADMA RX DBG MON0</u>	32	ADMA RX Debug Monitor 0
1510623C	<u>ADMA RX DBG MON1</u>	32	ADMA RX Debug Monitor 1
15106240	<u>ADMA INT STS GRP0</u>	32	ADMA Interrupt Status Group 0
15106244	<u>ADMA INT STS GRP1</u>	32	ADMA Interrupt Status Group 1
15106248	<u>ADMA INT STS GRP2</u>	32	ADMA Interrupt Status Group 2
1510624C	<u>ADMA INT STS GRP3</u>	32	ADMA Interrupt Status Group 3
15106250	<u>ADMA INT GRP1</u>	32	ADMA Interrupt Group 1 Control
15106254	<u>ADMA INT GRP2</u>	32	ADMA Interrupt Group 2 Control
15106258	<u>ADMA INT GRP3</u>	32	ADMA Interrupt Group 3 Control
15106260	<u>ADMA BUS CFG</u>	32	ADMA AXI BUS Configuration
15106264	<u>ADMA ULTRA CFG</u>	32	ADMA AXI ULTRA Configuration
15106280	<u>ADMA SCH Q01 CFG</u>	32	ADMA Scheduler Configuration for Q0&Q1
15106284	<u>ADMA SCH Q23 CFG</u>	32	ADMA Scheduler Configuration for Q2&Q3
15106290	<u>ADMA INT STATUS 0</u>	32	ADMA Interrupt Status 0
15106294	<u>ADMA INT MASK 0</u>	32	ADMA Interrupt Mask 0
15106298	<u>ADMA INT STATUS 1</u>	32	ADMA Interrupt Status 1
1510629C	<u>ADMA INT MASK 1</u>	32	ADMA Interrupt Mask 1
151062A0	<u>ADMA INT STATUS 2</u>	32	ADMA Interrupt Status 2
151062A4	<u>ADMA INT MASK 2</u>	32	ADMA Interrupt Mask 2
151062A8	<u>ADMA INT STATUS 3</u>	32	ADMA Interrupt Status 3
151062AC	<u>ADMA INT MASK 3</u>	32	ADMA Interrupt Mask 3
151062B0	<u>ADMA TX DELAY INT CFG 0</u>	32	ADMA Tx Delay Interrupt Configuration 0
151062B4	<u>ADMA TX DELAY INT CFG 1</u>	32	ADMA Tx Delay Interrupt Configuration 1
151062C0	<u>ADMA RX DELAY INT CFG 0</u>	32	ADMA Rx Delay Interrupt Configuration 0
151062C8	<u>ADMA RX FC CFG 0</u>	32	ADMA Rx Flow Control Configuration 0
151062CC	<u>ADMA RX FC CFG 1</u>	32	ADMA Rx Flow Control Configuration 1
15106400	<u>LRO2 ALT TIMER</u>	32	Reserved
15106408	<u>LRO2 CTRL DW0</u>	32	Control CRs
1510640C	<u>LRO2 CTRL DW1</u>	32	Control CRs
15106410	<u>LRO2 CTRL DW2</u>	32	Control CRs
15106414	<u>LRO2 CTRL DW3</u>	32	Control CRs
15106418	<u>LRO2 CTRL DW4</u>	32	Control CRs
1510641C	<u>LRO2 ALT SCORE DELTA</u>	32	
15106420	<u>LRO2 TIMEOUT FLAG</u>	32	
15106430	<u>LRO2 RING1 STS</u>	32	LRO2 Ring1 Status

15106434	<u>LRO2_RING2_STS</u>	32	LRO2 Ring2 Status
15106438	<u>LRO2_RING3_STS</u>	32	LRO2 Ring3 Status
1510643C	<u>LRO2_RING4_STS</u>	32	LRO2 Ring4 Status
15106440	<u>LRO2_ALT_DBG</u>	32	LRO2 ALT debug
15106444	<u>LRO2_ALT_DBG_DATA</u>	32	LRO2 ALT debug data
15106450	<u>LRO2_RING1_STP_DTP_DW</u>	32	Source TCP port number
15106454	<u>LRO2_RING1_DIP_DW0</u>	32	Destination IP address[31:0]
15106458	<u>LRO2_RING1_DIP_DW1</u>	32	Destination IP address[63:32]
1510645C	<u>LRO2_RING1_DIP_DW2</u>	32	Destination IP address[95:64]
15106460	<u>LRO2_RING1_DIP_DW3</u>	32	Destination IP address[127:96]
15106464	<u>LRO2_RING1_SIP_DW0</u>	32	Source IP address[31:0]
15106468	<u>LRO2_RING1_SIP_DW1</u>	32	Source IP address[63:32]
1510646C	<u>LRO2_RING1_SIP_DW2</u>	32	Source IP address[95:64]
15106470	<u>LRO2_RING1_SIP_DW3</u>	32	Source IP address[127:96]
15106474	<u>LRO2_RING1_CTRL_DW0</u>	32	I2_vlan_vid_I2_I
15106478	<u>LRO2_RING1_CTRL_DW1</u>	32	RX ring age time[9:0]
1510647C	<u>LRO2_RING1_CTRL_DW2</u>	32	LRO2_MAX_AGGREGATED_CNT_L
15106480	<u>LRO2_RING1_CTRL_DW3</u>	32	Reserved
15106490	<u>LRO2_RING2_STP_DTP_DW</u>	32	Source TCP port number
15106494	<u>LRO2_RING2_DIP_DW0</u>	32	Destination IP address[31:0]
15106498	<u>LRO2_RING2_DIP_DW1</u>	32	Destination IP address[63:32]
1510649C	<u>LRO2_RING2_DIP_DW2</u>	32	Destination IP address[95:64]
151064A0	<u>LRO2_RING2_DIP_DW3</u>	32	Destination IP address[127:96]
151064A4	<u>LRO2_RING2_SIP_DW0</u>	32	Source IP address[31:0]
151064A8	<u>LRO2_RING2_SIP_DW1</u>	32	Source IP address[63:32]
151064AC	<u>LRO2_RING2_SIP_DW2</u>	32	Source IP address[95:64]
151064B0	<u>LRO2_RING2_SIP_DW3</u>	32	Source IP address[127:96]
151064B4	<u>LRO2_RING2_CTRL_DW0</u>	32	I2_vlan_vid_I2_I
151064B8	<u>LRO2_RING2_CTRL_DW1</u>	32	RX ring age time[9:0]
151064BC	<u>LRO2_RING2_CTRL_DW2</u>	32	LRO2_MAX_AGGREGATED_CNT_L
151064C0	<u>LRO2_RING2_CTRL_DW3</u>	32	Reserved
151064D0	<u>LRO2_RING3_STP_DTP_DW</u>	32	Source TCP port number
151064D4	<u>LRO2_RING3_DIP_DW0</u>	32	Destination IP address[31:0]
151064D8	<u>LRO2_RING3_DIP_DW1</u>	32	Destination IP address[63:32]
151064DC	<u>LRO2_RING3_DIP_DW2</u>	32	Destination IP address[95:64]
151064E0	<u>LRO2_RING3_DIP_DW3</u>	32	Destination IP address[127:96]
151064E4	<u>LRO2_RING3_SIP_DW0</u>	32	Source IP address[31:0]
151064E8	<u>LRO2_RING3_SIP_DW1</u>	32	Source IP address[63:32]
151064EC	<u>LRO2_RING3_SIP_DW2</u>	32	Source IP address[95:64]
151064F0	<u>LRO2_RING3_SIP_DW3</u>	32	Source IP address[127:96]
151064F4	<u>LRO2_RING3_CTRL_DW0</u>	32	I2_vlan_vid_I2_I
151064F8	<u>LRO2_RING3_CTRL_DW1</u>	32	RX ring age time[9:0]
151064FC	<u>LRO2_RING3_CTRL_DW2</u>	32	LRO2_MAX_AGGREGATED_CNT_L
15106500	<u>LRO2_RING3_CTRL_DW3</u>	32	Reserved
15106510	<u>LRO2_RING4_STP_DTP_DW</u>	32	Source TCP port number
15106514	<u>LRO2_RING4_DIP_DW0</u>	32	Destination IP address[31:0]

15106518	<u>LRO2_RING4_DIP_DW1</u>	32	Destination IP address[63:32]
1510651C	<u>LRO2_RING4_DIP_DW2</u>	32	Destination IP address[95:64]
15106520	<u>LRO2_RING4_DIP_DW3</u>	32	Destination IP address[127:96]
15106524	<u>LRO2_RING4_SIP_DW0</u>	32	Source IP address[31:0]
15106528	<u>LRO2_RING4_SIP_DW1</u>	32	Source IP address[63:32]
1510652C	<u>LRO2_RING4_SIP_DW2</u>	32	Source IP address[95:64]
15106530	<u>LRO2_RING4_SIP_DW3</u>	32	Source IP address[127:96]
15106534	<u>LRO2_RING4_CTRL_DW0</u>	32	I2_vlan_vid_I2_I
15106538	<u>LRO2_RING4_CTRL_DW1</u>	32	RX ring age time[9:0]
1510653C	<u>LRO2_RING4_CTRL_DW2</u>	32	LRO2_MAX_AGGREGATED_CNT_L
15106540	<u>LRO2_RING4_CTRL_DW3</u>	32	Reserved
15106800	<u>RSS2_GLO_CFG</u>	32	RSS Global Configuration
15106804	<u>RSS2_GLO_CFG2</u>	32	RSS Global Configuration2
15106808	<u>RSS2_GLO_CFG3</u>	32	RSS Global Configuration3
1510680C	<u>RSS2_LFB_TIMER</u>	32	Low Flow Balance Timer
15106818	<u>RSS2_DBG_PROBE</u>	32	RSS DEBUG PROBE
15106820	<u>RSS2_HASH_KEY_DW0</u>	32	RSS hash Key DW0
15106824	<u>RSS2_HASH_KEY_DW1</u>	32	RSS hash Key DW1
15106828	<u>RSS2_HASH_KEY_DW2</u>	32	RSS hash Key DW2
1510682C	<u>RSS2_HASH_KEY_DW3</u>	32	RSS hash Key DW3
15106830	<u>RSS2_HASH_KEY_DW4</u>	32	RSS hash Key DW4
15106834	<u>RSS2_HASH_KEY_DW5</u>	32	RSS hash Key DW5
15106838	<u>RSS2_HASH_KEY_DW6</u>	32	RSS hash Key DW6
1510683C	<u>RSS2_HASH_KEY_DW7</u>	32	RSS hash Key DW7
15106840	<u>RSS2_HASH_KEY_DW8</u>	32	RSS hash Key DW8
15106844	<u>RSS2_HASH_KEY_DW9</u>	32	RSS hash Key DW9
15106850	<u>RSS2_INDR_TABLE_DW0</u>	32	RSS Indirection table DW0
15106854	<u>RSS2_INDR_TABLE_DW1</u>	32	RSS Indirection table DW1
15106858	<u>RSS2_INDR_TABLE_DW2</u>	32	RSS Indirection table DW2
1510685C	<u>RSS2_INDR_TABLE_DW3</u>	32	RSS Indirection table DW3
15106860	<u>RSS2_INDR_TABLE_DW4</u>	32	RSS Indirection table DW4
15106864	<u>RSS2_INDR_TABLE_DW5</u>	32	RSS Indirection table DW5
15106868	<u>RSS2_INDR_TABLE_DW6</u>	32	RSS Indirection table DW6
1510686C	<u>RSS2_INDR_TABLE_DW7</u>	32	RSS Indirection table DW7
15110000	<u>MAC_PPSC</u>	32	PHY Polling and SMI Master Control
15110004	<u>MAC_PIAC</u>	32	PHY Indirect Access Control
15110008	<u>MAC_GPC</u>	32	GIGA MAC Port Control
1511000C	<u>MAC_MISC</u>	32	MAC MISC register
15110100	<u>MAC_P1_MCR</u>	32	Port 1 MAC Control
15110104	<u>MAC_P1_EEE</u>	32	Port 1 EEE Control
15110108	<u>MAC_P1_SR</u>	32	Port 1 MAC Status
1511010C	<u>MAC_P1_FSM</u>	32	Port 1 FSM
15110110	<u>MAC_P1_WOL</u>	32	Port 1 WOL
15110114	<u>MAC_P1_SGMII</u>	32	Port 1 SGMII
15110118	<u>MAC_P1_PFC_CTRL</u>	32	Port 1 PFC Control
1511011C	<u>MAC_P1_PFC_STS</u>	32	Port 1 PFC Status

15110120	<u>MAC P1 PFC RX PSON CNT</u> <u>L</u>	32	Port 1 RX PFC pause on counter for low priority
15110124	<u>MAC P1 PFC RX PSON CNT</u> <u>H</u>	32	Port 1 RX PFC pause on counter for high priority
15110128	<u>MAC P1 PFC RX PSOFF CNT</u> <u>L</u>	32	Port 1 RX PFC pause off counter for low priority
1511012C	<u>MAC P1 PFC RX PSOFF CNT</u> <u>H</u>	32	Port 1 RX PFC pause off counter for high priority
15110130	<u>MAC P1 PFC TX PSON CNT</u> <u>L</u>	32	Port 1 TX PFC pause on counter for low priority
15110134	<u>MAC P1 PFC TX PSON CNT</u> <u>H</u>	32	Port 1 TX PFC pause on counter for high priority
15110138	<u>MAC P1 PFC TX PSOFF CNT</u> <u>L</u>	32	Port 1 TX PFC pause off counter for low priority
1511013C	<u>MAC P1 PFC TX PSOFF CNT</u> <u>H</u>	32	Port 1 TX PFC pause off counter for high priority
15110200	<u>MAC P2 MCR</u>	32	Port 2 MAC Control
15110204	<u>MAC P2 EEE</u>	32	Port 2 EEE Control
15110208	<u>MAC P2 SR</u>	32	Port 2 MAC Status
1511020C	<u>MAC P2 FSM</u>	32	Port 2 FSM
15110210	<u>MAC P2 WOL</u>	32	Port 2 WOL
15110214	<u>MAC P2 SGMII</u>	32	Port 2 SGMII
15110218	<u>MAC P2 PFC CTRL</u>	32	Port 2 PFC Control
1511021C	<u>MAC P2 PFC STS</u>	32	Port 2 PFC Status
15110220	<u>MAC P2 PFC RX PSON CNT</u> <u>L</u>	32	Port 2 RX PFC pause on counter for low priority
15110224	<u>MAC P2 PFC RX PSON CNT</u> <u>H</u>	32	Port 2 RX PFC pause on counter for high priority
15110228	<u>MAC P2 PFC RX PSOFF CNT</u> <u>L</u>	32	Port 2 RX PFC pause off counter for low priority
1511022C	<u>MAC P2 PFC RX PSOFF CNT</u> <u>H</u>	32	Port 2 RX PFC pause off counter for high priority
15110230	<u>MAC P2 PFC TX PSON CNT</u> <u>L</u>	32	Port 2 TX PFC pause on counter for low priority
15110234	<u>MAC P2 PFC TX PSON CNT</u> <u>H</u>	32	Port 2 TX PFC pause on counter for high priority
15110238	<u>MAC P2 PFC TX PSOFF CNT</u> <u>L</u>	32	Port 2 TX PFC pause off counter for low priority
1511023C	<u>MAC P2 PFC TX PSOFF CNT</u> <u>H</u>	32	Port 2 TX PFC pause off counter for high priority
15110400	<u>GMAC P1 RX UCST PKTCNTL</u>	32	Port 1 RX unicast packet count low word
15110404	<u>GMAC P1 RX UCST PKTCNT</u> <u>H</u>	32	Port 1 RX unicast packet count high word
15110408	<u>GMAC P1 RX UCST BYTECN</u> <u>TL</u>	32	Port 1 RX unicast byte count low word
1511040C	<u>GMAC P1 RX UCST BYTECN</u> <u>TH</u>	32	Port 1 RX unicast byte count high word

15110410	<u>GMAC P1 RX MCST PKTCNT</u> <u>L</u>	32	Port 1 RX multicast packet count low word
15110414	<u>GMAC P1 RX MCST PKTCNT</u> <u>H</u>	32	Port 1 RX multicast packet count high word
15110418	<u>GMAC P1 RX MCST BYTECN</u> <u>TL</u>	32	Port 1 RX multicast byte count low word
1511041C	<u>GMAC P1 RX MCST BYTECN</u> <u>TH</u>	32	Port 1 RX multicast byte count high word
15110420	<u>GMAC P1 RX BCST PKTCNTL</u>	32	Port 1 RX broadcast packet count low word
15110424	<u>GMAC P1 RX BCST PKTCNT</u> <u>H</u>	32	Port 1 RX broadcast packet count high word
15110428	<u>GMAC P1 RX BCST BYTECNT</u> <u>L</u>	32	Port 1 RX broadcast byte count low word
1511042C	<u>GMAC P1 RX BCST BYTECNT</u> <u>H</u>	32	Port 1 RX broadcast byte count high word
15110430	<u>GMAC P1 TX UCST PKTCNTL</u>	32	Port 1 TX unicast packet count low word
15110434	<u>GMAC P1 TX UCST PKTCNT</u> <u>H</u>	32	Port 1 TX unicast packet count high word
15110438	<u>GMAC P1 TX UCST BYTECNT</u> <u>L</u>	32	Port 1 TX unicast byte count low word
1511043C	<u>GMAC P1 TX UCST BYTECNT</u> <u>H</u>	32	Port 1 TX unicast byte count high word
15110440	<u>GMAC P1 TX MCST PKTCNT</u> <u>L</u>	32	Port 1 TX multicast packet count low word
15110444	<u>GMAC P1 TX MCST PKTCNT</u> <u>H</u>	32	Port 1 TX multicast packet count high word
15110448	<u>GMAC P1 TX MCST BYTECN</u> <u>TL</u>	32	Port 1 TX multicast byte count low word
1511044C	<u>GMAC P1 TX MCST BYTECN</u> <u>TH</u>	32	Port 1 TX multicast byte count high word
15110450	<u>GMAC P1 TX BCST PKTCNTL</u>	32	Port 1 TX broadcast packet count low word
15110454	<u>GMAC P1 TX BCST PKTCNT</u> <u>H</u>	32	Port 1 TX broadcast packet count high word
15110458	<u>GMAC P1 TX BCST BYTECNT</u> <u>L</u>	32	Port 1 TX broadcast byte count low word
1511045C	<u>GMAC P1 TX BCST BYTECNT</u> <u>H</u>	32	Port 1 TX broadcast byte count high word
15110460	<u>GMAC P2 RX UCST PKTCNTL</u>	32	Port 2 RX unicast packet count low word
15110464	<u>GMAC P2 RX UCST PKTCNT</u> <u>H</u>	32	Port 2 RX unicast packet count high word
15110468	<u>GMAC P2 RX UCST BYTECN</u> <u>TL</u>	32	Port 2 RX unicast byte count low word
1511046C	<u>GMAC P2 RX UCST BYTECN</u> <u>TH</u>	32	Port 2 RX unicast byte count high word
15110470	<u>GMAC P2 RX MCST PKTCNT</u> <u>L</u>	32	Port 2 RX multicast packet count low word
15110474	<u>GMAC P2 RX MCST PKTCNT</u> <u>H</u>	32	Port 2 RX multicast packet count high word

15110478	<u>GMAC P2 RX MCST BYTECN</u> <u>TL</u>	32	Port 2 RX multicast byte count low word
1511047C	<u>GMAC P2 RX MCST BYTECN</u> <u>TH</u>	32	Port 2 RX multicast byte count high word
15110480	<u>GMAC P2 RX BCST PKTCNTL</u>	32	Port 2 RX broadcast packet count low word
15110484	<u>GMAC P2 RX BCST PKTCNT</u> <u>H</u>	32	Port 2 RX broadcast packet count high word
15110488	<u>GMAC P2 RX BCST BYTECNT</u> <u>L</u>	32	Port 2 RX broadcast byte count low word
1511048C	<u>GMAC P2 RX BCST BYTECNT</u> <u>H</u>	32	Port 2 RX broadcast byte count high word
15110490	<u>GMAC P2 TX UCST PKTCNTL</u>	32	Port 2 TX unicast packet count low word
15110494	<u>GMAC P2 TX UCST PKTCNT</u> <u>H</u>	32	Port 2 TX unicast packet count high word
15110498	<u>GMAC P2 TX UCST BYTECNT</u> <u>L</u>	32	Port 2 TX unicast byte count low word
1511049C	<u>GMAC P2 TX UCST BYTECNT</u> <u>H</u>	32	Port 2 TX unicast byte count high word
151104A0	<u>GMAC P2 TX MCST PKTCNT</u> <u>L</u>	32	Port 2 TX multicast packet count low word
151104A4	<u>GMAC P2 TX MCST PKTCNT</u> <u>H</u>	32	Port 2 TX multicast packet count high word
151104A8	<u>GMAC P2 TX MCST BYTECN</u> <u>TL</u>	32	Port 2 TX multicast byte count low word
151104AC	<u>GMAC P2 TX MCST BYTECN</u> <u>TH</u>	32	Port 2 TX multicast byte count high word
151104B0	<u>GMAC P2 TX BCST PKTCNTL</u>	32	Port 2 TX broadcast packet count low word
151104B4	<u>GMAC P2 TX BCST PKTCNT</u> <u>H</u>	32	Port 2 TX broadcast packet count high word
151104B8	<u>GMAC P2 TX BCST BYTECNT</u> <u>L</u>	32	Port 2 TX broadcast byte count low word
151104BC	<u>GMAC P2 TX BCST BYTECNT</u> <u>H</u>	32	Port 2 TX broadcast byte count high word
151A0000	<u>IRQ_SEL0</u>	32	IRQ Selection 0 Register
151A0004	<u>IRQ_SEL1</u>	32	IRQ Selection 1 Register
151A0008	<u>IRQ_SEL2</u>	32	IRQ Selection 2 Register
151A000C	<u>IRQ_SEL3</u>	32	IRQ Selection 3 Register
151A0010	<u>IRQ_SEL4</u>	32	IRQ Selection 4 Register
151A0014	<u>IRQ_SEL5</u>	32	IRQ Selection 5 Register
151A0018	<u>IRQ_SEL6</u>	32	IRQ Selection 6 Register
151A001C	<u>IRQ_SEL7</u>	32	IRQ Selection 7 Register
151A0020	<u>IRQ_SEL8</u>	32	IRQ Selection 8 Register
151A0024	<u>IRQ_SEL9</u>	32	IRQ Selection 9 Register
151A0028	<u>IRQ_SEL10</u>	32	IRQ Selection 10 Register
151A002C	<u>IRQ_SEL11</u>	32	IRQ Selection 11 Register
151A0030	<u>IRQ_SEL12</u>	32	IRQ Selection 12 Register
151A0034	<u>IRQ_SEL13</u>	32	IRQ Selection 13 Register
151A0038	<u>IRQ_SEL14</u>	32	IRQ Selection 14 Register

151A003C	<u>IRQ_SEL15</u>	32	IRQ Selection 15 Register
151A006C	<u>FIQ_SEL</u>	32	FIQ Selection Register
151A0070	<u>IRQ_MASK</u>	32	IRQ Mask Register
151A0074	<u>IRQ_MASKM</u>	32	IRQ Mask Register Middle
151A0080	<u>IRQ_MASK_CLR</u>	32	IRQ Mask Clear Register
151A0084	<u>IRQ_MASK_CLRM</u>	32	IRQ Mask Clear Register Middle
151A0090	<u>IRQ_MASK_SET</u>	32	IRQ Mask Set Register
151A0094	<u>IRQ_MASK_SETM</u>	32	IRQ Mask Set Register Middle
151A00A0	<u>IRQ_EOI</u>	32	IRQ End of Interrupt Register
151A00A4	<u>IRQ_EOIM</u>	32	IRQ End of Interrupt Register Middle
151A00B0	<u>IRQ_SENS</u>	32	IRQ Sensitive Register
151A00B4	<u>IRQ_SENSM</u>	32	IRQ Sensitive Register Middle
151A00C0	<u>IRQ_SOFT</u>	32	IRQ Software Interrupt Register
151A00C4	<u>IRQ_SOFTM</u>	32	IRQ Software Interrupt Register Middle
151A00D0	<u>FIQ_CON</u>	32	FIQ Control Register
151A00D4	<u>FIQ_EOI</u>	32	FIQ End of Interrupt Register
151A00D8	<u>IRQ_STA2</u>	32	Binary Coded Value of IRQ_STATUS
151A00DC	<u>IRQ_EOI2</u>	32	Binary Coded Value of IRQ_EOI
151A00E0	<u>IRQ_ASTA</u>	32	Binary Value of IRQ Source Status
151A00E4	<u>IRQ_ASTAM</u>	32	Binary Value of IRQ Source Status Middle
151A00F0	<u>IRQ_EEVT</u>	32	Binary Value of EINT Event
151A0100	<u>EINT_STA</u>	32	EINT Status Register
151A0104	<u>EINT_MASK</u>	32	EINT Mask Register
151A0108	<u>EINT_MASK_CLR</u>	32	EINT Mask Clear Register
151A010C	<u>EINT_MASK_SET</u>	32	EINT Mask Set Register
151A0110	<u>EINT_INTACK</u>	32	EINT Interrupt Acknowledge Register
151A0114	<u>EINT_SENS</u>	32	EINT Sensitive Register
151A0118	<u>EINT_SOFT</u>	32	EINT Software Interrupt Register
151A0120	<u>EINT0_CON</u>	32	EINT 0 De-bounce Control Register
151A0130	<u>EINT1_CON</u>	32	EINT 1 De-bounce Control Register
151A0140	<u>EINT2_CON</u>	32	EINT 2 De-bounce Control Register
151A0150	<u>EINT3_CON</u>	32	EINT 3 De-bounce Control Register
151A0160	<u>EINT4_CON</u>	32	EINT 4 De-bounce Control Register
151A0170	<u>EINT5_CON</u>	32	EINT 5 De-bounce Control Register
151A0180	<u>EINT6_CON</u>	32	EINT 6 De-bounce Control Register
151A0190	<u>EINT7_CON</u>	32	EINT 7 De-bounce Control Register
151A01A0	<u>EINT8_CON</u>	32	EINT 8 De-bounce Control Register
151A01B0	<u>EINT9_CON</u>	32	EINT 9 De-bounce Control Register
151A01C0	<u>EINTA_CON</u>	32	EINTA De-bounce Control Register
151A01D0	<u>EINTB_CON</u>	32	EINT B De-bounce Control Register
151A01E0	<u>EINTC_CON</u>	32	EINT C De-bounce Control Register
151A01F0	<u>EINTD_CON</u>	32	EINT D De-bounce Control Register
151A0200	<u>EINTE_CON</u>	32	EINT E De-bounce Control Register
151A0210	<u>EINTF_CON</u>	32	EINT F De-bounce Control Register
151A0220	<u>EINT10_CON</u>	32	EINT 10 De-bounce Control Register
151A0230	<u>EINT11_CON</u>	32	EINT 11 De-bounce Control Register

151A0240	<u>EINT12_CON</u>	32	EINT 12 De-bounce Control Register
151A0250	<u>EINT13_CON</u>	32	EINT 13 De-bounce Control Register
151A0400	<u>IRQ_SRC</u>	32	monitor IRQ source 0~31 for debug
151A0404	<u>IRQ_SRCM</u>	32	monitor IRQ source 32~63 for debug
151A0408	<u>EINT_SRC</u>	32	monitor EINT source for debug
151A1000	<u>GPT_ISR</u>	32	GPT Interrupt Status Register
151A1004	<u>GPT_IER</u>	32	GPT Interrupt Enable Register
151A1010	<u>GPT0_CTRL</u>	32	GPT0 Control Register
151A1014	<u>GPT0_ICNT</u>	32	GPT0 Initial Counter Register
151A1020	<u>GPT1_CTRL</u>	32	GPT1 Control Register
151A1024	<u>GPT1_ICNT</u>	32	GPT1 Initial Counter Register
151A1030	<u>GPT2_CTRL</u>	32	GPT2 Control Register
151A1034	<u>GPT2_CNT</u>	32	GPT2 Counter Register
151A1040	<u>GPT0_CNT</u>	32	GPT0 Counter Register
151A1044	<u>GPT1_CNT</u>	32	GPT1 Counter Register
151A1050	<u>GPT3_CTRL</u>	32	GPT3 Control Register
151A1054	<u>GPT3_INIT</u>	32	GPT3 Initial Value
151A1058	<u>GPT3_CNT</u>	32	GPT3 Counter Register
151A105C	<u>GPT3_EXPIRE</u>	32	GPT3 Expire Value
151A1060	<u>GPT4_CTRL</u>	32	GPT4 Control Register
151A1064	<u>GPT4_INIT</u>	32	GPT4 Initial Value
151A1068	<u>GPT4_CNT</u>	32	GPT4 Counter Register
151A1070	<u>GPT_DBGSEL</u>	32	GPT debug selection register
151A2030	<u>WDT_MODE</u>	32	Watchdog Timer Control Register
151A2034	<u>WDT_TIMEOUT</u>	32	Watchdog Time-Out Interval Register
151A2038	<u>WDT_RESTART</u>	32	Watchdog Timer Restart Register
151A203C	<u>WDT_STA</u>	32	Watchdog Timer Status Register
151A2040	<u>WDT_RST_DT</u>	32	Watchdog Reset Duration Register
151A2044	<u>WDT_SWRST</u>	32	Watchdog Timer Software Reset Register
151A2050	<u>WDT_IRQEN_B</u>	32	Watchdog Timer IRQ Enable Register
151A3000	<u>BT_WR_DATA</u>	32	UART BT TX Write Data Register
151A3004	<u>WF_WR_DATA</u>	32	UART WF TX Write Data Register
151A3008	<u>STA</u>	32	Status Register
151A300C	<u>CTRL1</u>	32	UART Control 1 Register
151A3010	<u>BCDF_BASE0</u>	32	Baud Rate Divider 0
151A3014	<u>ADJUST</u>	32	Baud Rate Adjust
151A7000	<u>HANG_DET_CTL</u>	32	Hang Detection Control
151A7004	<u>HANG_CYC_THRE</u>	32	Hang cycle threshold
151A7008	<u>PC_CHK_BITMAP</u>	32	PC check bitmap
151A700C	<u>IGN_ADDR_CFG</u>	32	Ignored Address Configuration
151A7010	<u>IGN_ADDR_0</u>	32	Igrone Address 0
151A7014	<u>IGN_ADDR_1</u>	32	Igrone Address 1
151A7018	<u>IGN_ADDR_2</u>	32	Igrone Address 2
151A701C	<u>IGN_ADDR_3</u>	32	Igrone Address 3
151A7020	<u>IGN_ADDR_4</u>	32	Igrone Address 4
151A7024	<u>IGN_ADDR_5</u>	32	Igrone Address 5

151A7028	<u>IGN_ADDR_6</u>	32	Igrone Address 6
151A702C	<u>IGN_ADDR_7</u>	32	Igrone Address 7
151A7030	<u>RO_CHK_PC</u>	32	current checked PC
151A7034	<u>RO_CYC_CNT</u>	32	current cycle counter
151A7038	<u>PC_MON_CTL</u>	32	PC monitor control
151A703C	<u>PC_MON_STS</u>	32	PC monitor status
151A7040	<u>MON_PC_CFG0</u>	32	Monitor PC config 0
151A7044	<u>MON_PC_CFG1</u>	32	Monitor PC config 1
151A7048	<u>MON_PC_CFG2</u>	32	Monitor PC config 2
151A704C	<u>MON_PC_CFG3</u>	32	Monitor PC config 3
151A7050	<u>MON_PC_CFG4</u>	32	Monitor PC config 4
151A7054	<u>MON_PC_CFG5</u>	32	Monitor PC config 5
151A7058	<u>MON_PC_CFG6</u>	32	Monitor PC config 6
151A705C	<u>MON_PC_CFG7</u>	32	Monitor PC config 7
151A7060	<u>MON_PC_CFG8</u>	32	Monitor PC config 8
151A7064	<u>MON_PC_CFG9</u>	32	Monitor PC config 9
151A7068	<u>MON_PC_CFG10</u>	32	Monitor PC config 10
151A706C	<u>MON_PC_CFG11</u>	32	Monitor PC config 11
151A7070	<u>MON_PC_CFG12</u>	32	Monitor PC config 12
151A7074	<u>MON_PC_CFG13</u>	32	Monitor PC config 13
151A7078	<u>MON_PC_CFG14</u>	32	Monitor PC config 14
151A707C	<u>MON_PC_CFG15</u>	32	Monitor PC config 15
151A7080	<u>SW_DBG_CTL</u>	32	SW DEBUG CONTROL
151A7090	<u>MCU_DBG_IF_CMD</u>	32	MCU_DBG_IF_CMD
151A7094	<u>MCU_DBG_IF_ARG0</u>	32	MCU_DBG_IF_ARG0
151A7098	<u>MCU_DBG_IF_ARG1</u>	32	MCU_DBG_IF_ARG1
151A709C	<u>MCU_DBG_IF_CTL</u>	32	MCU_DBG_IF_CTL
151A7100	<u>DBG_PC_LOG_CTL</u>	32	DBG_PC_LOG_CTL
151A7104	<u>DBG_PC_LOG_0</u>	32	DBG_PC_LOG_0
151A7108	<u>DBG_PC_LOG_1</u>	32	DBG_PC_LOG_1
151A710C	<u>DBG_PC_LOG_2</u>	32	DBG_PC_LOG_2
151A7110	<u>DBG_PC_LOG_3</u>	32	DBG_PC_LOG_3
151A7114	<u>DBG_PC_LOG_4</u>	32	DBG_PC_LOG_4
151A7118	<u>DBG_PC_LOG_5</u>	32	DBG_PC_LOG_5
151A711C	<u>DBG_PC_LOG_6</u>	32	DBG_PC_LOG_6
151A7120	<u>DBG_PC_LOG_7</u>	32	DBG_PC_LOG_7
151A7124	<u>DBG_PC_LOG_8</u>	32	DBG_PC_LOG_8
151A7128	<u>DBG_PC_LOG_9</u>	32	DBG_PC_LOG_9
151A712C	<u>DBG_PC_LOG_10</u>	32	DBG_PC_LOG_10
151A7130	<u>DBG_PC_LOG_11</u>	32	DBG_PC_LOG_11
151A7134	<u>DBG_PC_LOG_12</u>	32	DBG_PC_LOG_12
151A7138	<u>DBG_PC_LOG_13</u>	32	DBG_PC_LOG_13
151A713C	<u>DBG_PC_LOG_14</u>	32	DBG_PC_LOG_14
151A7140	<u>DBG_PC_LOG_15</u>	32	DBG_PC_LOG_15
151A7144	<u>DBG_PC_LOG_16</u>	32	DBG_PC_LOG_16
151A7148	<u>DBG_PC_LOG_17</u>	32	DBG_PC_LOG_17

151A714C	<u>DBG_PC_LOG_18</u>	32	DBG_PC_LOG_18
151A7150	<u>DBG_PC_LOG_19</u>	32	DBG_PC_LOG_19
151A7154	<u>DBG_PC_LOG_20</u>	32	DBG_PC_LOG_20
151A7158	<u>DBG_PC_LOG_21</u>	32	DBG_PC_LOG_21
151A715C	<u>DBG_PC_LOG_22</u>	32	DBG_PC_LOG_22
151A7160	<u>DBG_PC_LOG_23</u>	32	DBG_PC_LOG_23
151A7164	<u>DBG_PC_LOG_24</u>	32	DBG_PC_LOG_24
151A7168	<u>DBG_PC_LOG_25</u>	32	DBG_PC_LOG_25
151A716C	<u>DBG_PC_LOG_26</u>	32	DBG_PC_LOG_26
151A7170	<u>DBG_PC_LOG_27</u>	32	DBG_PC_LOG_27
151A7174	<u>DBG_PC_LOG_28</u>	32	DBG_PC_LOG_28
151A7178	<u>DBG_PC_LOG_29</u>	32	DBG_PC_LOG_29
151A717C	<u>DBG_PC_LOG_30</u>	32	DBG_PC_LOG_30
151A7180	<u>DBG_PC_LOG_31</u>	32	DBG_PC_LOG_31
151A7200	<u>DBG_GPR_LOG_CTL</u>	32	DBG_GPR_LOG_CTL
151A7204	<u>DBG_GPR_LOG_0</u>	32	DBG_GPR_LOG_0
151A7208	<u>DBG_GPR_LOG_1</u>	32	DBG_GPR_LOG_1
151A720C	<u>DBG_GPR_LOG_2</u>	32	DBG_GPR_LOG_2
151A7210	<u>DBG_GPR_LOG_3</u>	32	DBG_GPR_LOG_3
151A7214	<u>DBG_GPR_LOG_4</u>	32	DBG_GPR_LOG_4
151A7218	<u>DBG_GPR_LOG_5</u>	32	DBG_GPR_LOG_5
151A721C	<u>DBG_GPR_LOG_6</u>	32	DBG_GPR_LOG_6
151A7220	<u>DBG_GPR_LOG_7</u>	32	DBG_GPR_LOG_7
151A7224	<u>DBG_GPR_LOG_8</u>	32	DBG_GPR_LOG_8
151A7228	<u>DBG_GPR_LOG_9</u>	32	DBG_GPR_LOG_9
151A722C	<u>DBG_GPR_LOG_10</u>	32	DBG_GPR_LOG_10
151A7230	<u>DBG_GPR_LOG_11</u>	32	DBG_GPR_LOG_11
151A7234	<u>DBG_GPR_LOG_12</u>	32	DBG_GPR_LOG_12
151A7238	<u>DBG_GPR_LOG_13</u>	32	DBG_GPR_LOG_13
151A723C	<u>DBG_GPR_LOG_14</u>	32	DBG_GPR_LOG_14
151A7240	<u>DBG_GPR_LOG_15</u>	32	DBG_GPR_LOG_15
151A7244	<u>DBG_GPR_LOG_16</u>	32	DBG_GPR_LOG_16
151A7248	<u>DBG_GPR_LOG_17</u>	32	DBG_GPR_LOG_17
151A724C	<u>DBG_GPR_LOG_18</u>	32	DBG_GPR_LOG_18
151A7250	<u>DBG_GPR_LOG_19</u>	32	DBG_GPR_LOG_19
151A7254	<u>DBG_GPR_LOG_20</u>	32	DBG_GPR_LOG_20
151A7258	<u>DBG_GPR_LOG_21</u>	32	DBG_GPR_LOG_21
151A725C	<u>DBG_GPR_LOG_22</u>	32	DBG_GPR_LOG_22
151A7260	<u>DBG_GPR_LOG_23</u>	32	DBG_GPR_LOG_23
151A7264	<u>DBG_GPR_LOG_24</u>	32	DBG_GPR_LOG_24
151A7268	<u>DBG_GPR_LOG_25</u>	32	DBG_GPR_LOG_25
151A726C	<u>DBG_GPR_LOG_26</u>	32	DBG_GPR_LOG_26
151A7270	<u>DBG_GPR_LOG_27</u>	32	DBG_GPR_LOG_27
151A7274	<u>DBG_GPR_LOG_28</u>	32	DBG_GPR_LOG_28
151A7278	<u>DBG_GPR_LOG_29</u>	32	DBG_GPR_LOG_29
151A727C	<u>DBG_GPR_LOG_30</u>	32	DBG_GPR_LOG_30

151A7280	<u>DBG_GPR_LOG_31</u>	32	DBG_GPR_LOG_31
151A8000	<u>IRQ_SEL0</u>	32	IRQ Selection 0 Register
151A8004	<u>IRQ_SEL1</u>	32	IRQ Selection 1 Register
151A8008	<u>IRQ_SEL2</u>	32	IRQ Selection 2 Register
151A800C	<u>IRQ_SEL3</u>	32	IRQ Selection 3 Register
151A8010	<u>IRQ_SEL4</u>	32	IRQ Selection 4 Register
151A8014	<u>IRQ_SEL5</u>	32	IRQ Selection 5 Register
151A8018	<u>IRQ_SEL6</u>	32	IRQ Selection 6 Register
151A801C	<u>IRQ_SEL7</u>	32	IRQ Selection 7 Register
151A8020	<u>IRQ_SEL8</u>	32	IRQ Selection 8 Register
151A8024	<u>IRQ_SEL9</u>	32	IRQ Selection 9 Register
151A8028	<u>IRQ_SEL10</u>	32	IRQ Selection 10 Register
151A802C	<u>IRQ_SEL11</u>	32	IRQ Selection 11 Register
151A8030	<u>IRQ_SEL12</u>	32	IRQ Selection 12 Register
151A8034	<u>IRQ_SEL13</u>	32	IRQ Selection 13 Register
151A8038	<u>IRQ_SEL14</u>	32	IRQ Selection 14 Register
151A803C	<u>IRQ_SEL15</u>	32	IRQ Selection 15 Register
151A806C	<u>FIQ_SEL</u>	32	FIQ Selection Register
151A8070	<u>IRQ_MASK</u>	32	IRQ Mask Register
151A8074	<u>IRQ_MASKM</u>	32	IRQ Mask Register Middle
151A8080	<u>IRQ_MASK_CLR</u>	32	IRQ Mask Clear Register
151A8084	<u>IRQ_MASK_CLRM</u>	32	IRQ Mask Clear Register Middle
151A8090	<u>IRQ_MASK_SET</u>	32	IRQ Mask Set Register
151A8094	<u>IRQ_MASK_SETM</u>	32	IRQ Mask Set Register Middle
151A80A0	<u>IRQ_EOI</u>	32	IRQ End of Interrupt Register
151A80A4	<u>IRQ_EOIM</u>	32	IRQ End of Interrupt Register Middle
151A80B0	<u>IRQ_SENS</u>	32	IRQ Sensitive Register
151A80B4	<u>IRQ_SENSM</u>	32	IRQ Sensitive Register Middle
151A80C0	<u>IRQ_SOFT</u>	32	IRQ Software Interrupt Register
151A80C4	<u>IRQ_SOFTM</u>	32	IRQ Software Interrupt Register Middle
151A80D0	<u>FIQ_CON</u>	32	FIQ Control Register
151A80D4	<u>FIQ_EOI</u>	32	FIQ End of Interrupt Register
151A80D8	<u>IRQ_STA2</u>	32	Binary Coded Value of IRQ_STATUS
151A80DC	<u>IRQ_EOI2</u>	32	Binary Coded Value of IRQ_EOI
151A80E0	<u>IRQ_ASTA</u>	32	Binary Value of IRQ Source Status
151A80E4	<u>IRQ_ASTAM</u>	32	Binary Value of IRQ Source Status Middle
151A80F0	<u>IRQ_EEVT</u>	32	Binary Value of EINT Event
151A8100	<u>EINT_STA</u>	32	EINT Status Register
151A8104	<u>EINT_MASK</u>	32	EINT Mask Register
151A8108	<u>EINT_MASK_CLR</u>	32	EINT Mask Clear Register
151A810C	<u>EINT_MASK_SET</u>	32	EINT Mask Set Register
151A8110	<u>EINT_INTACK</u>	32	EINT Interrupt Acknowledge Register
151A8114	<u>EINT_SENS</u>	32	EINT Sensitive Register
151A8118	<u>EINT_SOFT</u>	32	EINT Software Interrupt Register
151A8120	<u>EINT0_CON</u>	32	EINT 0 De-bounce Control Register
151A8130	<u>EINT1_CON</u>	32	EINT 1 De-bounce Control Register

151A8140	<u>EINT2_CON</u>	32	EINT 2 De-bounce Control Register
151A8150	<u>EINT3_CON</u>	32	EINT 3 De-bounce Control Register
151A8160	<u>EINT4_CON</u>	32	EINT 4 De-bounce Control Register
151A8170	<u>EINT5_CON</u>	32	EINT 5 De-bounce Control Register
151A8180	<u>EINT6_CON</u>	32	EINT 6 De-bounce Control Register
151A8190	<u>EINT7_CON</u>	32	EINT 7 De-bounce Control Register
151A81A0	<u>EINT8_CON</u>	32	EINT 8 De-bounce Control Register
151A81B0	<u>EINT9_CON</u>	32	EINT 9 De-bounce Control Register
151A81C0	<u>EINTA_CON</u>	32	EINTA De-bounce Control Register
151A81D0	<u>EINTB_CON</u>	32	EINT B De-bounce Control Register
151A81E0	<u>EINTC_CON</u>	32	EINT C De-bounce Control Register
151A81F0	<u>EINTD_CON</u>	32	EINT D De-bounce Control Register
151A8200	<u>EINTE_CON</u>	32	EINT E De-bounce Control Register
151A8210	<u>EINTF_CON</u>	32	EINT F De-bounce Control Register
151A8220	<u>EINT10_CON</u>	32	EINT 10 De-bounce Control Register
151A8230	<u>EINT11_CON</u>	32	EINT 11 De-bounce Control Register
151A8240	<u>EINT12_CON</u>	32	EINT 12 De-bounce Control Register
151A8250	<u>EINT13_CON</u>	32	EINT 13 De-bounce Control Register
151A8400	<u>IRQ_SRC</u>	32	monitor IRQ source 0~31 for debug
151A8404	<u>IRQ_SRCM</u>	32	monitor IRQ source 32~63 for debug
151A8408	<u>EINT_SRC</u>	32	monitor EINT source for debug
151A9000	<u>GPT_ISR</u>	32	GPT Interrupt Status Register
151A9004	<u>GPT_IER</u>	32	GPT Interrupt Enable Register
151A9010	<u>GPT0_CTRL</u>	32	GPT0 Control Register
151A9014	<u>GPT0_ICNT</u>	32	GPT0 Initial Counter Register
151A9020	<u>GPT1_CTRL</u>	32	GPT1 Control Register
151A9024	<u>GPT1_ICNT</u>	32	GPT1 Initial Counter Register
151A9030	<u>GPT2_CTRL</u>	32	GPT2 Control Register
151A9034	<u>GPT2_CNT</u>	32	GPT2 Counter Register
151A9040	<u>GPT0_CNT</u>	32	GPT0 Counter Register
151A9044	<u>GPT1_CNT</u>	32	GPT1 Counter Register
151A9050	<u>GPT3_CTRL</u>	32	GPT3 Control Register
151A9054	<u>GPT3_INIT</u>	32	GPT3 Initial Value
151A9058	<u>GPT3_CNT</u>	32	GPT3 Counter Register
151A905C	<u>GPT3_EXPIRE</u>	32	GPT3 Expire Value
151A9060	<u>GPT4_CTRL</u>	32	GPT4 Control Register
151A9064	<u>GPT4_INIT</u>	32	GPT4 Initial Value
151A9068	<u>GPT4_CNT</u>	32	GPT4 Counter Register
151A9070	<u>GPT_DBGSEL</u>	32	GPT debug selection register
151AA030	<u>WDT_MODE</u>	32	Watchdog Timer Control Register
151AA034	<u>WDT_TIMEOUT</u>	32	Watchdog Time-Out Interval Register
151AA038	<u>WDT_RESTART</u>	32	Watchdog Timer Restart Register
151AA03C	<u>WDT_STA</u>	32	Watchdog Timer Status Register
151AA040	<u>WDT_RST_DT</u>	32	Watchdog Reset Duration Register
151AA044	<u>WDT_SWRST</u>	32	Watchdog Timer Software Reset Register
151AA050	<u>WDT_IRQEN_B</u>	32	Watchdog Timer IRQ Enable Register

151AB000	<u>BT_WR_DATA</u>	32	UART BT TX Write Data Register
151AB004	<u>WF_WR_DATA</u>	32	UART WF TX Write Data Register
151AB008	<u>STA</u>	32	Status Register
151AB00C	<u>CTRL1</u>	32	UART Control 1 Register
151AB010	<u>BCDF_BASE0</u>	32	Baud Rate Divider 0
151AB014	<u>ADJUST</u>	32	Baud Rate Adjust
151AF000	<u>HANG_DET_CTL</u>	32	Hang Detection Control
151AF004	<u>HANG_CYC_THRE</u>	32	Hang cycle threshold
151AF008	<u>PC_CHK_BITMAP</u>	32	PC check bitmap
151AF00C	<u>IGN_ADDR_CFG</u>	32	Ignored Address Configuration
151AF010	<u>IGN_ADDR_0</u>	32	Igrone Address 0
151AF014	<u>IGN_ADDR_1</u>	32	Igrone Address 1
151AF018	<u>IGN_ADDR_2</u>	32	Igrone Address 2
151AF01C	<u>IGN_ADDR_3</u>	32	Igrone Address 3
151AF020	<u>IGN_ADDR_4</u>	32	Igrone Address 4
151AF024	<u>IGN_ADDR_5</u>	32	Igrone Address 5
151AF028	<u>IGN_ADDR_6</u>	32	Igrone Address 6
151AF02C	<u>IGN_ADDR_7</u>	32	Igrone Address 7
151AF030	<u>RO_CHK_PC</u>	32	current checked PC
151AF034	<u>RO_CYC_CNT</u>	32	current cycle counter
151AF038	<u>PC_MON_CTL</u>	32	PC monitor control
151AF03C	<u>PC_MON_STS</u>	32	PC monitor status
151AF040	<u>MON_PC_CFG0</u>	32	Monitor PC config 0
151AF044	<u>MON_PC_CFG1</u>	32	Monitor PC config 1
151AF048	<u>MON_PC_CFG2</u>	32	Monitor PC config 2
151AF04C	<u>MON_PC_CFG3</u>	32	Monitor PC config 3
151AF050	<u>MON_PC_CFG4</u>	32	Monitor PC config 4
151AF054	<u>MON_PC_CFG5</u>	32	Monitor PC config 5
151AF058	<u>MON_PC_CFG6</u>	32	Monitor PC config 6
151AF05C	<u>MON_PC_CFG7</u>	32	Monitor PC config 7
151AF060	<u>MON_PC_CFG8</u>	32	Monitor PC config 8
151AF064	<u>MON_PC_CFG9</u>	32	Monitor PC config 9
151AF068	<u>MON_PC_CFG10</u>	32	Monitor PC config 10
151AF06C	<u>MON_PC_CFG11</u>	32	Monitor PC config 11
151AF070	<u>MON_PC_CFG12</u>	32	Monitor PC config 12
151AF074	<u>MON_PC_CFG13</u>	32	Monitor PC config 13
151AF078	<u>MON_PC_CFG14</u>	32	Monitor PC config 14
151AF07C	<u>MON_PC_CFG15</u>	32	Monitor PC config 15
151AF080	<u>SW_DBG_CTL</u>	32	SW DEBUG CONTROL
151AF090	<u>MCU_DBG_IF_CMD</u>	32	MCU_DBG_IF_CMD
151AF094	<u>MCU_DBG_IF_ARG0</u>	32	MCU_DBG_IF_ARG0
151AF098	<u>MCU_DBG_IF_ARG1</u>	32	MCU_DBG_IF_ARG1
151AF09C	<u>MCU_DBG_IF_CTL</u>	32	MCU_DBG_IF_CTL
151AF100	<u>DBG_PC_LOG_CTL</u>	32	DBG_PC_LOG_CTL
151AF104	<u>DBG_PC_LOG_0</u>	32	DBG_PC_LOG_0
151AF108	<u>DBG_PC_LOG_1</u>	32	DBG_PC_LOG_1

151AF10C	<u>DBG_PC_LOG_2</u>	32	DBG_PC_LOG_2
151AF110	<u>DBG_PC_LOG_3</u>	32	DBG_PC_LOG_3
151AF114	<u>DBG_PC_LOG_4</u>	32	DBG_PC_LOG_4
151AF118	<u>DBG_PC_LOG_5</u>	32	DBG_PC_LOG_5
151AF11C	<u>DBG_PC_LOG_6</u>	32	DBG_PC_LOG_6
151AF120	<u>DBG_PC_LOG_7</u>	32	DBG_PC_LOG_7
151AF124	<u>DBG_PC_LOG_8</u>	32	DBG_PC_LOG_8
151AF128	<u>DBG_PC_LOG_9</u>	32	DBG_PC_LOG_9
151AF12C	<u>DBG_PC_LOG_10</u>	32	DBG_PC_LOG_10
151AF130	<u>DBG_PC_LOG_11</u>	32	DBG_PC_LOG_11
151AF134	<u>DBG_PC_LOG_12</u>	32	DBG_PC_LOG_12
151AF138	<u>DBG_PC_LOG_13</u>	32	DBG_PC_LOG_13
151AF13C	<u>DBG_PC_LOG_14</u>	32	DBG_PC_LOG_14
151AF140	<u>DBG_PC_LOG_15</u>	32	DBG_PC_LOG_15
151AF144	<u>DBG_PC_LOG_16</u>	32	DBG_PC_LOG_16
151AF148	<u>DBG_PC_LOG_17</u>	32	DBG_PC_LOG_17
151AF14C	<u>DBG_PC_LOG_18</u>	32	DBG_PC_LOG_18
151AF150	<u>DBG_PC_LOG_19</u>	32	DBG_PC_LOG_19
151AF154	<u>DBG_PC_LOG_20</u>	32	DBG_PC_LOG_20
151AF158	<u>DBG_PC_LOG_21</u>	32	DBG_PC_LOG_21
151AF15C	<u>DBG_PC_LOG_22</u>	32	DBG_PC_LOG_22
151AF160	<u>DBG_PC_LOG_23</u>	32	DBG_PC_LOG_23
151AF164	<u>DBG_PC_LOG_24</u>	32	DBG_PC_LOG_24
151AF168	<u>DBG_PC_LOG_25</u>	32	DBG_PC_LOG_25
151AF16C	<u>DBG_PC_LOG_26</u>	32	DBG_PC_LOG_26
151AF170	<u>DBG_PC_LOG_27</u>	32	DBG_PC_LOG_27
151AF174	<u>DBG_PC_LOG_28</u>	32	DBG_PC_LOG_28
151AF178	<u>DBG_PC_LOG_29</u>	32	DBG_PC_LOG_29
151AF17C	<u>DBG_PC_LOG_30</u>	32	DBG_PC_LOG_30
151AF180	<u>DBG_PC_LOG_31</u>	32	DBG_PC_LOG_31
151AF200	<u>DBG_GPR_LOG_CTL</u>	32	DBG_GPR_LOG_CTL
151AF204	<u>DBG_GPR_LOG_0</u>	32	DBG_GPR_LOG_0
151AF208	<u>DBG_GPR_LOG_1</u>	32	DBG_GPR_LOG_1
151AF20C	<u>DBG_GPR_LOG_2</u>	32	DBG_GPR_LOG_2
151AF210	<u>DBG_GPR_LOG_3</u>	32	DBG_GPR_LOG_3
151AF214	<u>DBG_GPR_LOG_4</u>	32	DBG_GPR_LOG_4
151AF218	<u>DBG_GPR_LOG_5</u>	32	DBG_GPR_LOG_5
151AF21C	<u>DBG_GPR_LOG_6</u>	32	DBG_GPR_LOG_6
151AF220	<u>DBG_GPR_LOG_7</u>	32	DBG_GPR_LOG_7
151AF224	<u>DBG_GPR_LOG_8</u>	32	DBG_GPR_LOG_8
151AF228	<u>DBG_GPR_LOG_9</u>	32	DBG_GPR_LOG_9
151AF22C	<u>DBG_GPR_LOG_10</u>	32	DBG_GPR_LOG_10
151AF230	<u>DBG_GPR_LOG_11</u>	32	DBG_GPR_LOG_11
151AF234	<u>DBG_GPR_LOG_12</u>	32	DBG_GPR_LOG_12
151AF238	<u>DBG_GPR_LOG_13</u>	32	DBG_GPR_LOG_13
151AF23C	<u>DBG_GPR_LOG_14</u>	32	DBG_GPR_LOG_14

151AF240	DBG GPR LOG 15	32	DBG_GPR_LOG_15
151AF244	DBG GPR LOG 16	32	DBG_GPR_LOG_16
151AF248	DBG GPR LOG 17	32	DBG_GPR_LOG_17
151AF24C	DBG GPR LOG 18	32	DBG_GPR_LOG_18
151AF250	DBG GPR LOG 19	32	DBG_GPR_LOG_19
151AF254	DBG GPR LOG 20	32	DBG_GPR_LOG_20
151AF258	DBG GPR LOG 21	32	DBG_GPR_LOG_21
151AF25C	DBG GPR LOG 22	32	DBG_GPR_LOG_22
151AF260	DBG GPR LOG 23	32	DBG_GPR_LOG_23
151AF264	DBG GPR LOG 24	32	DBG_GPR_LOG_24
151AF268	DBG GPR LOG 25	32	DBG_GPR_LOG_25
151AF26C	DBG GPR LOG 26	32	DBG_GPR_LOG_26
151AF270	DBG GPR LOG 27	32	DBG_GPR_LOG_27
151AF274	DBG GPR LOG 28	32	DBG_GPR_LOG_28
151AF278	DBG GPR LOG 29	32	DBG_GPR_LOG_29
151AF27C	DBG GPR LOG 30	32	DBG_GPR_LOG_30
151AF280	DBG GPR LOG 31	32	DBG_GPR_LOG_31

15000000 CHIPID0_3 ID Mode 0~3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

15000004 CHIPID4_7 ID Mode 4~7 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

1500000C REVISION_ID ETHSYS Revision Identification 22000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ETHSYS_VER															
Type	RO															
Reset	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ETHSYS_VER								ETHSYS_ECO_ID							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:8	ETHSYS_VER	ETHSYS revision number
7:0	ETHSYS_ECO_ID	ETHSYS ECO ID (IPM version in FPGA)

15000010 SYSCFG0 System Configuration Register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TEST_CODE															
Type	RW															
Reset	0	0	0	0	0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description
31:24	TEST_CODE	Default value is from bootstrap and can be modified by software.

15000014 SYSCFG1 System Configuration Register 1 00110014

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RSV1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GE2_MODE		GE1_MODE		GE0_MODE		SGMII_CONFIG_0	SGMII_CONFIG_1	RSV0							
Type	RW		RW		RW		RW	RW	RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0

Bit(s)	Name	Description
31:16	RSV1	Reserved
15:14	GE2_MODE	Gigabit Port #2 Mode
		Sets the interface mode on Gigabit port 2
13:12	GE1_MODE	Gigabit Port #1 Mode
		Sets the interface mode on Gigabit port 1
11:10	GE0_MODE	Gigabit Port #0 Mode
		Sets the interface mode on Gigabit port 0
9	SGMII_CONFIG_0	SGMII path enable of GMAC1
8	SGMII_CONFIG_1	SGMII path enable of GMAC2
7:0	RSV0	Reserved

15000018 TESTSTAT0 Firmware Test Status 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TESTSTAT0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TESTSTAT0															
Type	RW															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TESTSTAT0	Firmware Test Status Register 0

1500001C TESTSTAT1 Firmware Test Status 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TESTSTAT1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TESTSTAT1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TESTSTAT1	Firmware Test Status Register 1

15000020 CDM_TXFIFO_CNT CDM TX FIFO Count Status 000007FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

15000024 **BOOT_RELEASE** Release CPU's Command to Boot from SRAM 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BOOT_RELEASE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BOOT_RELEASE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	BOOT_RELEASE	Reserved

15000028 **FE_RST_CHK_IDLE_EN** Frame Engine Check IDLE Enable 003FFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

1500002C **CLKCFG0** Clock Configuration Register 0 C4001FE0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	OSC_1US_DIV															
Type	RW															
Reset	1	1	0	0	0	1										

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description
31:26	OSC_1US_DIV	Oscillator 1 usec Divider Sets the maximum for the reference clock counter for either a 20 MHz or 40 MHz external XTAL input. The count increments each 1usec (indicating 1 MHz), up to the maximum, before resetting to zero. This counts the frequency of an external XTAL. This count is used to output a 32 KHz frequency to the REFCLK0 pin.

15000030 CLKCFG1 Clock Configuration Register 1 FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																ESW_CLK_EN
Type																RW
Reset																1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WOCPU0_CLK_EN	WOCPU1_CLK_EN					GP0_CLK_EN	GP1_CLK_EN	GP2_CLK_EN	FE_CLK_EN						
Type	RW	RW					RW	RW	RW	RW						
Reset	1	1					1	1	1	1						

Bit(s)	Name	Description
16	ESW_CLK_EN	Ethernet switch clock control
15	WOCPU0_CLK_EN	WOCPU clock control
14	WOCPU1_CLK_EN	WOCPU clock control
9	GP0_CLK_EN	Giga port 0 clock control
8	GP1_CLK_EN	Giga port 1 clock control
7	GP2_CLK_EN	Giga port 2 clock control
6	FE_CLK_EN	Frame Engine clock control

15000034 RSTCTL Reset Control Register 06000004

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	PPE1_RST	PPE0_RST						RSV5	GMAC_RST							RSV2
Type	RW	RW						RW	RW							RW
Reset	0	0						0	0							0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								PMTR_RST		FE_RST						
Type								RW		RW						
Reset								0		0						

Bit(s)	Name	Description
31	PPE1_RST	PPE1 reset control
30	PPE0_RST	PPE0 reset control
24	RSV5	Reserved (EPHY reset control)
23	GMAC_RST	GMAC reset control
16	RSV2	Reserved (ETH switch reset control)
8	PMTR_RST	PMTR reset control
6	FE_RST	Frame Engine reset control

15000038 RSTSTAT Reset Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														SWSYS_RST		
Type														W1C		
Reset														0		

Bit(s)	Name	Description
2	SWSYSRST	Software system reset occurred This bit will be set if software reset the chip by writing to the RSTSYS bit in RSTCTL. Writing a '1' will clear this bit. Writing a '0' has not effect. NOTE: This register is reset only by a power on reset.

1500003C RSTCTL_WARP Reset Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

15000040 GPIO0_MODE GPIO0 Purpose Selection 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPIO0_MODE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO0_MODE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	GPIO0_MODE	Depend on SB_FIFO_SW_RD_EN. If SB_FIFO_SW_RD_EN=0: Reserved If SB_FIFO_SW_RD_EN=1: Side band FIFO read LSB

15000044 GPIO1_MODE GPIO1 Purpose Selection 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPIO1_MODE															
Type	RW															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO1_MODE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	GPIO1_MODE	Depend on SB_FIFO_SW_RD_EN. If SB_FIFO_SW_RD_EN=0: Reserved If SB_FIFO_SW_RD_EN=1: Side band FIFO read MSB

15000048 MEMO0 Memory0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MEMO0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MEMO0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MEMO0	Memory0

1500004C MEMO1 Memory1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MEMO1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MEMO1															

Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MEMO1	Memory1

15000050 **MEMO2** **Memory2** 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MEMO2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MEMO2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MEMO2	Memory2 (utif_in debug read)

15000054 **MEMO3** **Memory3** 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MEMO3															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MEMO3															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MEMO3	Memory3 (utif_out debug read)

15000058 MEMO4 Memory4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MEMO4															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description
31	MEMO4	Memory4 (MCUSYS_DBG_SEL0)

1500005C MEMO5 Memory5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MEMO5															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MEMO5															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MEMO5	Memory5 (MCUSYS_DBG_SEL1)

15000060 IOC_EN NETSYS IO Coherence Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	GLOBAL_IOC_EN															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					WOCPU_IOC_EN	WED1_IOC_EN	WED0_IOC_EN	FDMA_IOC_EN	EDMA1_IOC_EN	EDMA0_IOC_EN	MDMA_IOC_EN	WDMA1_IOC_EN	WDMA0_IOC_EN	PPE1_IOC_EN	PPE0_IOC_EN	ADMA_IOC_EN
Type					RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	GLOBAL_IOC_EN	Global IOC enable
11	WOCPU_IOC_EN	WOCPU IOC enable Only valid when GLOBAL_IOC_EN = 1
10	WED1_IOC_EN	WED1 IOC enable Only valid when GLOBAL_IOC_EN = 1
9	WED0_IOC_EN	WED0 IOC enable Only valid when GLOBAL_IOC_EN = 1
8	FDMA_IOC_EN	FDMA IOC enable Only valid when GLOBAL_IOC_EN = 1
7	EDMA1_IOC_EN	EDMA1 IOC enable Only valid when GLOBAL_IOC_EN = 1
6	EDMA0_IOC_EN	EDMA0 IOC enable Only valid when GLOBAL_IOC_EN = 1
5	MDMA_IOC_EN	MDMA IOC enable Only valid when GLOBAL_IOC_EN = 1
4	WDMA1_IOC_EN	WDMA1 IOC enable Only valid when GLOBAL_IOC_EN = 1
3	WDMA0_IOC_EN	WDMA0 IOC enable Only valid when GLOBAL_IOC_EN = 1
2	PPE1_IOC_EN	PPE1 IOC enable Only valid when GLOBAL_IOC_EN = 1
1	PPE0_IOC_EN	PPE0 IOC enable Only valid when GLOBAL_IOC_EN = 1
0	ADMA_IOC_EN	ADMA IOC enable Only valid when GLOBAL_IOC_EN = 1

15000064	BIST_CTRL	NETSYS Global BIST Configuration Register														00000000
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	INFRA2_NETSYS															

	NEAR_FULL															
Type	RO															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						NETSYS2INFRA_BIST_FAIL	NETSYS2INFRA_BIST_DONE	NETSYS2INFRA_BIST_EN		NETSYS2EMI_M1_BIST_FAIL	NETSYS2EMI_M1_BIST_DONE	NETSYS2EMI_M1_BIST_EN		NETSYS2EMI_M0_BIST_FAIL	NETSYS2EMI_M0_BIST_DONE	NETSYS2EMI_M0_BIST_EN
Type						RO	RO	RW		RO	RO	RW		RO	RO	RW
Reset						0	0	0		0	0	0		0	0	0

Bit(s)	Name	Description
31	INFRA2NETSYS_NEAR_FULL	INFRA2NETSYS GALS read data FIFO near full flag
10	NETSYS2INFRA_BIST_FAIL	Asserted when NETSYS2INFRA BIST test fails. Only valid when NETSYS2INFRA_BIST_DONE = 1
9	NETSYS2INFRA_BIST_DONE	Asserted when NETSYS2INFRA BIST test finishes
8	NETSYS2INFRA_BIST_EN	Start NETSYS2INFRA BIST test
6	NETSYS2EMI_M1_BIST_FAIL	Asserted when NETSYS2EMI_M1 BIST test fails. Only valid when NETSYS2EMI_M1_BIST_DONE = 1
5	NETSYS2EMI_M1_BIST_DONE	Asserted when NETSYS2EMI_M1 BIST test finishes
4	NETSYS2EMI_M1_BIST_EN	Start NETSYS2EMI_M1 BIST test
2	NETSYS2EMI_M0_BIST_FAIL	Asserted when NETSYS2EMI_M0 BIST test fails. Only valid when NETSYS2EMI_M0_BIST_DONE = 1
1	NETSYS2EMI_M0_BIST_DONE	Asserted when NETSYS2EMI_M0 BIST test finishes
0	NETSYS2EMI_M0_BIST_EN	Start NETSYS2EMI_M0 BIST test

15000068 BIST_NETSYS2EMI0 NETSYS2EMI_M0 BIST Configuration Register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													NETSYS2EMI_M0_AWULTRA_EN		NETSYS2EMI_M0_AWDOMAI_N_EN	
Type													RW		RW	
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	NETSYS2EMI_M0_AWUSER_EN	NETSYS2EMI_M0_AWPROT_EN	NETSYS2EMI_M0_AWCACHE_EN	NETSYS2EMI_M0_AWBURST_EN	NETSYS2EMI_M0_AWSIZE_EN	NETSYS2EMI_M0_AWADDR_EN	NETSYS2EMI_M0_AWLEN_EN	NETSYS2EMI_M0_AWID_EN								
Type	RW	RW	RW	RW	RW	RW	RW	RW								

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
19:18	NETSYS2EMI_M0_AWULTRA_EN	Test NETSYS2EMI_M0 awultra signal
17:16	NETSYS2EMI_M0_AWDOMAIN_EN	Test NETSYS2EMI_M0 awdomain signal
15:14	NETSYS2EMI_M0_AWUSER_EN	Test NETSYS2EMI_M0 awuser signal
13:12	NETSYS2EMI_M0_AWPROT_EN	Test NETSYS2EMI_M0 awprot signal
11:10	NETSYS2EMI_M0_AWCACHE_EN	Test NETSYS2EMI_M0 awcache signal
9:8	NETSYS2EMI_M0_AWBURST_EN	Test NETSYS2EMI_M0 awburst signal
7:6	NETSYS2EMI_M0_AWSIZE_EN	Test NETSYS2EMI_M0 awsize signal
5:4	NETSYS2EMI_M0_AWADDR_EN	Test NETSYS2EMI_M0 awaddr signal
3:2	NETSYS2EMI_M0_AWLEN_EN	Test NETSYS2EMI_M0 awlen signal
1:0	NETSYS2EMI_M0_AWID_EN	Test NETSYS2EMI_M0 awid signal

1500006C	BIST_NETSYS2EMI1				NETSYS2EMI_M0 BIST Configuration Register 1								00000000			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			NETSYS2EMI_M0_RRESP_EN		NETSYS2EMI_M0_RDATA_EN		NETSYS2EMI_M0_BRESP_EN		NETSYS2EMI_M0_WSTRB_EN		NETSYS2EMI_M0_WDATA_EN		NETSYS2EMI_M0_ARULTRA_EN		NETSYS2EMI_M0_ARDOMAIN_EN	
Type			RW		RW		RW		RW		RW		RW		RW	
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	NETSYS2EMI_M0_ARUSER_EN		NETSYS2EMI_M0_ARPROT_EN		NETSYS2EMI_M0_ARCACHE_EN		NETSYS2EMI_M0_ARBURST_EN		NETSYS2EMI_M0_ARSIZE_EN		NETSYS2EMI_M0_ARADDR_EN		NETSYS2EMI_M0_ARLEN_EN		NETSYS2EMI_M0_ARID_EN	
Type	RW		RW		RW		RW		RW		RW		RW		RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29:28	NETSYS2EMI_M0_RRESP_EN	Test NETSYS2EMI_M0 rresp signal
27:26	NETSYS2EMI_M0_RDATA_EN	Test NETSYS2EMI_M0 rdata signal
25:24	NETSYS2EMI_M0_BRESP_EN	Test NETSYS2EMI_M0 bresp signal
23:22	NETSYS2EMI_M0_WSTRB_EN	Test NETSYS2EMI_M0 wstrb signal
21:20	NETSYS2EMI_M0_WDATA_EN	Test NETSYS2EMI_M0 wdata signal
19:18	NETSYS2EMI_M0_ARULTRA_EN	Test NETSYS2EMI_M0 arultra signal
17:16	NETSYS2EMI_M0_ARDOMAIN_EN	Test NETSYS2EMI_M0 ardomain signal
15:14	NETSYS2EMI_M0_ARUSER_EN	Test NETSYS2EMI_M0 aruser signal
13:12	NETSYS2EMI_M0_ARPROT_EN	Test NETSYS2EMI_M0 arprot signal
11:10	NETSYS2EMI_M0_ARCACHE_EN	Test NETSYS2EMI_M0 arcache signal
9:8	NETSYS2EMI_M0_ARBURST_EN	Test NETSYS2EMI_M0 arburst signal
7:6	NETSYS2EMI_M0_ARSIZE_EN	Test NETSYS2EMI_M0 arsize signal
5:4	NETSYS2EMI_M0_ARADDR_EN	Test NETSYS2EMI_M0 araddr signal
3:2	NETSYS2EMI_M0_ARLEN_EN	Test NETSYS2EMI_M0 arlen signal

Bit(s)	Name	Description
1:0	NETSYS2EMI_M0_ARID_EN	Test NETSYS2EMI_M0 arid signal

15000070 BIST NETSYS2EMI2 NETSYS2EMI_M1 BIST Configuration Register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													NETSYS2EMI_M1_AWULTRA_EN		NETSYS2EMI_M1_AWDOMAIN_EN	
Type													RW		RW	
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	NETSYS2EMI_M1_AWUSER_EN		NETSYS2EMI_M1_AWPROT_EN		NETSYS2EMI_M1_AWCACHE_EN		NETSYS2EMI_M1_AWBURST_EN		NETSYS2EMI_M1_AWSIZE_EN		NETSYS2EMI_M1_AWADDR_EN		NETSYS2EMI_M1_AWLEN_EN		NETSYS2EMI_M1_AWID_EN	
Type	RW		RW		RW		RW		RW		RW		RW		RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
19:18	NETSYS2EMI_M1_AWULTRA_EN	Test NETSYS2EMI_M1 awultra signal
17:16	NETSYS2EMI_M1_AWDOMAIN_EN	Test NETSYS2EMI_M1 awdomain signal
15:14	NETSYS2EMI_M1_AWUSER_EN	Test NETSYS2EMI_M1 awuser signal
13:12	NETSYS2EMI_M1_AWPROT_EN	Test NETSYS2EMI_M1 awprot signal
11:10	NETSYS2EMI_M1_AWCACHE_EN	Test NETSYS2EMI_M1 awcache signal
9:8	NETSYS2EMI_M1_AWBURST_EN	Test NETSYS2EMI_M1 awburst signal
7:6	NETSYS2EMI_M1_AWSIZE_EN	Test NETSYS2EMI_M1 awsize signal
5:4	NETSYS2EMI_M1_AWADDR_EN	Test NETSYS2EMI_M1 awaddr signal
3:2	NETSYS2EMI_M1_AWLEN_EN	Test NETSYS2EMI_M1 awlen signal
1:0	NETSYS2EMI_M1_AWID_EN	Test NETSYS2EMI_M1 awid signal

15000074 BIST NETSYS2EMI3 NETSYS2EMI_M1 BIST Configuration Register 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			NETSYS2EMI_M1_RRESP_EN		NETSYS2EMI_M1_RDATA_EN		NETSYS2EMI_M1_BRESP_EN		NETSYS2EMI_M1_WSTRB_EN		NETSYS2EMI_M1_WDATA_EN		NETSYS2EMI_M1_ARULTRA_EN		NETSYS2EMI_M1_ARDOMAIN_EN	
Type			RW		RW		RW		RW		RW		RW		RW	
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	NETSYS2EMI_M1_ARUSER_EN	NETSYS2EMI_M1_ARPROT_EN	NETSYS2EMI_M1_ARCACHE_EN	NETSYS2EMI_M1_ARBURST_EN	NETSYS2EMI_M1_ARSIZE_EN	NETSYS2EMI_M1_ARADDR_EN	NETSYS2EMI_M1_ARLEN_EN	NETSYS2EMI_M1_ARID_EN
Type	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29:28	NETSYS2EMI_M1_RRESP_EN	Test NETSYS2EMI_M1 rresp signal
27:26	NETSYS2EMI_M1_RDATA_EN	Test NETSYS2EMI_M1 rdata signal
25:24	NETSYS2EMI_M1_BRESP_EN	Test NETSYS2EMI_M1 bresp signal
23:22	NETSYS2EMI_M1_WSTRB_EN	Test NETSYS2EMI_M1 wstrb signal
21:20	NETSYS2EMI_M1_WDATA_EN	Test NETSYS2EMI_M1 wdata signal
19:18	NETSYS2EMI_M1_ARULTRA_EN	Test NETSYS2EMI_M1 arultra signal
17:16	NETSYS2EMI_M1_ARDOMAIN_EN	Test NETSYS2EMI_M1 ardomain signal
15:14	NETSYS2EMI_M1_ARUSER_EN	Test NETSYS2EMI_M1 aruser signal
13:12	NETSYS2EMI_M1_ARPROT_EN	Test NETSYS2EMI_M1 arprot signal
11:10	NETSYS2EMI_M1_ARCACHE_EN	Test NETSYS2EMI_M1 arcache signal
9:8	NETSYS2EMI_M1_ARBURST_EN	Test NETSYS2EMI_M1 arburst signal
7:6	NETSYS2EMI_M1_ARSIZE_EN	Test NETSYS2EMI_M1 arsize signal
5:4	NETSYS2EMI_M1_ARADDR_EN	Test NETSYS2EMI_M1 araddr signal
3:2	NETSYS2EMI_M1_ARLEN_EN	Test NETSYS2EMI_M1 arlen signal
1:0	NETSYS2EMI_M1_ARID_EN	Test NETSYS2EMI_M1 arid signal

15000078 BIST NETSYS2INFRA0 NETSYS2INFRA BIST Configuration Register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													NETSYS2INFRA_AWULTRA_EN		NETSYS2INFRA_AWDOMAIN_EN	
Type													RW		RW	
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	NETSYS2INFRA_AWUSER_EN	NETSYS2INFRA_AWPROT_EN	NETSYS2INFRA_AWCACHE_EN	NETSYS2INFRA_AWBURST_EN	NETSYS2INFRA_AWSIZE_EN	NETSYS2INFRA_AWADDR_EN	NETSYS2INFRA_AWLEN_EN	NETSYS2INFRA_AWID_EN								
Type	RW	RW	RW	RW	RW	RW	RW	RW								
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
19:18	NETSYS2INFRA_AWULTRA_EN	Test NETSYS2INFRA awultra signal
17:16	NETSYS2INFRA_AWDOMAIN_EN	Test NETSYS2INFRA awdomain signal
15:14	NETSYS2INFRA_AWUSER_EN	Test NETSYS2INFRA awuser signal
13:12	NETSYS2INFRA_AWPROT_EN	Test NETSYS2INFRA awprot signal
11:10	NETSYS2INFRA_AWCACHE_EN	Test NETSYS2INFRA awcache signal

Bit(s)	Name	Description
9:8	NETSYS2INFRA_AWBURST_EN	Test NETSYS2INFRA awburst signal
7:6	NETSYS2INFRA_AWSIZE_EN	Test NETSYS2INFRA awsize signal
5:4	NETSYS2INFRA_AWADDR_EN	Test NETSYS2INFRA awaddr signal
3:2	NETSYS2INFRA_AWLEN_EN	Test NETSYS2INFRA awlen signal
1:0	NETSYS2INFRA_AWID_EN	Test NETSYS2INFRA awid signal

1500007C BIST_NETSYS2INFRA1 NETSYS2INFRA BIST Configuration Register 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			NETSYS2INFRA_RRESP_EN	NETSYS2INFRA_RDATA_EN	NETSYS2INFRA_BRESP_EN	NETSYS2INFRA_WSTRB_EN	NETSYS2INFRA_WDATA_EN	NETSYS2INFRA_ARULTRA_EN	NETSYS2INFRA_ARDOMAIN_EN							
Type			RW	RW	RW	RW	RW	RW	RW							
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	NETSYS2INFRA_ARUSER_EN	NETSYS2INFRA_ARPROT_EN	NETSYS2INFRA_ARCACHE_EN	NETSYS2INFRA_ARBURST_EN	NETSYS2INFRA_ARSIZE_EN	NETSYS2INFRA_ARADDR_EN	NETSYS2INFRA_ARLEN_EN	NETSYS2INFRA_ARID_EN								
Type	RW	RW	RW	RW	RW	RW	RW	RW								
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29:28	NETSYS2INFRA_RRESP_EN	Test NETSYS2INFRA rresp signal
27:26	NETSYS2INFRA_RDATA_EN	Test NETSYS2INFRA rdata signal
25:24	NETSYS2INFRA_BRESP_EN	Test NETSYS2INFRA bresp signal
23:22	NETSYS2INFRA_WSTRB_EN	Test NETSYS2INFRA wstrb signal
21:20	NETSYS2INFRA_WDATA_EN	Test NETSYS2INFRA wdata signal
19:18	NETSYS2INFRA_ARULTRA_EN	Test NETSYS2INFRA arultra signal
17:16	NETSYS2INFRA_ARDOMAIN_EN	Test NETSYS2INFRA ardomain signal
15:14	NETSYS2INFRA_ARUSER_EN	Test NETSYS2INFRA aruser signal
13:12	NETSYS2INFRA_ARPROT_EN	Test NETSYS2INFRA arprot signal
11:10	NETSYS2INFRA_ARCACHE_EN	Test NETSYS2INFRA arcache signal
9:8	NETSYS2INFRA_ARBURST_EN	Test NETSYS2INFRA arburst signal
7:6	NETSYS2INFRA_ARSIZE_EN	Test NETSYS2INFRA arsize signal
5:4	NETSYS2INFRA_ARADDR_EN	Test NETSYS2INFRA araddr signal
3:2	NETSYS2INFRA_ARLEN_EN	Test NETSYS2INFRA arlen signal
1:0	NETSYS2INFRA_ARID_EN	Test NETSYS2INFRA arid signal

15000080 AXICFG0 AXI Sideband Configuration Register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																

Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ADMA_M_ARFLUSH		ADMA_M_ARULTRA		ADMA_M_ARDOMAIN				ADMA_M_AWFLUSH		ADMA_M_AWULTRA		ADMA_M_AWDOMAIN			
Type	RW		RW		RW				RW		RW		RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:14	ADMA_M_ARFLUSH	ADMA arflush
13:12	ADMA_M_ARULTRA	ADMA arultra
11:8	ADMA_M_ARDOMAIN	ADMA ardomain
7:6	ADMA_M_AWFLUSH	ADMA awflush
5:4	ADMA_M_AWULTRA	ADMA awultra
3:0	ADMA_M_AWDOMAIN	ADMA awdomain

15000084 AXICFG1 AXI Sideband Configuration Register 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PPE1_M_ARFLUSH		PPE1_M_ARULTRA		PPE1_M_ARDOMAIN				PPE1_M_AWFLUSH		PPE1_M_AWULTRA		PPE1_M_AWDOMAIN			
Type	RW		RW		RW				RW		RW		RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PPE0_M_ARFLUSH		PPE0_M_ARULTRA		PPE0_M_ARDOMAIN				PPE0_M_AWFLUSH		PPE0_M_AWULTRA		PPE0_M_AWDOMAIN			
Type	RW		RW		RW				RW		RW		RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:30	PPE1_M_ARFLUSH	PPE1 arflush
29:28	PPE1_M_ARULTRA	PPE1 arultra
27:24	PPE1_M_ARDOMAIN	PPE1 ardomain
23:22	PPE1_M_AWFLUSH	PPE1 awflush
21:20	PPE1_M_AWULTRA	PPE1 awultra
19:16	PPE1_M_AWDOMAIN	PPE1 awdomain
15:14	PPE0_M_ARFLUSH	PPE0 arflush
13:12	PPE0_M_ARULTRA	PPE0 arultra
11:8	PPE0_M_ARDOMAIN	PPE0 ardomain
7:6	PPE0_M_AWFLUSH	PPE0 awflush

Bit(s)	Name	Description
5:4	PPE0_M_AWULTRA	PPE0 awultra
3:0	PPE0_M_AWDOMAIN	PPE0 awdomain

15000088 GALSCFG0 GALS Configuration Register 0 01000100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		NETSYS2EMI_M1_IDLE_MASK						NETSYS2EMI_M1_SAMPLE_SEL	NETSYS2EMI_M1_SLV_SYNC_SEL	NETSYS2EMI_M1_MST_SYNC_SEL	NETSYS2EMI_M1_ARFLUSH_THRE	NETSYS2EMI_M1_AWFLUSH_THRE				
Type		RW						RW	RW	RW	RW	RW				
Reset		0	0	0				1	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		NETSYS2EMI_M0_IDLE_MASK						NETSYS2EMI_M0_SAMPLE_SEL	NETSYS2EMI_M0_SLV_SYNC_SEL	NETSYS2EMI_M0_MST_SYNC_SEL	NETSYS2EMI_M0_ARFLUSH_THRE	NETSYS2EMI_M0_AWFLUSH_THRE				
Type		RW						RW	RW	RW	RW	RW				
Reset		0	0	0				1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
30:28	NETSYS2EMI_M1_IDLE_MASK	Idle signal mask
24	NETSYS2EMI_M1_SAMPLE_SEL	NETSYS2EMI_M1 GALS select first step of sample clock edge of master & slaver synchronizer
23:22	NETSYS2EMI_M1_SLV_SYNC_SEL	NETSYS2EMI_M1 GALS slaver synchronizer step
21:20	NETSYS2EMI_M1_MST_SYNC_SEL	NETSYS2EMI_M1 GALS master synchronizer step
19:18	NETSYS2EMI_M1_ARFLUSH_THRE	NETSYS2EMI_M1 GALS read FIFO near full threshold
17:16	NETSYS2EMI_M1_AWFLUSH_THRE	NETSYS2EMI_M1 GALS write FIFO near full threshold
14:12	NETSYS2EMI_M0_IDLE_MASK	Idle signal mask
8	NETSYS2EMI_M0_SAMPLE_SEL	NETSYS2EMI_M0 GALS select first step of sample clock edge of master & slaver synchronizer
7:6	NETSYS2EMI_M0_SLV_SYNC_SEL	NETSYS2EMI_M0 GALS slaver synchronizer step
5:4	NETSYS2EMI_M0_MST_SYNC_SEL	NETSYS2EMI_M0 GALS master synchronizer step
3:2	NETSYS2EMI_M0_ARFLUSH_THRE	NETSYS2EMI_M0 GALS read FIFO near full threshold
1:0	NETSYS2EMI_M0_AWFLUSH_THRE	NETSYS2EMI_M0 GALS write FIFO near full threshold

1500008C GALSCFG1 GALS Configuration Register 1 01000100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name			INFRA2NETSYS_IDLE_MASK				INFRA2NETSYS_RFIFO_NEAR_FULL_EN	INFRA2NETSYS_SAMPLE_SEL	INFRA2NETSYS_SLV_SYNC_SEL		INFRA2NETSYS_MST_SYNC_SEL		INFRA2NETSYS_RFIFO_THRE			
Type			RW				RW	RW	RW		RW		RW			
Reset			0	0			0	1	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		NETSYS2INFRA_IDLE_MASK						NETSYS2INFRA_SAMPLE_SEL	NETSYS2INFRA_SLV_SYNC_SEL		NETSYS2INFRA_MST_SYNC_SEL		NETSYS2INFRA_ARFLUSH_THRE		NETSYS2INFRA_AWFLUSH_THRE	
Type		RW						RW	RW		RW		RW		RW	
Reset		0	0	0				1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29:28	INFRA2NETSYS_IDLE_MASK	Idle signal mask
25	INFRA2NETSYS_RFIFO_NEAR_FULL_EN	INFRA2NETSYS GALS read data FIFO near full control enable
24	INFRA2NETSYS_SAMPLE_SEL	INFRA2NETSYS GALS select first step of sample clock edge of master & slaver synchronizer
23:22	INFRA2NETSYS_SLV_SYNC_SEL	INFRA2NETSYS GALS slaver synchronizer step
21:20	INFRA2NETSYS_MST_SYNC_SEL	INFRA2NETSYS GALS master synchronizer step
19:16	INFRA2NETSYS_RFIFO_THRE	INFRA2NETSYS GALS read data FIFO near full threshold
14:12	NETSYS2INFRA_IDLE_MASK	Idle signal mask
8	NETSYS2INFRA_SAMPLE_SEL	NETSYS2INFRA GALS select first step of sample clock edge of master & slaver synchronizer
7:6	NETSYS2INFRA_SLV_SYNC_SEL	NETSYS2INFRA GALS slaver synchronizer step
5:4	NETSYS2INFRA_MST_SYNC_SEL	NETSYS2INFRA GALS master synchronizer step
3:2	NETSYS2INFRA_ARFLUSH_THRE	NETSYS2INFRA GALS read FIFO near full threshold
1:0	NETSYS2INFRA_AWFLUSH_THRE	NETSYS2INFRA GALS write FIFO near full threshold

15000090				MISTAT				NETSYS Bus MI Status Register								00000000			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16			
Name																			
Type																			
Reset																			
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0			

Name			MAS_UP1_ERR_FLGA	MAS_UP0_ERR_FLGA		SLV_MI_LOCK_ERR_FLAG	SLV_MI_ERRMID_SET_RIRQ	SLV_MI_ERRMID_SET_BIRQ		MAS_MI1_LOCK_ERR_FLAG	MAS_MI1_ERRMID_SET_RIRQ	MAS_MI1_ERRMID_SET_BIRQ		MAS_MIO_LOCK_ERR_FLAG	MAS_MIO_ERRMID_SET_RIRQ	MAS_MIO_ERRMID_SET_BIRQ
Type			RO	RO		RO	RO	RO		RO	RO	RO		RO	RO	RO
Reset			0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Name	Description
13	MAS_UP1_ERR_FLGA	MAS_UP1 detects error
12	MAS_UP0_ERR_FLGA	MAS_UP0 detects error
10	SLV_MI_LOCK_ERR_FLAG	SLV_MI detects lock error
9	SLV_MI_ERRMID_SET_RIRQ	SLV_MI detects error MID from slave in R channel
8	SLV_MI_ERRMID_SET_BIRQ	SLV_MI detects error MID from slave in B channel
6	MAS_MI1_LOCK_ERR_FLAG	MAS_MI1 detects lock error
5	MAS_MI1_ERRMID_SET_RIRQ	MAS_MI1 detects error MID from slave in R channel
4	MAS_MI1_ERRMID_SET_BIRQ	MAS_MI1 detects error MID from slave in B channel
2	MAS_MIO_LOCK_ERR_FLAG	MAS_MIO detects lock error
1	MAS_MIO_ERRMID_SET_RIRQ	MAS_MIO detects error MID from slave in R channel
0	MAS_MIO_ERRMID_SET_BIRQ	MAS_MIO detects error MID from slave in B channel

15000094 **SIOSTAT0** NETSYS Bus SI Status Register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SLV_SI_VIO_ID												SLV_SI_VIO_WAY_EN			SLV_SI_VIO_WR
Type	RO												RO			RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SLV_SI_VIO_RD	SLV_SI_VIO_DECERR	MAS_SI_VIO_ID									MAS_SI_VIO_WAY_EN			MAS_SI_VIO_WR	MAS_SI_VIO_DECERR
Type	RO	RO	RO									RO			RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:20	SLV_SI_VIO_ID	SLV_SI violation id
19:17	SLV_SI_VIO_WAY_EN	SLV_SI violation way_en
16	SLV_SI_VIO_WR	SLV_SI violation write transaction
15	SLV_SI_VIO_RD	SLV_SI violation read transaction
14	SLV_SI_VIO_DECERR	SLV_SI violation decode error

Bit(s)	Name	Description
13:6	MAS_SI_VIO_ID	MAS_SI violation id
5:3	MAS_SI_VIO_WAY_EN	MAS_SI violation way_en
2	MAS_SI_VIO_WR	MAS_SI violation write transaction
1	MAS_SI_VIO_RD	MAS_SI violation read transaction
0	MAS_SI_VIO_DECERR	MAS_SI violation decode error

15000098 **SI0STAT1** NETSYS Bus SI Status Register 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAS_SI_VIO_ADDR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAS_SI_VIO_ADDR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MAS_SI_VIO_ADDR	MAS_SI violation address

1500009C **SI0STAT2** NETSYS Bus SI Status Register 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SLV_SI_VIO_ADDR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SLV_SI_VIO_ADDR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SLV_SI_VIO_ADDR	SLV_SI violation address

150000A0 S2PSTAT0 NETSYS Bus S2P Status Register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SLV_S2P_VIO_ID															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SLV_S2P_VIO_DOMAIN				SLV_S2P_VIO_WAY_EN								SLV_S2P_VIO_WR	SLV_S2P_VIO_RD	SLV_S2P_VIO_DECERR	SLV_S2P_VIO_ADDR_unaligned
Type	RO				RO								RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:17	SLV_S2P_VIO_ID	SLV_S2P violation id
15:12	SLV_S2P_VIO_DOMAIN	SLV_S2P violation domain
11:4	SLV_S2P_VIO_WAY_EN	SLV_S2P violation way_en
3	SLV_S2P_VIO_WR	SLV_S2P violation write transaction
2	SLV_S2P_VIO_RD	SLV_S2P violation read transaction
1	SLV_S2P_VIO_DECERR	SLV_S2P violation decode error
0	SLV_S2P_VIO_ADDR_unaligned	SLV_S2P violation unaligned address

150000A4 S2PSTAT1 NETSYS Bus S2P Status Register 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SLV_S2P_VIO_ADDR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SLV_S2P_VIO_ADDR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SLV_S2P_VIO_ADDR	SLV_S2P violation address

150000A8 X2SSTAT0 NETSYS Bus X2S Status Register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						SLV_X2S_VIO_ID										
Type						RO										
Reset						0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SLV_X2S_VIO_ID				SLV_X2S_VIO_WR	SLV_X2S_VIO_RD									SLV_X2S_VIO_DECERR	SLV_X2S_VIO_ADDR_unaligned
Type	RO				RO	RO									RO	RO
Reset	0	0	0	0	0	0									0	0

Bit(s)	Name	Description
26:12	SLV_X2S_VIO_ID	SLV_X2S violation id
11	SLV_X2S_VIO_WR	SLV_X2S violation write transaction
10	SLV_X2S_VIO_RD	SLV_X2S violation read transaction
1	SLV_X2S_VIO_DECERR	SLV_X2S violation decode error
0	SLV_X2S_VIO_ADDR_unaligned	SLV_X2S violation unaligned address

150000AC X2SSTAT1 NETSYS Bus X2S Status Register 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SLV_X2S_VIO_ADDR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SLV_X2S_VIO_ADDR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SLV_X2S_VIO_ADDR	SLV_X2S violation address

150000B0 R2XCFG0 R2X Configuration Register 0 000F00FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	R2X_MST_SEL								R2X_INT_B							
Type	RW								RO							
Reset		0	0	0					0	0	0	0	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									R2X_INT_EN							
Type									RW							
Reset									1	1	1	1	1	1	1	1

Bit(s)	Name	Description
30:28	R2X_MST_SEL	R2X channel debug information select
23:16	R2X_INT_B	R2X interrupt status R2X wrapper interrupt will set 1'b1 when receive len = 0 cmd from rbus master.
7:0	R2X_INT_EN	R2X Interrupt Enable Enable R2X wrapper interrupt when receive len = 0 cmd from rbus master.

150000B4 R2XCFG1 R2X Configuration Register 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	R2X_DBG_SEL_7				R2X_DBG_SEL_6				R2X_DBG_SEL_5				R2X_DBG_SEL_4			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	R2X_DBG_SEL_3				R2X_DBG_SEL_2				R2X_DBG_SEL_1				R2X_DBG_SEL_0			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:28	R2X_DBG_SEL_7	Select debug information from R2X (Reserved)
27:24	R2X_DBG_SEL_6	Select debug information from R2X (Reserved)
23:20	R2X_DBG_SEL_5	Select debug information from R2X (Reserved)
19:16	R2X_DBG_SEL_4	Select debug information from R2X (Reserved)

Bit(s)	Name	Description
15:12	R2X_DBG_SEL_3	Select debug information from R2X (Reserved)
11:8	R2X_DBG_SEL_2	Select debug information from R2X (NETSYS PPE1)
7:4	R2X_DBG_SEL_1	Select debug information from R2X (NETSYS PPE0)
3:0	R2X_DBG_SEL_0	Select debug information from R2X (NETSYS ADMA)

150000B8 R2XSTAT0 R2X Status Register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	R2X_INT_STATUS															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	R2X_INT_STATUS															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	R2X_INT_STATUS	Record the address when receive len = 0 cmd from R2X selected channel according to R2XCFG0[30:28]

150000BC R2XSTAT1 R2X Status Register 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	R2X_DBG_INFO															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	R2X_DBG_INFO															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	R2X_DBG_INFO	Record debug information from R2X selected channel according to R2XCFG0[30:28]

150000C0 APBCFG NETSYS_APB Configuration Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																NETSYS_APB_INT_CLR
Type																W1C
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	NETSYS_APB_ERR_CNT						NETSYS_APB_INT_CNT									
Type	RO						RW									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	NETSYS_APB_INT_CLR	NETSYS_APB interrupt clear Write 1 to clear this interrupt.
15:10	NETSYS_APB_ERR_CNT	NETSYS_APB error counter
9:0	NETSYS_APB_INT_CNT	NETSYS_APB interrupt countdown timer Sets a delay timer which begins counting down when an error is detected. When the timer reaches zero the interrupt is then triggered.

150000C4 APBSTAT NETSYS_APB Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	NETSYS_APB_ERR_ADDR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	NETSYS_APB_ERR_ADDR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	NETSYS_APB_ERR_ADDR	NETSYS_APB address record for previous error found

150000CC NETSYS_DVFS_CFG0 NETSYS DVFS Configuration0 00320030

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

150000D0 NETSYS_DVFS_CFG1 NETSYS DVFS Configuration1 00000331

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

150000D4 NETSYS_DVFS_CFG2 NETSYS DVFS Configuration2 77777777

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																

Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

150000D8 NETSYS DVFS_TH1 NETSYS DVFS ThresHold1 00D800B4

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

150000DC NETSYS DVFS_TH2 NETSYS DVFS ThresHold2 0090006C

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																

Reset																

Bit(s)	Name	Description

150000E0 **NETSYS DVFS TH3** **NETSYS DVFS ThresHold3** **00480024**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

150000E4 **NETSYS LP_CFG0** **NETSYS Low Power Configuration0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

150000E8 **NETSYS LP_CFG1** **NETSYS Low Power Configuration1** **B0000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

150000EC NETSYS_IDLE_CFG0 NETSYS Low Power Idle Configuration0 0032007F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

150000F0 NETSYS_IDLE_CFG1 NETSYS Low Power Idle Configuration1 01F401F4

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

150000F4 **NETSYS_INT_STATUS** **NETSYS interrupt status** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

150000F8 **NETSYS_INT_ENABLE** **NETSYS interrupt enable** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

150000FC		NETSYS_MISC				NETSYS MISC								00000080		
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

15001000		MBIST_GCTRL				MBIST Global Control Register											3FC00000	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16		
Name																		
Type																		
Reset																		
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
Name																		
Type																		
Reset																		

Bit(s)	Name	Description

15001004		MBIST_BKG		MBIST Background Control Register												55AA55AA	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
Name																	

Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

15001008 MBIST_BSEL MBIST bsel Control Register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

1500100C MBIST_MISC MBIST Misc. Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																

Type																
Reset																

Bit(s)	Name	Description

15001010 MBIST_GSTS MBIST Global Status Register 00000002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

15001020 MBIST_STS_G0 MBIST Status Register Group 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

15001024 MBIST_STS_G1 MBIST Status Register Group 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

15001028 MBIST_STS_G2 MBIST Status Register Group 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

15001040 MBIST_FINISH_G0 MBIST Finish Register Group 0 0000003F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

15001044 **MBIST_FINISH_G1** **MBIST Finish Register Group 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

15001048 **MBIST_FINISH_G2** **MBIST Finish Register Group 2** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

15001060 MBIST_DELSEL_G0 MBIST DELSEL Register Group 0 00002AAA

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

15001064 MBIST_DELSEL_G1 MBIST DELSEL Register Group 1 0000002A

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

15001068 MBIST_DELSEL_G2 MBIST DELSEL Register Group 2 000A041A

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																

Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

150010F0 **RG SPARE G0** **RG Spare Register Group 0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

150010F4 **RG SPARE G1** **RG Spare Register Group 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																

Type																
Reset																

Bit(s)	Name	Description

15001100 ETH MEM DESEL GRP0 ETHSYS SRAM DESEL Group 0 0AAAA5A5

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

15001104 ETH MEM DESEL GRP1 ETHSYS SRAM DESEL Group 1 0000AAAA

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

15001108 ETH MEM BKG_GRP0 ETHSYS SRAM MBIST Background Group 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

1500110C ETH MEM BSEL_GRP0 ETHSYS SRAM BSEL Group 0 FFFF0F73

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

15001110 WED0_MBIST_GCTRL WED0 MBIST Global Control Register 01000100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

15001114 WED0_MBIST_GSTS WED0 MBIST Global Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

15001118 WED0_MEM_DELSEL WED0 Memory DELSEL 00000052

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

1500111C WED0 MBIST BKG WED0 MBIST Background 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

15001120 WED0 MBIST BSEL WED0 MBIST BSEL FFFF0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

15001124 WED1 MBIST GCTRL WED1 MBIST Global Control Register 01000100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																

Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

15001128 WED1 MBIST GSTS WED1 MBIST Global Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

1500112C WED1 MEM DELSEL WED1 Memory DELSEL 00000052

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																

Type																
Reset																

Bit(s)	Name	Description

15001130 WED1_MBIST_BKG WED1 MBIST Background 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

15001134 WED1_MBIST_BSEL WED1 MBIST BSEL FFFF0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

15001800 TMBIST_DESEL_0 MEM_BIST_DESEL_REG_0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name														delsel		
Type														RW		
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	delsel															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
19:0	delsel	

15001804 TMBIST_USE_DEFAULT_DESEL_MRM_BIST_USE_DEFAULT_DESEL_0 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																use_default_delsel
Type																RW
Reset																1

Bit(s)	Name	Description
0	use_default_delsel	

15001808 TMBIST_DESEL_1 MEM_BIST_DESEL_REG_1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name														delsel		

Type													RW			
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dtsel															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
19:0	dtsel	

1500180C TMBIST_USE_DEFAULT_DESE MRM_BIST_USE_DEFAULT_DESEL_1 00000001
L_1

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																use_de fault_d tsel
Type																RW
Reset																1

Bit(s)	Name	Description
0	use_default_dtsel	

15001810 TMBIST_DESEL_2 MEM_BIST_DESEL_REG_2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													dtsel			
Type													RW			
Reset													0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	delsel															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
19:0	delsel	

15001814 **TMBIST_USE_DEFAULT_DESE_MRM_BIST_USE_DEFAULT_DELSEL_2** 00000001
L 2

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																use_de fault_d elsel
Type																RW
Reset																1

Bit(s)	Name	Description
0	use_default_delsel	

15001818 **TMBIST_DESEL_3** **MEM_BIST_DESEL_REG_3** 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													delsel			
Type													RW			
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	delsel															

Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
19:0	delsel	

1500181C TMBIST_USE_DEFAULT_DESE_MRM_BIST_USE_DEFAULT_DESEL_3 00000001

L 3

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																use_de fault_d elsel
Type																RW
Reset																1

Bit(s)	Name	Description
0	use_default_delsel	

15001820 TMBIST_DESEL_4 MEM_BIST_DESEL_REG_4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													delsel			
Type													RW			
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	delsel															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
19:0	delsel	

15001824 **TMBIST USE DEFAULT DESE MRM_BIST_USE_DEFAULT_DELSEL_4** 00000001

L 4

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																use_de fault_d elsel
Type																RW
Reset																1

Bit(s)	Name	Description
0	use_default_delsel	

15001828 **TMBIST DESEL_5 MEM_BIST_DESEL_REG_5** 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													delsel			
Type													RW			
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	delsel															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
19:0	delsel	

1500182C TMBIST USE DEFAULT DESE MRM_BIST_USE_DEFAULT_DESEL_5

00000001

L 5

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																use_de fault_d elsel
Type																RW
Reset																1

Bit(s)	Name	Description
0	use_default_delsel	

15001830 TMBIST DESEL 6 MEM_BIST_DESEL_REG_6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													delsel			
Type													RW			
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	delsel															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
19:0	delsel	

15001834 TMBIST USE DEFAULT DESE MRM_BIST_USE_DEFAULT_DESEL_6

00000001

L 6

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																use_de fault_d elsel
Type																RW
Reset																1

Bit(s)	Name	Description
0	use_default_delsel	

15001838 TMBIST_DESEL_7 MEM_BIST_DESEL_REG_7 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													delsel			
Type													RW			
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	delsel															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
19:0	delsel	

1500183C TMBIST_USE_DEFAULT_DESE MRM_BIST_USE_DEFAULT_DESEL_7 00000001
L_7

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																

Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																use_de fault_d elsel
Type																RW
Reset																1

Bit(s)	Name	Description
0	use_default_delsel	

15001840 TMBIST_DESEL_8 MEM_BIST_DESEL_REG_8 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																delsel
Type																RW
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																delsel
Type																RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
19:0	delsel	

15001844 TMBIST_USE_DEFAULT_DESEL_MRM_BIST_USE_DEFAULT_DESEL_8 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name																	use_de fault_d elsel
Type																	RW
Reset																	1

Bit(s)	Name	Description
0	use_default_delsel	

15001848 TMBIST_DESEL_9 MEM_BIST_DESEL_REG_9 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													delsel			
Type													RW			
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	delsel															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
19:0	delsel	

1500184C TMBIST_USE_DEFAULT_DESE MRM_BIST_USE_DEFAULT_DESEL_9 00000001
L 9

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																use_de fault_d elsel

Type																	RW
Reset																	1

Bit(s)	Name	Description
0	use_default_dtsel	

15001850 TMBIST_DESEL_10 MEM_BIST_DESEL_REG_10 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													dtsel			
Type													RW			
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dtsel															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
19:0	dtsel	

15001854 TMBIST_USE_DEFAULT_DESEL_MRM_BIST_USE_DEFAULT_DESEL_10 00000001
L 10

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																use_default_dtsel
Type																RW
Reset																1

Bit(s)	Name	Description
0	use_default_delsel	

15001858 **TMBIST_DESEL_11** **MEM_BIST_DESEL_REG_11** 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													delsel			
Type													RW			
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	delsel															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
19:0	delsel	

1500185C **TMBIST_USE_DEFAULT_DESE_MRM_BIST_USE_DEFAULT_DESEL_11** 00000001
L 11

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																use_default_delsel
Type																RW
Reset																1

Bit(s)	Name	Description
0	use_default_delsel	

15001860 TMBIST_DESEL_12 MEM_BIST_DESEL_REG_12 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name														delsel		
Type														RW		
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	delsel															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
19:0	delsel	

15001864 TMBIST_USE_DEFAULT_DESE_MRM_BIST_USE_DEFAULT_DESEL_12 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																use_de fault_d elsel
Type																RW
Reset																1

Bit(s)	Name	Description
0	use_default_delsel	

15001868 TMBIST_DESEL_13 MEM_BIST_DESEL_REG_13 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name														delsel		

Type													RW			
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dtsel															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
19:0	dtsel	

1500186C TMBIST_USE_DEFAULT_DESE MRM_BIST_USE_DEFAULT_DESEL_13 00000001
L_13

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																use_de fault_d tsel
Type																RW
Reset																1

Bit(s)	Name	Description
0	use_default_dtsel	

15001870 TMBIST_DESEL_14 MEM_BIST_DESEL_REG_14 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													dtsel			
Type													RW			
Reset													0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	delsel															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
19:0	delsel	

15001874 TMBIST_USE_DEFAULT_DESE_MRM_BIST_USE_DEFAULT_DELSEL_14 00000001
L 14

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																use_de fault_d elsel
Type																RW
Reset																1

Bit(s)	Name	Description
0	use_default_delsel	

15001878 TMBIST_CLK_CG_EN MEM_BIST_CLK_CG_EN 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																delsel

Type																	RW
Reset																	0

Bit(s)	Name	Description
0	delsel	

15001A00 TMBIST_PREFUSE_LOAD MEM_PREFUSE_LOAD_REG 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																prefuse_load
Type																RW
Reset																0

Bit(s)	Name	Description
0	prefuse_load	

15001A04 TMBIST_PREFUSE_SEL MEM_PREFUSE_SEL_REG 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																prefuse_sel
Type																RW
Reset																0

Bit(s)	Name	Description
0	prefuse_sel	

15001A08 TMBIST_PREFUSE_CONFIG0 MEM_PREFUSE_CONFIG0_REG 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

15001A0C TMBIST_PREFUSE_CONFIG1 MEM_PREFUSE_CONFIG1_REG 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

15001A10 TMBIST_PREFUSE_CONFIG2 MEM_PREFUSE_CONFIG2_REG 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

15001A14 TMBIST_PREFUSE_CONFIG3 MEM_PREFUSE_CONFIG3_REG 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

15001A18 TMBIST_PREFUSE_CONFIG4 MEM_PREFUSE_CONFIG4_REG 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name																
Type																
Reset																

Bit(s)	Name	Description

15001A1C TMBIST_PREFUSE_CONFIG5 MEM_PREFUSE_CONFIG5_REG 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

15001A20 TMBIST_PREFUSE_CONFIG6 MEM_PREFUSE_CONFIG6_REG 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description														
15004000		PMTR_MAIN_CTL				Main control and total cntr overflow										00000000
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PMTR_DLY_EN														PMTR_DT1_WR_TOTAL_CNTR_OVERFLOW	PMTR_DT1_RD_TOTAL_CNTR_OVERFLOW
Type	RW														RO	RO
Reset	0														0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PMTR_DT1_WDTOTAL_CNTR_OVERFLOW	PMTR_DT1_RDTOTAL_CNTR_OVERFLOW	PMTR_DT1_WRTOTAL_CNTR_OVERFLOW	PMTR_DT1_RDTOTAL_CNTR_OVERFLOW	PMTR_DT1_WRTOTAL_CNTR_OVERFLOW	PMTR_DT1_RDTOTAL_CNTR_OVERFLOW	PMTR_CNTL_PT_MODE	PMTR_PT_MODE								PMTR_EN
Type	RO	RO	RO	RO	RO	RO	RW	RW								RW
Reset	0	0	0	0	0	0	0	0								0

Bit(s)	Name	Description
31	PMTR_DLY_EN	PMTR Delay Function Enable delay function counter enable 0: Enable pmtr when rg_pmtr_en_pre =1 1: enable pmtr when rg_pmtr_en_pre = 1 and delay counter expired
17	PMTR_DT1_WR_TOTAL_CNTR_OVERFLOW	DT1 WRT REQ Total Counter OV Write request total counter overflow for DT1 If overflow bit is 1, the value of PMTR_DT1_WR_TOTAL_CNTR is meaningless.
16	PMTR_DT1_RD_TOTAL_CNTR_OVERFLOW	DT1 RD REQ Total Counter OV Read request total counter overflow for DT1 If overflow bit is 1, the value of PMTR_DT1_RD_TOTAL_CNTR is meaningless.
15	PMTR_DT1_WDT_TOTAL_CNTR_OVERFLOW	DT1 WRT Data Total Counter OV Write data total counter overflow for DT1 If overflow bit is 1, the value of PMTR_DT1_WDT_TOTAL_CNTR is meaningless.
14	PMTR_DT1_RDT_TOTAL_CNTR_OVERFLOW	DT1 RD Data Total Counter OV Read data total counter overflow for DT1 If overflow bit is 1, the value of PMTR_DT1_RDT_TOTAL_CNTR is meaningless.

Bit(s)	Name	Description
13	PMTR_DT0_WR_TOTAL_CNTR_OVERFLOW	DT0 WRT REQ Total Counter OV Write request total counter overflow for DT0 If overflow bit is 1, the value of PMTR_DT0_WR_TOTAL_CNTR is meaningless.
12	PMTR_DT0_RD_TOTAL_CNTR_OVERFLOW	DT0 RD REQ Total Counter OV Read request total counter overflow for DT0 If overflow bit is 1, the value of PMTR_DT0_RD_TOTAL_CNTR is meaningless.
11	PMTR_DT0_WDT_TOTAL_CNTR_OVERFLOW	DT0 WRT Data Total Counter OV Write data total counter overflow for DT0 If overflow bit is 1, the value of PMTR_DT0_WDT_TOTAL_CNTR is meaningless.
10	PMTR_DT0_RDT_TOTAL_CNTR_OVERFLOW	DT0 RD Data Total Counter OV Read data total counter overflow for DT0 If overflow bit is 1, the value of PMTR_DT0_RDT_TOTAL_CNTR is meaningless.
9	PMTR_CNTI_MODE	PMTR_DT Continuous Mode Selection In one shot mode, PMTR_DT stop the measuring at the end of sampling period. PMTR_EN auto clear to 0 at interrupt. SW need to clear the interrupt, then set rg_pmtr_en again to 1 to restart PMTR_DT. In Continuous mode, PMTR_DT keep measuring the bus traffic and save the counter value at the end of each sampling period
8	PMTR_PT_MODE	PMTR_DT PT Mode Selection In pattern mode, PMTR_DTY stop the measuring at the end of sampling period or trigger address end mach. PMTR_EN auto clear to 0 at interrupt. SW need to clear the interrupt, then set rg_pmtr_en again to 1 to restart PMTR_DT. Note: PMTR_DT PT Mode is active only when One Shot Mode is enabled.
0	PMTR_EN	PMTR Enable Enable Bus Monitor function. If enabled, the measuring results are latched to registers at the end of each sampling period. When PMTR_EN from 0 -> 1, all counters are reset to 0

15004004	PMTR_PRD								Sampling period								00000001	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16		
Name									PMTR_PRD									
Type									RW									
Reset									0	0	0	0	0	0	0	0		
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
Name	PMTR_PRD																	
Type	RW																	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1		

Bit(s)	Name	Description
23:0	PMTR_PRD	PMTR Period Default period is 10us, 10us step incremental. Timer is clocked by 26MHz xtal clock

15004008 PMTR_INT Interrupt control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								PMTR_DLY_INT_EN								PMTR_INT_EN
Type								RW								RW
Reset								0								0

Bit(s)	Name	Description
8	PMTR_DLY_INT_EN	PMTR Delay Function Interrupt Enable Set 1 to enable delay function interrupt assertion upon the end of each sample period 0: Disable delay function Interrupt 1: Enable delay function interrupt
0	PMTR_INT_EN	PMTR Interrupt Enable Set 1 to enable interrupt assertion upon the end of each sample period

15004010 PMTR_DT0_MASTER_ID Request DT0 Master ID selection 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																PMTR_DT0_MASTER_ID
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PMTR_DT0_MASTER_ID															

Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16:0	PMTR_DT0_MASTER_ID	PMTR SFlash Master ID Select the master ID to be monitored

15004014 PMTR_DT0_MASTER_ID_MASK Request DT0 SRAM Master ID Mask 0001FFF0
K

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																PMTR_DT0_MASTER_ID_MASK
Type																RW
Reset																1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PMTR_DT0_MASTER_ID_MASK															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0

Bit(s)	Name	Description
16:0	PMTR_DT0_MASTER_ID_MASK	PMTR SFlash Master ID MASK Bits Set the master ID Mask bit for filtering

15004018 PMTR_DT1_MASTER_ID Request DT1 Master ID selection 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																PMTR_DT1_MASTER_ID
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	PMTR_DT1_MASTER_ID															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16:0	PMTR_DT1_MASTER_ID	PMTR SRAM Master ID Select the master ID to be monitored

1500401C PMTR_DT1_MASTER_ID_MASK Request DT1 SRAM Master ID Mask 0001FFFF
K

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																PMTR_DT1_MASTER_ID_MASK
Type																RW
Reset																1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PMTR_DT1_MASTER_ID_MASK															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0

Bit(s)	Name	Description
16:0	PMTR_DT1_MASTER_ID_MASK	PMTR SRAM Master ID MASK Bits Set the master ID Mask bit for filtering

15004080 PMTR_10U_PRD 10 us counter limit 00000104

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name								PMTR_10U_PRD								
Type								RW								
Reset								1	0	0	0	0	0	1	0	0

Bit(s)	Name	Description
8:0	PMTR_10U_PRD	PMTR 10us Period 10us timer counter, used to increment PMTR_CNTR. The value is determined by the 10us calculation from XTAL CK Freq :26Mhz

15004084 PMTR_SW_RST PMTR SW Reset 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																PMTR_SW_RESET
Type																W1C
Reset																0

Bit(s)	Name	Description
0	PMTR_SW_RESET	PMTR_TOP Software Reset Activate Set this bit to activate the PMTR_TOP includes PMTR_DT & PMTR_LTCY blocks, this is write once register. Hardware automatically clear this bit

15004088 PMTR_CLK_CON PMTR Clock Control 00000007

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name																	PMTR_AXI1_CK_EN	PMTR_AXI0_CK_EN	PMTR_XTAL_CK_EN
Type																	RW	RW	RW
Reset																	1	1	1

Bit(s)	Name	Description
2	PMTR_AXI1_CK_EN	AXI1 Clock Enable Enable PMTR_DT, PMTR_LTCY AXI1 clock
1	PMTR_AXI0_CK_EN	AXI0 Clock Enable Enable PMTR_DT, PMTR_LTCY AXI0 clock
0	PMTR_XTAL_CK_EN	XTAL Clock Enable Enable PMTR_DT, PMTR_LTCY XTAL clock

15004090 PMTR_INT_STA Interrupt Status 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								PMTR_TMR_HIT_FOR_DLY_CNT								PMTR_TMR_HIT
Type								RO								RO
Reset								0								0

Bit(s)	Name	Description
8	PMTR_TMR_HIT_FOR_DLY_CNT	PMTR Timer Delay Function Interrupt Hit Signaling that the Sampling period is up
0	PMTR_TMR_HIT	PMTR Timer Interrupt Hit Signaling that the Sampling period is up

15004094 PMTR_INT_CLR Interrupt Status clear 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																

Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								PMTR_INT_CLR_FOR_DLY_CNT								PMTR_INT_CLR
Type								W1C								W1C
Reset								0								0

Bit(s)	Name	Description
8	PMTR_INT_CLR_FOR_DLY_CNT	PMTR Timer Delay Function Interrupt Clear Set this bit to clear the PMTR_INT_STA_FOR_DLY_CNT status, this is write once register. Hardware automatically clear this bit
0	PMTR_INT_CLR	PMTR Timer Interrupt Clear Set this bit to clear the PMTR_INT_STA status, this is write once register. Hardware automatically clear this bit

15004120 PMTR_DT0_WR_CNTR DT0 WR REQ NUMBER 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PMTR_DT0_WR_CNTR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PMTR_DT0_WR_CNTR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	PMTR_DT0_WR_CNTR	PMTR SRAM Write Request Counter Number of Write request from specific master to SRAM (The maximum is 32'hffffff, which means overflow.)

15004124 PMTR_DT0_RD_CNTR DT0 RD REQ NUMBER 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PMTR_DT0_RD_CNTR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PMTR_DT0_RD_CNTR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	PMTR_DT0_RD_CNTR	PMTR SRAM Read Request Counter Number of read request from specific master to SRAM (The maximum is 32'hffffff, which means overflow.)

15004128 PMTR_DT0_WR_TOTAL_CNTRDT0 WR REQ TOTAL NUMBER 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PMTR_DT0_WR_TOTAL_CNTR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PMTR_DT0_WR_TOTAL_CNTR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	PMTR_DT0_WR_TOTAL_CNTR	PMTR SRAM Write Request Total Counter Number of Write request from all masters to SRAM (The maximum is 32'hffffff, which means overflow.)

1500412C PMTR_DT0_RD_TOTAL_CNTRDT0 RD REQ TOTAL NUMBER 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PMTR_DT0_RD_TOTAL_CNTR															

Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PMTR_DT0_RD_TOTAL_CNTR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	PMTR_DT0_RD_TOTAL_CNTR	PMTR SRAM Read Request Toal Counter Number of read request from all masters to SRAM (The maximum is 32'hffffff, which means overflow.)

15004130 **PMTR_DT0_WDT_CNTR** **DT0 WR DATA NUMBER** 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PMTR_DT0_WDT_CNTR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PMTR_DT0_WDT_CNTR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	PMTR_DT0_WDT_CNTR	PMTR SRAM Write Data Counter Number of Write data from specific master to SRAM (The maximum is 32'hffffff, which means overflow.)

15004134 **PMTR_DT0_RDT_CNTR** **DT0 RD DATA NUMBER** 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PMTR_DT0_RDT_CNTR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PMTR_DT0_RDT_CNTR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	PMTR_DT0_RDT_CNTR	PMTR SRAM Read Data Counter Number of read data from specific master to SRAM (The maximum is 32'hffffff, which means overflow.)

15004138 PMTR_DT0_WDT_TOTAL_CNT DT0 WR DATA TOTAL NUMBER 00000000
R

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PMTR_DT0_WDT_TOTAL_CNTR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PMTR_DT0_WDT_TOTAL_CNTR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	PMTR_DT0_WDT_TOTAL_CNTR	PMTR SRAM Write Data Total Counter Number of Write data from all masters to SRAM (The maximum is 32'hffffff, which means overflow.)

1500413C PMTR_DT0_RDT_TOTAL_CNT DT0 RD DATA TOTAL NUMBER 00000000
R

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PMTR_DT0_RDT_TOTAL_CNTR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	PMTR_DT0_RDT_TOTAL_CNTR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	PMTR_DT0_RDT_TOTAL_CNTR	PMTR SRAM Read Data Counter Number of read data from all masters to SRAM (The maximum is 32'hffffff, which means overflow.)

15004140 **PMTR_DT1_WR_CNTR** **DT1 WR REQ NUMBER** 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PMTR_DT1_WR_CNTR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PMTR_DT1_WR_CNTR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	PMTR_DT1_WR_CNTR	PMTR WIFI Write Request Counter Number of Write request from specific master to WIFI (The maximum is 32'hffffff, which means overflow.)

15004144 **PMTR_DT1_RD_CNTR** **DT1 RD REQ NUMBER** 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PMTR_DT1_RD_CNTR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PMTR_DT1_RD_CNTR															
Type	RO															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	PMTR_DT1_RD_CNTR	PMTR WIFI Read Request Counter Number of read request from specific master to WIFI (The maximum is 32'hfffffff, which means overflow.)

15004148 **PMTR_DT1_WR_TOTAL_CNTR** DT1 WR REQ TOTAL NUMBER 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PMTR_DT1_WR_TOTAL_CNTR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PMTR_DT1_WR_TOTAL_CNTR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	PMTR_DT1_WR_TOTAL_CNTR	PMTR WIFI Write Request Total Counter Number of Write request from all masters to WIFI (The maximum is 32'hfffffff, which means overflow.)

1500414C **PMTR_DT1_RD_TOTAL_CNTR** DT1 RD REQ TOTAL NUMBER 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PMTR_DT1_RD_TOTAL_CNTR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PMTR_DT1_RD_TOTAL_CNTR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	PMTR_DT1_RD_TOTAL_CNTR	PMTR WIFI Read Request Total Counter Number of read request from all masters to WIFI (The maximum is 32'hfffffff, which means overflow.)

15004150 **PMTR_DT1_WDT_CNTR** **DT1 WR DATA NUMBER** 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PMTR_DT1_WDT_CNTR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PMTR_DT1_WDT_CNTR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	PMTR_DT1_WDT_CNTR	PMTR WIFI Write Data Counter Number of Write data from specific master to WIFI (The maximum is 32'hfffffff, which means overflow.)

15004154 **PMTR_DT1_RDT_CNTR** **DT1 RD DATA NUMBER** 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PMTR_DT1_RDT_CNTR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PMTR_DT1_RDT_CNTR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	PMTR_DT1_RDT_CNTR	PMTR WIFI Read Data Counter Number of read data from specific master to WIFI (The maximum is 32'hfffffff, which means overflow.)

Bit(s)	Name	Description

15004158 **PMTR_DT1_WDT_TOTAL_CNTR** DT1 WR DATA TOTAL NUMBER 00000000
R

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PMTR_DT1_WDT_TOTAL_CNTR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PMTR_DT1_WDT_TOTAL_CNTR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	PMTR_DT1_WDT_TOTAL_CNTR	PMTR WIFI Write Data Total Counter Number of Write data from all masters to WIFI (The maximum is 32'hffffff, which means overflow.)

1500415C **PMTR_DT1_RDT_TOTAL_CNTR** DT1 RD DATA TOTAL NUMBER 00000000
R

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PMTR_DT1_RDT_TOTAL_CNTR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PMTR_DT1_RDT_TOTAL_CNTR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	PMTR_DT1_RDT_TOTAL_CNTR	PMTR WIFI Read Data Total Counter Number of read data from all masters to WIFI (The maximum is 32'hffffff, which means overflow.)

15004200 PMTR_DLY_PRD Delay function counter period 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									PMTR_DELAY_FUNCTION_PRD							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PMTR_DELAY_FUNCTION_PRD															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
23:0	PMTR_DELAY_FUNCTION_PRD	Delay Timer Period Default value is 10us. 10us step incremental.

15004204 PMTR_PT_SLAVE_SEL PMTR Pattern Mode Request Target selection 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														PMTR_PT_SLAVE_SEL		
Type														RW		
Reset														0	0	0

Bit(s)	Name	Description
2:0	PMTR_PT_SLAVE_SEL	PMTR Pattern Mode Slave SEL Select which slave target to be monitored

15004208 PMTR_PT_ADDR_BEG PMTR Pattern Mode Request Trigger Begin Address 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	PMTR_PT_ADDR_BEG															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PMTR_PT_ADDR_BEG															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	PMTR_PT_ADDR_BEG	PMTR_DT Trigger Address Begin Trigger to start monitoring

1500420C PMTR_PT_ADDR_END PMTR Pattern Mode Request Trigger End Address FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PMTR_PT_ADDR_END															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PMTR_PT_ADDR_END															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:0	PMTR_PT_ADDR_END	PMTR_DT Trigger Address End Trigger to stop monitoring

15004210 PMTR_PT_PRD_ST PMTR Pattern Mode Sampling period counter status 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									PMTR_PT_PRD_ST							
Type									RO							

Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PMTR_PT_PRD_ST															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
23:0	PMTR_PT_PRD_ST	PMTR Pattern Mode Period counter status Default period is 10us, 10us step incremental. Timer is clocked by 26MHz xtal clock

15004214 PMTR_PT_10U_PRD_ST PMTR Pattern Mode 10 us counter status 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								PMTR_10U_PRD_ST								
Type								RO								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
8:0	PMTR_10U_PRD_ST	PMTR Pattern Mode 10us Period counter status 10us timer counter, used to increment PMTR_CNTR. The value is determined by the 10us calculation from XTAL CK Freq :26Mhz

15004800 LTCY_MAIN_CTL LTCY Main control and overflow 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	LTCY_DLY_EN															
Type	RW															
Reset	0															

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						LTCY1_TOTAL_WR_LATENCY_OVERFLOW	LTCY1_TOTAL_RD_LATENCY_OVERFLOW	LTCY0_TOTAL_WR_LATENCY_OVERFLOW	LTCY0_TOTAL_RD_LATENCY_OVERFLOW	LTCY1_WR_REQ_OVERFLOW	LTCY1_RD_REQ_OVERFLOW	LTCY0_WR_REQ_OVERFLOW	LTCY0_RD_REQ_OVERFLOW	LTCY_CNTI_MODE	LTCY_PT_MODE	LTCY_EN
Type						RO	RO	RO	RO	RO	RO	RO	RO	RW	RW	RW
Reset						0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	LTCY_DLY_EN	LTCY Delay Function Enable delay function counter enable 0: Enable LTCY when rg_ltcy_en_pre =1 1: enable LTCY when rg_ltcy_en_pre = 1 and delay counter expired
10	LTCY1_TOTAL_WR_LATENCY_OVERFLOW	LTCY3 Total Latency Cycles OV Total latency counter cycles overflow for Latency 3 If overflow bit is 1, the value of LTCY3_TOTAL_CNTR is meaningless.
9	LTCY1_TOTAL_RD_LATENCY_OVERFLOW	LTCY2 Total Latency Cycles OV Total latency counter cycles overflow for Latency 2 If overflow bit is 1, the value of LTCY2_TOTAL_CNTR is meaningless.
8	LTCY0_TOTAL_WR_LATENCY_OVERFLOW	LTCY1 Total Latency Cycles OV Total latency counter cycles overflow for Latency 1 If overflow bit is 1, the value of LTCY1_TOTAL_CNTR is meaningless.
7	LTCY0_TOTAL_RD_LATENCY_OVERFLOW	LTCY0 Total Latency Cycles OV Total latency counter cycles overflow for Latency 0 If overflow bit is 1, the value of LTCY_TOTAL_CNTR is meaningless.
6	LTCY1_WR_REQ_OVERFLOW	LTCY3 Total REQ OV Total request counter overflow for Latency 3 If overflow bit is 1, the value of LTCY3_TOTAL_REQ_CNTR is meaningless.
5	LTCY1_RD_REQ_OVERFLOW	LTCY2 Total REQ OV Total request counter overflow for Latency 2 If overflow bit is 1, the value of LTCY2_TOTAL_REQ_CNTR is meaningless.
4	LTCY0_WR_REQ_OVERFLOW	LTCY1 Total REQ OV Total request counter overflow for Latency 1 If overflow bit is 1, the value of LTCY1_TOTAL_REQ_CNTR is meaningless.
3	LTCY0_RD_REQ_OVERFLOW	LTCY0 Total REQ OV Total request counter overflow for Latency 0 If overflow bit is 1, the value of LTCY0_TOTAL_REQ_CNTR is meaningless.
2	LTCY_CNTI_MODE	PMTR_LTCY Continuous Mode Selection In one shot mode, PMTR_LTCY stop the measuring at the end of sampling period. LTCY_EN auto clear to 0 at interrupt. SW need to clear the interrupt, then set rg_pmtr_en again to 1 to restart PMTR_LTCY. In Continuous mode, PMTR_LTCY keep measuring the bus traffic and save the counter value at the end of each sampling period
1	LTCY_PT_MODE	PMTR_LTCY PT Mode Selection In pattern mode, PMTR_LTCY stop the measuring at the end of sampling period or trigger address end mach . LTCY_EN auto clear to 0 at interrupt. SW need to clear the interrupt, then set rg_pmtr_en again to 1 to restart PMTR_LTCY. Note: LTCY PT Mode is active only when One Shot Mode is enabled.

Bit(s)	Name	Description
0	LTCY_EN	LTCY Enable Enable Bus Monitor function. If enabled, the measuring results are latched to registers at the end of each sampling period. When LTCY_EN from 0 -> 1, all counters are reset to 0

15004804 **LTCY_PRD** **LTCY Sampling period** **00000001**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									LTCY_PRD							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LTCY_PRD															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
23:0	LTCY_PRD	LTCY Period Default period is 10us, 10us step incremental. Timer is clocked by 26MHz xtal clock

15004808 **LTCY_INT** **LTCY Interrupt control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								LTCY_DLY_INT_EN								LTCY_INT_EN
Type								RW								RW
Reset								0								0

Bit(s)	Name	Description
8	LTCY_DLY_INT_EN	PMTR Delay Function Interrupt Enable Set 1 to enable delay function interrupt assertion upon the end of each sample period 0: Disable delay function Interrupt 1: Enable delay function interrupt
0	LTCY_INT_EN	LTCY Interrupt Enable Set 1 to enable interrupt assertion upon the end of each sample period

15004830 **LTCY0_ADDR_FILTER_BEG** LTCY0 Request Target Begin Address selection 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	LTCY0_ADDR_FILTER_BEG															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LTCY0_ADDR_FILTER_BEG															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	LTCY0_ADDR_FILTER_BEG	LTCY0 Address Filter Begin Select which target to be monitored

15004834 **LTCY0_ADDR_FILTER_END** LTCY0 Request Target End Address selection FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	LTCY0_ADDR_FILTER_END															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LTCY0_ADDR_FILTER_END															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:0	LTCY0_ADDR_FILTER_END	LTCY0 Address Filter End Select which target to be monitored

15004838 **LTCY1_ADDR_FILTER_BEG** LTCY1 Request Target Begin Address selection 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	LTCY1_ADDR_FILTER_BEG															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LTCY1_ADDR_FILTER_BEG															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	LTCY1_ADDR_FILTER_BEG	LTCY1 Address Filter Begin Select which target to be monitored

1500483C **LTCY1_ADDR_FILTER_END** LTCY1 Request Target End Address selection FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	LTCY1_ADDR_FILTER_END															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LTCY1_ADDR_FILTER_END															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:0	LTCY1_ADDR_FILTER_END	LTCY1 Address Filter End Select which target to be monitored

15004880 **LTCY_10U_PRD** LTCY 10 us counter limit 00000104

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								LTCY_10U_PRD								
Type								RW								
Reset								1	0	0	0	0	0	1	0	0

Bit(s)	Name	Description
8:0	LTCY_10U_PRD	LTCY 10us Period 10us timer counter, used to increment LTCY_CNTR. The value is determined by the 10us calculation from XTAL CK Freq :26Mhz

15004890 **LTCY_INT_STA** LTCY Interrupt Status 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								LTCY_TMR_HIT_FOR_DLY_CNT								LTCY_TMR_HIT
Type								RO								RO
Reset								0								0

Bit(s)	Name	Description
8	LTCY_TMR_HIT_FOR_DLY_CNT	LTCY Timer Delay Function Interrupt Hit Signaling that the Sampling period is up
0	LTCY_TMR_HIT	LTCY Timer Interrupt Hit Signaling that the Sampling period is up

15004894 **LTCY_INT_CLR** LTCY Interrupt Status clear 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								LTCY_INT_CLR_FOR_DLY_CNT								LTCY_INT_CLR
Type								W1C								W1C
Reset								0								0

Bit(s)	Name	Description
8	LTCY_INT_CLR_FOR_DLY_CNT	LTCY Timer Delay Function Interrupt Clear Set this bit to clear the LTCY_INT_STA_FOR_DLY_CNT status, this is write once register. Hardware automatically clear this bit
0	LTCY_INT_CLR	LTCY Timer Interrupt Clear Set this bit to clear the LTCY_INT_STA status, this is write once register. Hardware automatically clear this bit

150048A0 **LTCY0_MASTER_ID** LTCY0 Master ID selection 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																LTCY0_MASTER_ID
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LTCY0_MASTER_ID															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16:0	LTCY0_MASTER_ID	LTCY0 Master ID Select the master ID to be monitored

150048A4 LTCY0_MASTER_ID_MASK LTCY0 Master ID Mask 0001FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																LTCY0_MASTER_ID_MASK
Type																RW
Reset																1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LTCY0_MASTER_ID_MASK															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
16:0	LTCY0_MASTER_ID_MASK	LTCY0 Master ID MASK Bits Set the master ID Mask bit for filtering

150048A8 LTCY1_MASTER_ID LTCY1 Master ID selection 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																LTCY1_MASTER_ID
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LTCY1_MASTER_ID															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16:0	LTCY1_MASTER_ID	LTCY1 Master ID Select the master ID to be monitored

150048AC LTCY1_MASTER_ID_MASK LTCY1 Master ID Mask 0001FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																LTCY1_MASTER_ID_MASK
Type																RW
Reset																1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LTCY1_MASTER_ID_MASK															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
16:0	LTCY1_MASTER_ID_MASK	LTCY1 Master ID MASK Bits Set the master ID Mask bit for filtering

15004900 LTCY0_WR_REQ_CNTR LTCY0 Write Request Number 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	LTCY0_WR_REQ_CNTR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LTCY0_WR_REQ_CNTR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	LTCY0_WR_REQ_CNTR	LTCY0 Total REQ Counter Number of total request

Bit(s)	Name	Description
		(The maximum is 32'hfffffff, which means overflow.)

15004904 LTCY0_RD_REQ_CNTR LTCY0 Read Request Number 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	LTCY0_RD_REQ_CNTR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LTCY0_RD_REQ_CNTR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	LTCY0_RD_REQ_CNTR	LTCY0 Total REQ Counter Number of total request (The maximum is 32'hfffffff, which means overflow.)

15004908 LTCY0_MIN_WR_CYCLE LTCY0 Minimum Write latency cycles 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	LTCY0_MIN_WR_CYCLE															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LTCY0_MIN_WR_CYCLE															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	LTCY0_MIN_WR_CYCLE	LTCY0 Minimum Latency Cycles Counter Number of latency cycles (The maximum is 16'hfff, which means overflow.)

1500490C LTCY0_MIN_RD_CYCLE LTCY0 Minimum Read latency cycles 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	LTCY0_MIN_RD_CYCLE															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LTCY0_MIN_RD_CYCLE															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	LTCY0_MIN_RD_CYCLE	LTCY0 Minimum Latency Cycles Counter Number of latency cycles (The maximum is 16'hffff, which means overflow.)

15004910 LTCY0_MAX_WR_CYCLE LTCY0 Maximum Write latency cycles 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	LTCY0_MAX_WR_CYCLE															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LTCY0_MAX_WR_CYCLE															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	LTCY0_MAX_WR_CYCLE	LTCY0 Maximum Latency Cycles Counter Number of latency cycles (The maximum is 16'hffff, which means overflow.)

15004914 LTCY0_MAX_RD_CYCLE LTCY0 Maximum Read latency cycles 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	LTCY0_MAX_RD_CYCLE															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LTCY0_MAX_RD_CYCLE															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	LTCY0_MAX_RD_CYCLE	LTCY0 Maximum Latency Cycles Counter Number of latency cycles (The maximum is 16'hffff, which means overflow.)

15004918 **LTCY0_MAX_OST_WR_COUNT** LTCY0 Maximum OST Write Count 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	LTCY0_MAX_OST_WR_COUNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LTCY0_MAX_OST_WR_COUNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	LTCY0_MAX_OST_WR_COUNT	LTCY0 Total Latency Cycles Counter Number of latency cycles (The maximum is 32'hfffffff, which means overflow.)

1500491C **LTCY0_MAX_OST_RD_COUNT** LTCY0 Maximum OST Read Count 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	LTCY0_MAX_OST_RD_COUNT															
Type	RO															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LTCY0_MAX_OST_RD_COUNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	LTCY0_MAX_OST_RD_COUNT	LTCY0 Total Latency Cycles Counter Number of latency cycles (The maximum is 32'hffffff, which means overflow.)

15004920 LTCY1_WR_REQ_CNTR LTCY1 Write Request Number 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	LTCY1_WR_REQ_CNTR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LTCY1_WR_REQ_CNTR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	LTCY1_WR_REQ_CNTR	LTCY1 Total REQ Counter Number of total request (The maximum is 32'hffffff, which means overflow.)

15004924 LTCY1_RD_REQ_CNTR LTCY1 Read Request Number 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	LTCY1_RD_REQ_CNTR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	LTCY1_RD_REQ_CNTR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	LTCY1_RD_REQ_CNTR	LTCY1 Total REQ Counter Number of total request (The maximum is 32'hffffff, which means overflow.)

15004928 LTCY1_MIN_WR_CYCLE LTCY1 Minimum Write latency cycles 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	LTCY1_MIN_WR_CYCLE															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LTCY1_MIN_WR_CYCLE															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	LTCY1_MIN_WR_CYCLE	LTCY1 Minimum Latency Cycles Counter Number of latency cycles (The maximum is 16'hfff, which means overflow.)

1500492C LTCY1_MIN_RD_CYCLE LTCY1 Minimum Read latency cycles 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	LTCY1_MIN_RD_CYCLE															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LTCY1_MIN_RD_CYCLE															
Type	RO															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	LTCY1_MIN_RD_CYCLE	LTCY1 Minimum Latency Cycles Counter Number of latency cycles (The maximum is 16'hffff, which means overflow.)

15004930 **LTCY1_MAX_WR_CYCLE** LTCY1 Maximum Write latency cycles 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	LTCY1_MAX_WR_CYCLE															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LTCY1_MAX_WR_CYCLE															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	LTCY1_MAX_WR_CYCLE	LTCY1 Maximum Latency Cycles Counter Number of latency cycles (The maximum is 16'hffff, which means overflow.)

15004934 **LTCY1_MAX_RD_CYCLE** LTCY1 Maximum Read latency cycles 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	LTCY1_MAX_RD_CYCLE															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LTCY1_MAX_RD_CYCLE															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	LTCY1_MAX_RD_CYCLE	LTCY1 Maximum Latency Cycles Counter Number of latency cycles (The maximum is 16'hffff, which means overflow.)

15004938 LTCY1_MAX_OST_WR_COUNT LTCY1 Maximum OST Write Count 00000000

I

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	LTCY1_MAX_OST_WR_COUNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LTCY1_MAX_OST_WR_COUNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	LTCY1_MAX_OST_WR_COUNT	LTCY1 Total Latency Cycles Counter Number of latency cycles (The maximum is 32'hfffffff, which means overflow.)

1500493C LTCY1_MAX_OST_RD_COUNT LTCY1 Maximum OST Read Count 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	LTCY1_MAX_OST_RD_COUNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LTCY1_MAX_OST_RD_COUNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	LTCY1_MAX_OST_RD_COUNT	LTCY1 Total Latency Cycles Counter Number of latency cycles

Bit(s)	Name	Description
		(The maximum is 32'hffffff, which means overflow.)

15004A00 LTCY_DLY_PRD LTCY Delay function counter period 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									LTCY_DELAY_FUNCTION_PRD							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LTCY_DELAY_FUNCTION_PRD															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
23:0	LTCY_DELAY_FUNCTION_PRD	LTCY Delay Timer Period Default value is 10us. 10us step incremental.

15004A04 LTCY_PT_MASTER_SEL LTCY Pattern Mode Master selection 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													LTCY_PT_MASTER_SEL			
Type													RW			
Reset													0	0	0	0

Bit(s)	Name	Description
3:0	LTCY_PT_MASTER_SEL	LTCY Master source SEL Select which master source to be monitored

15004A08 LTCY_PT_ADDR_BEG

LTCY Pattern Mode Request Trigger Begin
Address

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	LTCY_PT_ADDR_BEG															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LTCY_PT_ADDR_BEG															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	LTCY_PT_ADDR_BEG	PMTR_LTCY Trigger Address Begin Trigger to start monitoring

15004A0C LTCY_PT_ADDR_END

LTCY Pattern Mode Request Trigger End Address

FFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	LTCY_PT_ADDR_END															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LTCY_PT_ADDR_END															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:0	LTCY_PT_ADDR_END	PMTR_LTCY Trigger Address End Trigger to stop monitoring

15004A10 LTCY_PT_PRD_ST

LTCY Pattern Mode Sampling period counter
status

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name									LTCY_PT_PRD_ST							
Type									RO							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LTCY_PT_PRD_ST															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
23:0	LTCY_PT_PRD_ST	LTCY Pattern Mode Period counter status Default period is 10us, 10us step incremental. Timer is clocked by 26MHz xtal clock

15004A14 LTCY_PT_10U_PRD_ST LTCY Pattern Mode 10 us counter status 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								LTCY_10U_PRD_ST								
Type								RO								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
8:0	LTCY_10U_PRD_ST	LTCY Pattern Mode 10us Period counter status 10us timer counter, used to increment LTCY_CNTR. The value is determined by the 10us calculation from XTAL CK Freq :26Mhz

15100000 FE_GLO_CFG Frame Engine Global Configuration 810000B0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EXT_TPID															
Type	RW															

Reset	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LINK_DWN_0								L2_SPACE				INF_SPACE			
Type	RW								RW				RW			
Reset	0	0	0	0	0	0	0	0	1	0	1	1	0	0	0	0

Bit(s)	Name	Description
31:16	EXT_TPID	Extended VLAN TPID User-defined TPID except for 0x8100, 0x88a8. [note] This TPID field is used by CDM/GDM RX direction.
15:8	LINK_DWN_0	Disable PSE Port 0~7 When PSE port is not valid on the Frame Engine, user is suggested to disable the corresponding port.
7:4	L2_SPACE	L2 space The space unit is 8 bytes.
3:0	INF_SPACE	PKT_INFO space The space unit is 8 bytes. [Note1*] Per received packet has already occupied 8 bytes (1 unit) by default. The actual PKT_INFO space is equal to (INF_SPACE + 1) [Note2*] (L2_SPACE + INF_SPACE + 1) <= 0xF

15100004 FE_RST_GLO Frame Engine Global Reset 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RESVO															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESVO													PSE_RAM	PSE_MEM_EN	PSE_RESET
Type	RO													RW	RW	W1S
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:3	RESVO	Reserved
2	PSE_RAM	PSE accessible RAM mode [note*1] when this bit is reset, PSE packet memory is only accessible by Pbus (0xA000~0xDFFF). [note*2] when this bit is set, PSE packet memory is only accessible by Pbus (0x8000~0xDFFF)
1	PSE_MEM_EN	PSE access enable

Bit(s)	Name	Description
0	PSE_RESET	PSE soft reset (self-cleared) [note*1] Whenever SW set this bit, PSE will be initialized again and enter the normal mode.

15100008 FE_INT_STATUS Frame Engine Interrupt Status 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PPE_AF	REV0	GDM2_AF	GDM1_AF	GDM2_DOS_LIMIT	GDM1_DOS_LIMIT	MAC2_LINK	MAC1_LINK	GDM2_ERR	GDM2_CRC	GDM1_ERR	GDM1_CRC	RFIFO_UF	RFIFO_OV	INFIFO_GET_ERR	AFIFO_GET_ERR
Type	W1C	RO	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV2	CDM_TSO_ALIGN	CDM_TSO_ILLEGAL	CDM_TSO_FAIL	REV3		PSE_DROP	FQ_EMPTY	PSE_FC_ON_0							
Type	RO	W1C	W1C	W1C	RO		W1C	W1C	W1C							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	PPE_AF	MIB counter is almost full on PPE
30	REV0	Reserved
29	GDM2_AF	MIB counter is almost full on GDM2
28	GDM1_AF	MIB counter is almost full on GDM1
27	GDM2_DOS_LIMIT	Packet rate is reached (TCP SYN, UDP, ICMP) on GDM2
26	GDM1_DOS_LIMIT	Packet rate is reached (TCP SYN, UDP, ICMP) on GDM1
25	MAC2_LINK	Link Status Change on MAC2
24	MAC1_LINK	Link Status Change on MAC1
23	GDM2_ERR	Packet error (checksum, length, etc.) on GDM2 Including FIFO overflow, checksum error, undersize, oversize
22	GDM2_CRC	Packet CRC error on GDM2
21	GDM1_ERR	Packet error (checksum, length, etc.) on GDM1 Including FIFO overflow, checksum error, undersize, oversize
20	GDM1_CRC	Packet CRC error on GDM1
19	RFIFO_UF	Ring FIFO Underrun Defect
18	RFIFO_OV	Ring FIFO Overflow Defect
17	INFIFO_GET_ERR	IN FIFO Get Defect
16	AFIFO_GET_ERR	ASYNCFIFO Get Defect
15	REV2	Reserved
14	CDM_TSO_ALIGN	Detect EOF Alignment
13	CDM_TSO_ILLEGAL	Ignored illegal packet on CDM TSO
12	CDM_TSO_FAIL	TSO Fail on CDM
11:10	REV3	Reserved
9	PSE_DROP	Packet drop by PSE
8	FQ_EMPTY	PSE free queue is empty

Bit(s)	Name	Description
7:0	PSE_FC_ON_0	PSE PORT flow control is asserted PSE port[n] enables the flow control.

1510000C FE INT ENABLE Frame Engine Interrupt Enable 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PPE_AF	REV0	GDM2_AF	GDM1_AF	GDM2_DOS_LIMIT	GDM1_DOS_LIMIT	MAC2_LINK	MAC1_LINK	GDM2_ERR	GDM2_CRC	GDM1_ERR	GDM1_CRC	RFIFO_UF	RFIFO_OV	INFIFO_GET_ERR	AFIFO_GET_ERR
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV2	CDM_TSO_ALIGN	CDM_TSO_ILLEGAL	CDM_TSO_FAIL	REV3		PSE_DROP	FQ_EMPTY	PSE_FC_ON_0							
Type	RW	RW	RW	RW	RW		RW	RW	RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	PPE_AF	
30	REV0	
29	GDM2_AF	
28	GDM1_AF	
27	GDM2_DOS_LIMIT	
26	GDM1_DOS_LIMIT	
25	MAC2_LINK	
24	MAC1_LINK	
23	GDM2_ERR	
22	GDM2_CRC	
21	GDM1_ERR	
20	GDM1_CRC	
19	RFIFO_UF	
18	RFIFO_OV	
17	INFIFO_GET_ERR	
16	AFIFO_GET_ERR	
15	REV2	
14	CDM_TSO_ALIGN	
13	CDM_TSO_ILLEGAL	
12	CDM_TSO_FAIL	
11:10	REV3	
9	PSE_DROP	
8	FQ_EMPTY	
7:0	PSE_FC_ON_0	

15100010 FE_FOE_TS_T Frame Engine Time Stamp 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RESV0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FOE_TS_T															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	RESV0	Reserved
15:0	FOE_TS_T	Time stamp Time stamp unit is 1 sec. [Note] This timer is driven by free-running 125MHz clock

15100014 FE_IPV6_EXT Frame Engine IPv6 Extension Header 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	IP6_EXT3								IP6_EXT2							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IP6_EXT1								IP6_EXT0							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	IP6_EXT3	IPv6 extension header #3
23:16	IP6_EXT2	IPv6 extension header #2
15:8	IP6_EXT1	IPv6 extension header #1
7:0	IP6_EXT0	IPv6 extension header #0

15100018 FE_RATE_COMP Frame Engine Rate Limit Compensation 00001818

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REVO															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DMA_RATE_MINUS	DMA_RATE_BYTE							PSE_RATE_MINUS	PSE_RATE_BYTE						
Type	RW	RW							RW	RW						
Reset	0	0	0	1	1	0	0	0	0	0	0	1	1	0	0	0

Bit(s)	Name	Description
31:16	REVO	Reserved
15	DMA_RATE_MINUS	
14:8	DMA_RATE_BYTE	Byte number for rate control The byte number should be subtracted while calculating the rate limit.
7	PSE_RATE_MINUS	
6:0	PSE_RATE_BYTE	Byte number for rate control The byte number should be subtracted while calculating the rate limit.

1510001C LRO_ALT_REFRESH_TIMER Reserved 000FFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

15100020 FE_INT_GRP Frame Engine Interrupt Group 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_INT_G2_ASG				QDMA_INT_G1_ASG				QDMA_INT_G0_ASG				PDMA_INT_G2_ASG			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PDMA_INT_G1_ASG				PDMA_INT_G0_ASG				PDMA_INT_G3_ASG				FE_MISC_INT_ASG			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:28	QDMA_INT_G2_ASG	QDMA group 2 interrupt assignment
27:24	QDMA_INT_G1_ASG	QDMA group 1 interrupt assignment
23:20	QDMA_INT_G0_ASG	QDMA group 0 interrupt assignment
19:16	PDMA_INT_G2_ASG	PDMA group 2 interrupt assignment
15:12	PDMA_INT_G1_ASG	PDMA group 1 interrupt assignment
11:8	PDMA_INT_G0_ASG	PDMA group 0 interrupt assignment
7:4	PDMA_INT_G3_ASG	PDMA group 3 interrupt assignment
3:0	FE_MISC_INT_ASG	Frame engine misc. interrupt assignment

15100024 FE_GLO_CFG2 Frame Engine Global Configuration part2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										LINK_DWN_1						
Type										RW						
Reset										0	0	0	0	0	0	0

Bit(s)	Name	Description
6:0	LINK_DWN_1	Disable PSE Port 8~14 When PSE port is not valid on the Frame Engine, user is suggested to disable the corresponding port.

15100028 FE_INT_STATUS2 Frame Engine Interrupt Status part2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										PSE_FC_ON_1						
Type										W1C						
Reset										0	0	0	0	0	0	0

Bit(s)	Name	Description
6:0	PSE_FC_ON_1	PSE PORT flow control is asserted PSE port[n] enables the flow control.

1510002C FE_INT_ENABLE2 Frame Engine Interrupt Enable part2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										PSE_FC_ON_1						
Type										RW						
Reset										0	0	0	0	0	0	0

Bit(s)	Name	Description
6:0	PSE_FC_ON_1	

15100100 PSE_FQFC_CFG1 PSE Free Queue Flow Control part1 01FF01FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								FQ_PCNT								

Type								RO								
Reset								1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								FQ_MAX_PCNT								
Type								RW								
Reset								1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
24:16	FQ_PCNT	Free queue page count
8:0	FQ_MAX_PCNT	Maximum free Q page count.
Please reset PSE after re-programming this register		

15100104 PSE FQFC CFG2 PSE Free Queue Flow Control part2 012000E0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									FQ_HIGH							
Type									RW							
Reset								1	0	0	1	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									FQ_LOW							
Type									RW							
Reset								0	1	1	1	0	0	0	0	0

Bit(s)	Name	Description
24:16	FQ_HIGH	High threshold to release FC
8:0	FQ_LOW	Low threshold to trigger FC

15100110 PSE PPE0 DROP PPE0 drop packet enable port 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REVO															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REVO	PPE0_DROP_P14_EN	PPE0_DROP_P13_EN	PPE0_DROP_P12_EN	PPE0_DROP_P11_EN	PPE0_DROP_P10_EN	PPE0_DROP_P9_EN	PPE0_DROP_P8_EN	PPE0_DROP_P7_EN	PPE0_DROP_P6_EN	PPE0_DROP_P5_EN	PPE0_DROP_P4_EN	PPE0_DROP_P3_EN	PPE0_DROP_P2_EN	PPE0_DROP_P1_EN	PPE0_DROP_P0_EN
Type	RO	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:15	REVO	Reserved
14	PPE0_DROP_P14_EN	Enable PPE0 drop packet to port 14 due to RX ring full
13	PPE0_DROP_P13_EN	Enable PPE0 drop packet to port 13 due to RX ring full
12	PPE0_DROP_P12_EN	Enable PPE0 drop packet to port 12 due to RX ring full
11	PPE0_DROP_P11_EN	Enable PPE0 drop packet to port 11 due to RX ring full
10	PPE0_DROP_P10_EN	Enable PPE0 drop packet to port 10 due to RX ring full
9	PPE0_DROP_P9_EN	Enable PPE0 drop packet to port 9 due to RX ring full
8	PPE0_DROP_P8_EN	Enable PPE0 drop packet to port 8 due to RX ring full
7	PPE0_DROP_P7_EN	Enable PPE0 drop packet to port 7 due to RX ring full
6	PPE0_DROP_P6_EN	Enable PPE0 drop packet to port 6 due to RX ring full
5	PPE0_DROP_P5_EN	Enable PPE0 drop packet to port 5 due to RX ring full
4	PPE0_DROP_P4_EN	Enable PPE0 drop packet to port 4 due to RX ring full
3	PPE0_DROP_P3_EN	Enable PPE0 drop packet to port 3 due to RX ring full
2	PPE0_DROP_P2_EN	Enable PPE0 drop packet to port 2 due to RX ring full
1	PPE0_DROP_P1_EN	Enable PPE0 drop packet to port 1 due to RX ring full
0	PPE0_DROP_P0_EN	Enable PPE0 drop packet to port 0 due to RX ring full

15100114 PSE_PPE1_DROP PPE1 drop packet enable port 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REVO															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REVO	PPE1_DROP_P14_EN	PPE1_DROP_P13_EN	PPE1_DROP_P12_EN	PPE1_DROP_P11_EN	PPE1_DROP_P10_EN	PPE1_DROP_P9_EN	PPE1_DROP_P8_EN	PPE1_DROP_P7_EN	PPE1_DROP_P6_EN	PPE1_DROP_P5_EN	PPE1_DROP_P4_EN	PPE1_DROP_P3_EN	PPE1_DROP_P2_EN	PPE1_DROP_P1_EN	PPE1_DROP_P0_EN
Type	RO	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:15	REVO	Reserved
14	PPE1_DROP_P14_EN	Enable PPE1 drop packet to port 14 due to RX ring full
13	PPE1_DROP_P13_EN	Enable PPE1 drop packet to port 13 due to RX ring full

Bit(s)	Name	Description
12	PPE1_DROP_P12_EN	Enable PPE1 drop packet to port 12 due to RX ring full
11	PPE1_DROP_P11_EN	Enable PPE1 drop packet to port 11 due to RX ring full
10	PPE1_DROP_P10_EN	Enable PPE1 drop packet to port 10 due to RX ring full
9	PPE1_DROP_P9_EN	Enable PPE1 drop packet to port 9 due to RX ring full
8	PPE1_DROP_P8_EN	Enable PPE1 drop packet to port 8 due to RX ring full
7	PPE1_DROP_P7_EN	Enable PPE1 drop packet to port 7 due to RX ring full
6	PPE1_DROP_P6_EN	Enable PPE1 drop packet to port 6 due to RX ring full
5	PPE1_DROP_P5_EN	Enable PPE1 drop packet to port 5 due to RX ring full
4	PPE1_DROP_P4_EN	Enable PPE1 drop packet to port 4 due to RX ring full
3	PPE1_DROP_P3_EN	Enable PPE1 drop packet to port 3 due to RX ring full
2	PPE1_DROP_P2_EN	Enable PPE1 drop packet to port 2 due to RX ring full
1	PPE1_DROP_P1_EN	Enable PPE1 drop packet to port 1 due to RX ring full
0	PPE1_DROP_P0_EN	Enable PPE1 drop packet to port 0 due to RX ring full

15100124 FE_GLO_MISC PSE_PATCH 8000C406

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				MODEM_MSS_CR_SEL	MODEM_MSS_CR_VAL											
Type				RW	RW											
Reset				0	0	0	0	0	0	0	0	0	0	0	0	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			REV1		REV2		REV3									
Type			RW		RW		RW									
Reset			0		0		0									

Bit(s)	Name	Description
28	MODEM_MSS_CR_SEL	Selection for modem's MSS value from CR or packet's TCP checksum field
27:17	MODEM_MSS_CR_VAL	Modem's MSS CR value when MODEM_MSS_CR_SEL = 1
13	REV1	Reserved
11	REV2	Reserved
9	REV3	Reserved

15100130 FE_GDM_RXID1 FE_GDM_RXID Control 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GDM_VLAN_P R17_RXID_SEL	GDM_VLAN_P R16_RXID_SEL	GDM_VLAN_P R15_RXID_SEL	GDM_VLAN_P R14_RXID_SEL	GDM_VLAN_P R13_RXID_SEL	GDM_VLAN_P R12_RXID_SEL	GDM_VLAN_P R11_RXID_SEL	GDM_VLAN_P R10_RXID_SEL	GDM_VLAN_P R9_RXID_SEL	GDM_VLAN_P R8_RXID_SEL	GDM_VLAN_P R7_RXID_SEL	GDM_VLAN_P R6_RXID_SEL	GDM_VLAN_P R5_RXID_SEL	GDM_VLAN_P R4_RXID_SEL	GDM_VLAN_P R3_RXID_SEL	GDM_VLAN_P R2_RXID_SEL

Type	RW		RW		RW		RW		RW		RW		RW		RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											GDM_TCP_ACK_RXID_SEL		GDM_TCP_ACK_WZPC	GDM_RXID_PRI_SEL		
Type											RW		RW	RW		
Reset											0	0	0	0	0	0

Bit(s)	Name	Description
31:30	GDM_VLAN_PRI7_RXID_SEL	GDM RXID Select for VLAN Priority = 7
29:28	GDM_VLAN_PRI6_RXID_SEL	GDM RXID Select for VLAN Priority = 6
27:26	GDM_VLAN_PRI5_RXID_SEL	GDM RXID Select for VLAN Priority = 5
25:24	GDM_VLAN_PRI4_RXID_SEL	GDM RXID Select for VLAN Priority = 4
23:22	GDM_VLAN_PRI3_RXID_SEL	GDM RXID Select for VLAN Priority = 3
21:20	GDM_VLAN_PRI2_RXID_SEL	GDM RXID Select for VLAN Priority = 2
19:18	GDM_VLAN_PRI1_RXID_SEL	GDM RXID Select for VLAN Priority = 1
17:16	GDM_VLAN_PRI0_RXID_SEL	GDM RXID Select for VLAN Priority = 0
5:4	GDM_TCP_ACK_RXID_SEL	GDM RXID Select for TCP ACK
3	GDM_TCP_ACK_WZPC	GDM TCP ACK with zero payload check (L3 payload = L4 header)
2:0	GDM_RXID_PRI_SEL	GDM RXID Select Priority Setting
		Select Priority by PID/STAG, VLAN_PRI, and TCP_ACK

15100134 FE_GDM_RXID2 FE GDM RXID Control 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GDM_STAG7_RXID_SEL		GDM_STAG6_RXID_SEL		GDM_STAG5_RXID_SEL		GDM_STAG4_RXID_SEL		GDM_STAG3_RXID_SEL		GDM_STAG2_RXID_SEL		GDM_STAG1_RXID_SEL		GDM_STAG0_RXID_SEL	
Type	RW		RW		RW		RW		RW		RW		RW		RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													GDM_PID2_RXID_SEL		GDM_PID1_RXID_SEL	
Type													RW		RW	
Reset													0	0	0	0

Bit(s)	Name	Description
31:30	GDM_STAG7_RXID_SEL	GDM RXID Select for STAG = 7
29:28	GDM_STAG6_RXID_SEL	GDM RXID Select for STAG = 6

Bit(s)	Name	Description
27:26	GDM_STAG5_RXID_SEL	GDM RXID Select for STAG = 5
25:24	GDM_STAG4_RXID_SEL	GDM RXID Select for STAG = 4
23:22	GDM_STAG3_RXID_SEL	GDM RXID Select for STAG = 3
21:20	GDM_STAG2_RXID_SEL	GDM RXID Select for STAG = 2
19:18	GDM_STAG1_RXID_SEL	GDM RXID Select for STAG = 1
17:16	GDM_STAG0_RXID_SEL	GDM RXID Select for STAG = 0
3:2	GDM_PID2_RXID_SEL	GDM RXID Select for GDM2 (Port ID = 2)
1:0	GDM_PID1_RXID_SEL	GDM RXID Select for GDM1 (Port ID = 1)

15100138 FE_DBG_CFG FE Debug Configure 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

15100140 PSE_IQ_REV1 PSE Input Queue Reservation part1 000C0008

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								P1_IQ_RES								
Type								RW								
Reset								0	0	0	0	0	1	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								P0_IQ_RES								
Type								RW								
Reset								0	0	0	0	0	1	0	0	0

Bit(s)	Name	Description
24:16	P1_IQ_RES	Virtual input Q reservation [note*] After the flow control of the ingress port is asserted, it can be released when P[n]_IQ_PCNT is lower than (P[n]_IQ_RES/2).
8:0	P0_IQ_RES	Virtual input Q reservation [note*] After the flow control of the ingress port is asserted, it can be released when P[n]_IQ_PCNT is lower than (P[n]_IQ_RES/2).

15100144 PSE_IQ_REV2 PSE Input Queue Reservation part2 01FF000C

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								P3_IQ_RES								
Type								RW								
Reset								1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								P2_IQ_RES								
Type								RW								
Reset								0	0	0	0	0	1	1	0	0

Bit(s)	Name	Description
24:16	P3_IQ_RES	Virtual input Q reservation [note*] After the flow control of the ingress port is asserted, it can be released when P[n]_IQ_PCNT is lower than (P[n]_IQ_RES/2).
8:0	P2_IQ_RES	Virtual input Q reservation [note*] After the flow control of the ingress port is asserted, it can be released when P[n]_IQ_PCNT is lower than (P[n]_IQ_RES/2).

15100148 PSE_IQ_REV3 PSE Input Queue Reservation part3 000801FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								P5_IQ_RES								
Type								RW								
Reset								0	0	0	0	0	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								P4_IQ_RES								
Type								RW								

Reset								1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
24:16	P5_IQ_RES	Virtual input Q reservation [note*] After the flow control of the ingress port is asserted, it can be released when P[n]_IQ_PCNT is lower than (P[n]_IQ_RES/2).
8:0	P4_IQ_RES	Virtual input Q reservation [note*] After the flow control of the ingress port is asserted, it can be released when P[n]_IQ_PCNT is lower than (P[n]_IQ_RES/2).

1510014C PSE_IQ_REV4 PSE Input Queue Reservation part4 00080008

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								P7_IQ_RES								
Type								RW								
Reset								0	0	0	0	0	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								P6_IQ_RES								
Type								RW								
Reset								0	0	0	0	0	1	0	0	0

Bit(s)	Name	Description
24:16	P7_IQ_RES	Virtual input Q reservation [note*] After the flow control of the ingress port is asserted, it can be released when P[n]_IQ_PCNT is lower than (P[n]_IQ_RES/2).
8:0	P6_IQ_RES	Virtual input Q reservation [note*] After the flow control of the ingress port is asserted, it can be released when P[n]_IQ_PCNT is lower than (P[n]_IQ_RES/2).

15100150 PSE_IQ_REV5 PSE Input Queue Reservation part5 00080008

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								P9_IQ_RES								
Type								RW								
Reset								0	0	0	0	0	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name								P8_IQ_RES								
Type								RW								
Reset								0	0	0	0	0	1	0	0	0

Bit(s)	Name	Description
24:16	P9_IQ_RES	Virtual input Q reservation [note*] After the flow control of the ingress port is asserted, it can be released when P[n]_IQ_PCNT is lower than (P[n]_IQ_RES/2).
8:0	P8_IQ_RES	Virtual input Q reservation [note*] After the flow control of the ingress port is asserted, it can be released when P[n]_IQ_PCNT is lower than (P[n]_IQ_RES/2).

15100154 PSE_IQ_REV6 PSE Input Queue Reservation part6 00080008

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								P11_IQ_RES								
Type								RW								
Reset								0	0	0	0	0	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								P10_IQ_RES								
Type								RW								
Reset								0	0	0	0	0	1	0	0	0

Bit(s)	Name	Description
24:16	P11_IQ_RES	Virtual input Q reservation [note*] After the flow control of the ingress port is asserted, it can be released when P[n]_IQ_PCNT is lower than (P[n]_IQ_RES/2).
8:0	P10_IQ_RES	Virtual input Q reservation [note*] After the flow control of the ingress port is asserted, it can be released when P[n]_IQ_PCNT is lower than (P[n]_IQ_RES/2).

15100158 PSE_IQ_REV7 PSE Input Queue Reservation part7 00080008

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								P13_IQ_RES								
Type								RW								

Reset								0	0	0	0	0	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								P12_IQ_RES								
Type								RW								
Reset								0	0	0	0	0	1	0	0	0

Bit(s)	Name	Description
24:16	P13_IQ_RES	Virtual input Q reservation [note*] After the flow control of the ingress port is asserted, it can be released when P[n]_IQ_PCNT is lower than (P[n]_IQ_RES/2).
8:0	P12_IQ_RES	Virtual input Q reservation [note*] After the flow control of the ingress port is asserted, it can be released when P[n]_IQ_PCNT is lower than (P[n]_IQ_RES/2).

1510015C PSE_IQ_REV8 PSE Input Queue Reservation part8 00100008

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								FREE_DROP								
Type								RW								
Reset								0	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								P14_IQ_RES								
Type								RW								
Reset								0	0	0	0	0	1	0	0	0

Bit(s)	Name	Description
24:16	FREE_DROP	Free Buffer Drop Threshold
8:0	P14_IQ_RES	Virtual input Q reservation [note*] After the flow control of the ingress port is asserted, it can be released when P[n]_IQ_PCNT is lower than (P[n]_IQ_RES/2).

15100160 PSE_OQ_TH1 PSE Output Queue Threshold part1 00300020

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								P1_OQ_TH								

Type								RW							
Reset								0	0	0	1	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
Name								P0_OQ_TH							
Type								RW							
Reset								0	0	0	1	0	0	0	0

Bit(s)	Name	Description
24:16	P1_OQ_TH	Output Queue FC Threshold [note*] After the flow control of the egress port is asserted, it can be released when the free buffer count is higher than FQ_HIGH.
8:0	P0_OQ_TH	Output Queue FC Threshold [note*] After the flow control of the egress port is asserted, it can be released when the free buffer count is higher than FQ_HIGH.

15100164 PSE_OQ_TH2 PSE Output Queue Threshold part2 00400030

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								P3_OQ_TH								
Type								RW								
Reset								0	0	1	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								P2_OQ_TH								
Type								RW								
Reset								0	0	0	1	1	0	0	0	0

Bit(s)	Name	Description
24:16	P3_OQ_TH	Output Queue FC Threshold [note*] After the flow control of the egress port is asserted, it can be released when the free buffer count is higher than FQ_HIGH.
8:0	P2_OQ_TH	Output Queue FC Threshold [note*] After the flow control of the egress port is asserted, it can be released when the free buffer count is higher than FQ_HIGH.

15100168 PSE_OQ_TH3 PSE Output Queue Threshold part3 00200040

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								P5_OQ_TH								
Type								RW								
Reset								0	0	0	1	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								P4_OQ_TH								
Type								RW								
Reset								0	0	1	0	0	0	0	0	0

Bit(s)	Name	Description
24:16	P5_OQ_TH	Output Queue FC Threshold [note*] After the flow control of the egress port is asserted, it can be released when the free buffer count is higher than FQ_HIGH.
8:0	P4_OQ_TH	Output Queue FC Threshold [note*] After the flow control of the egress port is asserted, it can be released when the free buffer count is higher than FQ_HIGH.

1510016C PSE_OQ_TH4 PSE Output Queue Threshold part4 00200020

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								P7_OQ_TH								
Type								RW								
Reset								0	0	0	1	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								P6_OQ_TH								
Type								RW								
Reset								0	0	0	1	0	0	0	0	0

Bit(s)	Name	Description
24:16	P7_OQ_TH	Output Queue FC Threshold [note*] After the flow control of the egress port is asserted, it can be released when the free buffer count is higher than FQ_HIGH.
8:0	P6_OQ_TH	Output Queue FC Threshold [note*] After the flow control of the egress port is asserted, it can be released when the free buffer count is higher than FQ_HIGH.

15100170 PSE_OQ_TH5 PSE Output Queue Threshold part5 00200020

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								P9_OQ_TH								
Type								RW								
Reset								0	0	0	1	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								P8_OQ_TH								
Type								RW								
Reset								0	0	0	1	0	0	0	0	0

Bit(s)	Name	Description
24:16	P9_OQ_TH	Output Queue FC Threshold [note*] After the flow control of the egress port is asserted, it can be released when the free buffer count is higher than FQ_HIGH.
8:0	P8_OQ_TH	Output Queue FC Threshold [note*] After the flow control of the egress port is asserted, it can be released when the free buffer count is higher than FQ_HIGH.

15100174 PSE_OQ_TH6 PSE Output Queue Threshold part6 00200020

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								P11_OQ_TH								
Type								RW								
Reset								0	0	0	1	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								P10_OQ_TH								
Type								RW								
Reset								0	0	0	1	0	0	0	0	0

Bit(s)	Name	Description
24:16	P11_OQ_TH	Output Queue FC Threshold [note*] After the flow control of the egress port is asserted, it can be released when the free buffer count is higher than FQ_HIGH.
8:0	P10_OQ_TH	Output Queue FC Threshold

Bit(s)	Name	Description
		[note*] After the flow control of the egress port is asserted, it can be released when the free buffer count is higher than FQ_HIGH.

15100178 PSE_OQ_TH7 PSE Output Queue Threshold part7 00200020

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								P13_OQ_TH								
Type								RW								
Reset								0	0	0	1	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								P12_OQ_TH								
Type								RW								
Reset								0	0	0	1	0	0	0	0	0

Bit(s)	Name	Description
24:16	P13_OQ_TH	Output Queue FC Threshold [note*] After the flow control of the egress port is asserted, it can be released when the free buffer count is higher than FQ_HIGH.
8:0	P12_OQ_TH	Output Queue FC Threshold [note*] After the flow control of the egress port is asserted, it can be released when the free buffer count is higher than FQ_HIGH.

1510017C PSE_OQ_TH8 PSE Output Queue Threshold part8 00200020

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								REV								
Type								RW								
Reset								0	0	0	1	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								P14_OQ_TH								
Type								RW								
Reset								0	0	0	1	0	0	0	0	0

Bit(s)	Name	Description
24:16	REV	Reserved
8:0	P14_OQ_TH	Output Queue FC Threshold [note*] After the flow control of the egress port is asserted, it can be released when the free buffer count is higher than FQ_HIGH.

15100180 PSE_IQ_STA1 PSE Input Queue Status part1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								P1_IQ_PCNT								
Type								RO								
Reset								0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								P0_IQ_PCNT								
Type								RO								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
24:16	P1_IQ_PCNT	Virtual input Q page count
8:0	P0_IQ_PCNT	Virtual input Q page count

15100184 PSE_IQ_STA2 PSE Input Queue Status part2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								P3_IQ_PCNT								
Type								RO								
Reset								0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								P2_IQ_PCNT								
Type								RO								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
24:16	P3_IQ_PCNT	Virtual input Q page count
8:0	P2_IQ_PCNT	Virtual input Q page count

Bit(s)	Name	Description

15100188 PSE_IQ_STA3 PSE Input Queue Status part3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								P5_IQ_PCNT								
Type								RO								
Reset								0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								P4_IQ_PCNT								
Type								RO								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
24:16	P5_IQ_PCNT	Virtual input Q page count
8:0	P4_IQ_PCNT	Virtual input Q page count

1510018C PSE_IQ_STA4 PSE Input Queue Status part4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								P7_IQ_PCNT								
Type								RO								
Reset								0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								P6_IQ_PCNT								
Type								RO								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
24:16	P7_IQ_PCNT	Virtual input Q page count
8:0	P6_IQ_PCNT	Virtual input Q page count

15100190 PSE_IQ_STA5 PSE Input Queue Status part5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								P9_IQ_PCNT								
Type								RO								
Reset								0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								P8_IQ_PCNT								
Type								RO								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
24:16	P9_IQ_PCNT	Virtual input Q page count
8:0	P8_IQ_PCNT	Virtual input Q page count

15100194 PSE_IQ_STA6 PSE Input Queue Status part6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								P11_IQ_PCNT								
Type								RO								
Reset								0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								P10_IQ_PCNT								
Type								RO								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
24:16	P11_IQ_PCNT	Virtual input Q page count
8:0	P10_IQ_PCNT	Virtual input Q page count

15100198 PSE_IQ_STA7 PSE Input Queue Status part7 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								P13_IQ_PCNT								

Type								RO								
Reset								0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								P12_IQ_PCNT								
Type								RO								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
24:16	P13_IQ_PCNT	Virtual input Q page count
8:0	P12_IQ_PCNT	Virtual input Q page count

1510019C PSE_IQ_STA8 PSE Input Queue Status part8 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								P14_IQ_PCNT								
Type								RO								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
8:0	P14_IQ_PCNT	Virtual input Q page count

151001A0 PSE_OQ_STA1 PSE Output Queue Status part1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								P1_OQ_PCNT								
Type								RO								
Reset								0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name								P0_OQ_PCNT							
Type								RO							
Reset								0	0	0	0	0	0	0	0

Bit(s)	Name	Description
24:16	P1_OQ_PCNT	Output Q page count
8:0	P0_OQ_PCNT	Output Q page count

151001A4 PSE_OQ_STA2 PSE Output Queue Status part2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								P3_OQ_PCNT								
Type								RO								
Reset								0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								P2_OQ_PCNT								
Type								RO								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
24:16	P3_OQ_PCNT	Output Q page count
8:0	P2_OQ_PCNT	Output Q page count

151001A8 PSE_OQ_STA3 PSE Output Queue Status part3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								P5_OQ_PCNT								
Type								RO								
Reset								0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								P4_OQ_PCNT								
Type								RO								

Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
24:16	P5_OQ_PCNT	Output Q page count
8:0	P4_OQ_PCNT	Output Q page count

151001AC PSE_OQ_STA4 PSE Output Queue Status part4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								P7_OQ_PCNT								
Type								RO								
Reset								0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								P6_OQ_PCNT								
Type								RO								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
24:16	P7_OQ_PCNT	Output Q page count
8:0	P6_OQ_PCNT	Output Q page count

151001B0 PSE_OQ_STA5 PSE Output Queue Status part5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								P9_OQ_PCNT								
Type								RO								
Reset								0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								P8_OQ_PCNT								
Type								RO								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
24:16	P9_OQ_PCNT	Output Q page count
8:0	P8_OQ_PCNT	Output Q page count

151001B4 PSE_OQ_STA6 PSE Output Queue Status part6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								P11_OQ_PCNT								
Type								RO								
Reset								0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								P10_OQ_PCNT								
Type								RO								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
24:16	P11_OQ_PCNT	Output Q page count
8:0	P10_OQ_PCNT	Output Q page count

151001B8 PSE_OQ_STA7 PSE Output Queue Status part7 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								P13_OQ_PCNT								
Type								RO								
Reset								0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								P12_OQ_PCNT								
Type								RO								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
24:16	P13_OQ_PCNT	Output Q page count
8:0	P12_OQ_PCNT	Output Q page count

151001BC PSE_OQ_STA8 PSE Output Queue Status part8 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								P14_OQ_PCNT								
Type								RO								
Reset								0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description
24:16	P14_OQ_PCNT	Output Q page count

151001C0 PSE_TDM_TBL0 PSE TDM arbiter table0 84321A43

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TDM_TBL_7				TDM_TBL_6				TDM_TBL_5				TDM_TBL_4			
Type	RW				RW				RW				RW			
Reset	1	0	0	0	0	1	0	0	0	0	1	1	0	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TDM_TBL_3				TDM_TBL_2				TDM_TBL_1				TDM_TBL_0			
Type	RW				RW				RW				RW			
Reset	0	0	0	1	1	0	1	0	0	1	0	0	0	0	1	1

Bit(s)	Name	Description
31:28	TDM_TBL_7	PSE TDM arbiter table entry 7
27:24	TDM_TBL_6	PSE TDM arbiter table entry 6
23:20	TDM_TBL_5	PSE TDM arbiter table entry 5
19:16	TDM_TBL_4	PSE TDM arbiter table entry 4
15:12	TDM_TBL_3	PSE TDM arbiter table entry 3
11:8	TDM_TBL_2	PSE TDM arbiter table entry 2
7:4	TDM_TBL_1	PSE TDM arbiter table entry 1
3:0	TDM_TBL_0	PSE TDM arbiter table entry 0

151001C4 PSE TDM_TBL1 PSE TDM arbiter table1 321A4359

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TDM_TBL_15				TDM_TBL_14				TDM_TBL_13				TDM_TBL_12			
Type	RW				RW				RW				RW			
Reset	0	0	1	1	0	0	1	0	0	0	0	1	1	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TDM_TBL_11				TDM_TBL_10				TDM_TBL_9				TDM_TBL_8			
Type	RW				RW				RW				RW			
Reset	0	1	0	0	0	0	1	1	0	1	0	1	1	0	0	1

Bit(s)	Name	Description
31:28	TDM_TBL_15	PSE TDM arbiter table entry 15
27:24	TDM_TBL_14	PSE TDM arbiter table entry 14
23:20	TDM_TBL_13	PSE TDM arbiter table entry 13
19:16	TDM_TBL_12	PSE TDM arbiter table entry 12
15:12	TDM_TBL_11	PSE TDM arbiter table entry 11
11:8	TDM_TBL_10	PSE TDM arbiter table entry 10
7:4	TDM_TBL_9	PSE TDM arbiter table entry 9
3:0	TDM_TBL_8	PSE TDM arbiter table entry 8

151001C8 PSE TDM_TBL2 PSE TDM arbiter table2 1A436984

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TDM_TBL_23				TDM_TBL_22				TDM_TBL_21				TDM_TBL_20			
Type	RW				RW				RW				RW			
Reset	0	0	0	1	1	0	1	0	0	1	0	0	0	0	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TDM_TBL_19				TDM_TBL_18				TDM_TBL_17				TDM_TBL_16			
Type	RW				RW				RW				RW			
Reset	0	1	1	0	1	0	0	1	1	0	0	0	0	1	0	0

Bit(s)	Name	Description
31:28	TDM_TBL_23	PSE TDM arbiter table entry 23
27:24	TDM_TBL_22	PSE TDM arbiter table entry 22
23:20	TDM_TBL_21	PSE TDM arbiter table entry 21
19:16	TDM_TBL_20	PSE TDM arbiter table entry 20
15:12	TDM_TBL_19	PSE TDM arbiter table entry 19

Bit(s)	Name	Description
11:8	TDM_TBL_18	PSE TDM arbiter table entry 18
7:4	TDM_TBL_17	PSE TDM arbiter table entry 17
3:0	TDM_TBL_16	PSE TDM arbiter table entry 16

151001CC PSE TDM TBL3 PSE TDM arbiter table3 30A98432

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TDM_TBL_31				TDM_TBL_30				TDM_TBL_29				TDM_TBL_28			
Type	RW				RW				RW				RW			
Reset	0	0	1	1	0	0	0	0	1	0	1	0	1	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TDM_TBL_27				TDM_TBL_26				TDM_TBL_25				TDM_TBL_24			
Type	RW				RW				RW				RW			
Reset	1	0	0	0	0	1	0	0	0	0	1	1	0	0	1	0

Bit(s)	Name	Description
31:28	TDM_TBL_31	PSE TDM arbiter table entry 31
27:24	TDM_TBL_30	PSE TDM arbiter table entry 30
23:20	TDM_TBL_29	PSE TDM arbiter table entry 29
19:16	TDM_TBL_28	PSE TDM arbiter table entry 28
15:12	TDM_TBL_27	PSE TDM arbiter table entry 27
11:8	TDM_TBL_26	PSE TDM arbiter table entry 26
7:4	TDM_TBL_25	PSE TDM arbiter table entry 25
3:0	TDM_TBL_24	PSE TDM arbiter table entry 24

151001D0 PSE TDM TBL4 PSE TDM arbiter table4 8A432154

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TDM_TBL_39				TDM_TBL_38				TDM_TBL_37				TDM_TBL_36			
Type	RW				RW				RW				RW			
Reset	1	0	0	0	1	0	1	0	0	1	0	0	0	0	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TDM_TBL_35				TDM_TBL_34				TDM_TBL_33				TDM_TBL_32			
Type	RW				RW				RW				RW			
Reset	0	0	1	0	0	0	0	1	0	1	0	1	0	1	0	0

Bit(s)	Name	Description
31:28	TDM_TBL_39	PSE TDM arbiter table entry 39
27:24	TDM_TBL_38	PSE TDM arbiter table entry 38
23:20	TDM_TBL_37	PSE TDM arbiter table entry 37
19:16	TDM_TBL_36	PSE TDM arbiter table entry 36
15:12	TDM_TBL_35	PSE TDM arbiter table entry 35
11:8	TDM_TBL_34	PSE TDM arbiter table entry 34
7:4	TDM_TBL_33	PSE TDM arbiter table entry 33
3:0	TDM_TBL_32	PSE TDM arbiter table entry 32

151001D4 PSE TDM TBL5 PSE TDM arbiter table5 321A6439

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TDM_TBL_47				TDM_TBL_46				TDM_TBL_45				TDM_TBL_44			
Type	RW				RW				RW				RW			
Reset	0	0	1	1	0	0	1	0	0	0	0	1	1	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TDM_TBL_43				TDM_TBL_42				TDM_TBL_41				TDM_TBL_40			
Type	RW				RW				RW				RW			
Reset	0	1	1	0	0	1	0	0	0	0	1	1	1	0	0	1

Bit(s)	Name	Description
31:28	TDM_TBL_47	PSE TDM arbiter table entry 47
27:24	TDM_TBL_46	PSE TDM arbiter table entry 46
23:20	TDM_TBL_45	PSE TDM arbiter table entry 45
19:16	TDM_TBL_44	PSE TDM arbiter table entry 44
15:12	TDM_TBL_43	PSE TDM arbiter table entry 43
11:8	TDM_TBL_42	PSE TDM arbiter table entry 42
7:4	TDM_TBL_41	PSE TDM arbiter table entry 41
3:0	TDM_TBL_40	PSE TDM arbiter table entry 40

151001D8 PSE TDM TBL6 PSE TDM arbiter table6 8435A984

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TDM_TBL_55				TDM_TBL_54				TDM_TBL_53				TDM_TBL_52			
Type	RW				RW				RW				RW			
Reset	1	0	0	0	0	1	0	0	0	0	1	1	0	1	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TDM_TBL_51				TDM_TBL_50				TDM_TBL_49				TDM_TBL_48			

Type	RW				RW				RW				RW			
Reset	1	0	1	0	1	0	0	1	1	0	0	0	0	1	0	0

Bit(s)	Name	Description
31:28	TDM_TBL_55	PSE TDM arbiter table entry 55
27:24	TDM_TBL_54	PSE TDM arbiter table entry 54
23:20	TDM_TBL_53	PSE TDM arbiter table entry 53
19:16	TDM_TBL_52	PSE TDM arbiter table entry 52
15:12	TDM_TBL_51	PSE TDM arbiter table entry 51
11:8	TDM_TBL_50	PSE TDM arbiter table entry 50
7:4	TDM_TBL_49	PSE TDM arbiter table entry 49
3:0	TDM_TBL_48	PSE TDM arbiter table entry 48

151001DC PSE TDM TBL7 PSE TDM arbiter table7 602143A9

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TDM_TBL_63				TDM_TBL_62				TDM_TBL_61				TDM_TBL_60			
Type	RW				RW				RW				RW			
Reset	0	1	1	0	0	0	0	0	0	0	1	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TDM_TBL_59				TDM_TBL_58				TDM_TBL_57				TDM_TBL_56			
Type	RW				RW				RW				RW			
Reset	0	1	0	0	0	0	1	1	1	0	1	0	1	0	0	1

Bit(s)	Name	Description
31:28	TDM_TBL_63	PSE TDM arbiter table entry 63
27:24	TDM_TBL_62	PSE TDM arbiter table entry 62
23:20	TDM_TBL_61	PSE TDM arbiter table entry 61
19:16	TDM_TBL_60	PSE TDM arbiter table entry 60
15:12	TDM_TBL_59	PSE TDM arbiter table entry 59
11:8	TDM_TBL_58	PSE TDM arbiter table entry 58
7:4	TDM_TBL_57	PSE TDM arbiter table entry 57
3:0	TDM_TBL_56	PSE TDM arbiter table entry 56

151001E0 PSE SP CFG0 PSE Strict Priority Configure0 5CBA4312

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PRIORITY_7				PRIORITY_6				PRIORITY_5				PRIORITY_4			
Type	RW				RW				RW				RW			

Reset	0	1	0	1	1	1	0	0	1	0	1	1	1	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PRIORITY_3				PRIORITY_2				PRIORITY_1				PRIORITY_0			
Type	RW				RW				RW				RW			
Reset	0	1	0	0	0	0	1	1	0	0	0	1	0	0	1	0

Bit(s)	Name	Description
31:28	PRIORITY_7	PSE port num at priority 7
27:24	PRIORITY_6	PSE port num at priority 6
23:20	PRIORITY_5	PSE port num at priority 5
19:16	PRIORITY_4	PSE port num at priority 4
15:12	PRIORITY_3	PSE port num at priority 3
11:8	PRIORITY_2	PSE port num at priority 2
7:4	PRIORITY_1	PSE port num at priority 1
3:0	PRIORITY_0	PSE port num at priority 0

151001E4 PSE_SP_CFG1 PSE Strict Priority Configure1 77770986

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PRIORITY_15				PRIORITY_14				PRIORITY_13				PRIORITY_12			
Type	RW				RW				RW				RW			
Reset	0	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PRIORITY_11				PRIORITY_10				PRIORITY_9				PRIORITY_8			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	1	0	0	1	1	0	0	0	0	1	1	0

Bit(s)	Name	Description
31:28	PRIORITY_15	PSE port num at priority 15
27:24	PRIORITY_14	PSE port num at priority 14
23:20	PRIORITY_13	PSE port num at priority 13
19:16	PRIORITY_12	PSE port num at priority 12
15:12	PRIORITY_11	PSE port num at priority 11
11:8	PRIORITY_10	PSE port num at priority 10
7:4	PRIORITY_9	PSE port num at priority 9
3:0	PRIORITY_8	PSE port num at priority 8

151001E8 PSE_TDM_CFG PSE TDM arbiter configure 003F0003

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											PSE_TDM_ARB_NUM					
Type											RW					
Reset											1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															PSE_SP_ARB_EN	PSE_TDM_ARB_EN
Type															RW	RW
Reset															1	1

Bit(s)	Name	Description
21:16	PSE_TDM_ARB_NUM	TDM table entry number
1	PSE_SP_ARB_EN	Enable PSE Strict priority arbiter, it works if no request match current TDM slot
0	PSE_TDM_ARB_EN	Enable PSE TDM arbiter

15100200 FE_CDM1_DBG1 FE CDM1 Debug part1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CDM1_FS_RINF_LSB															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CDM1_FS_RINF_LSB															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CDM1_FS_RINF_LSB	CDM1 fs packet info [31:0]

15100204 FE_CDM1_DBG2 FE CDM1 Debug part2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	CDM1_FS_RINF_MSB															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CDM1_FS_RINF_MSB															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CDM1_FS_RINF_MSB	CDM1 fs packet info [63:32]

15100208 FE_CDM2_DBG1 FE CDM2 Debug part1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CDM2_FS_RINF_LSB															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CDM2_FS_RINF_LSB															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CDM2_FS_RINF_LSB	CDM2 fs packet info [31:0]

1510020C FE_CDM2_DBG2 FE CDM2 Debug part2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CDM2_FS_RINF_MSB															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	CDM2_FS_RINF_MSB															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CDM2_FS_RINF_MSB	CDM2 fs packet info [63:32]

15100210 FE_GDM1_DBG1 FE GDM1 Debug part1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GDM1_FS_RINF_LSB															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GDM1_FS_RINF_LSB															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	GDM1_FS_RINF_LSB	GDM1 fs packet info [31:0]

15100214 FE_GDM1_DBG2 FE GDM1 Debug part2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GDM1_FS_RINF_MSB															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GDM1_FS_RINF_MSB															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	GDM1_FS_RINF_MSB	GDM1 fs packet info [63:32]

15100218 FE_GDM2_DBG1 FE GDM2 Debug part1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GDM2_FS_RINF_LSB															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GDM2_FS_RINF_LSB															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	GDM2_FS_RINF_LSB	GDM2 fs packet info [31:0]

1510021C FE_GDM2_DBG2 FE GDM2 Debug part2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GDM2_FS_RINF_MSB															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GDM2_FS_RINF_MSB															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	GDM2_FS_RINF_MSB	GDM2 fs packet info [63:32]

15100220 FE_CDM1_FSM FE CDM1 FSM status 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name					FS_PARSER_FSM								FS_FSM			
Type					RO								RO			
Reset					0	0	0	0					0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					TS_PARSER_FSM								TS_FSM			
Type					RO								RO			
Reset					0	0	0	0	0				0	0	0	0

Bit(s)	Name	Description
27:24	FS_PARSER_FSM	FSM status in cdm_fs_parser
19:16	FS_FSM	FSM status in cdm_fs_fsm
12:8	TS_PARSER_FSM	FSM status in cdm_ts_parser
3:0	TS_FSM	FSM status in cdm_ts_fsm

15100224 FE_CDM2_FSM FE CDM2 FSM status 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					FS_PARSER_FSM								FS_FSM			
Type					RO								RO			
Reset					0	0	0	0					0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					TS_PARSER_FSM								TS_FSM			
Type					RO								RO			
Reset					0	0	0	0	0				0	0	0	0

Bit(s)	Name	Description
27:24	FS_PARSER_FSM	FSM status in cdm_fs_parser
19:16	FS_FSM	FSM status in cdm_fs_fsm
12:8	TS_PARSER_FSM	FSM status in cdm_ts_parser
3:0	TS_FSM	FSM status in cdm_ts_fsm

15100228 FE_GDM1_FSM FE GDM1 FSM status 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name				FS_FIFO_FSM					FS_PARSER_FSM				FS_FSM			
Type				RO					RO				RO			
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									TS_PARSER_FSM				TS_FSM			
Type									RO				RO			
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:24	FS_FIFO_FSM	FSM status in gdm_fs_fifo
23:20	FS_PARSER_FSM	FSM status in gdm_fs_parser
19:16	FS_FSM	FSM status in gdm_fs_fsm
7:4	TS_PARSER_FSM	FSM status in gdm_ts_parser
3:0	TS_FSM	FSM status in gdm_ts_fsm

1510022C FE_GDM2_FSM FE GDM2 FSM status 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				FS_FIFO_FSM					FS_PARSER_FSM				FS_FSM			
Type				RO					RO				RO			
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									TS_PARSER_FSM				TS_FSM			
Type									RO				RO			
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:24	FS_FIFO_FSM	FSM status in gdm_fs_fifo
23:20	FS_PARSER_FSM	FSM status in gdm_fs_parser
19:16	FS_FSM	FSM status in gdm_fs_fsm
7:4	TS_PARSER_FSM	FSM status in gdm_ts_parser
3:0	TS_FSM	FSM status in gdm_ts_fsm

15100230 FE_CDM3_DBG1

FE CDM3 Debug part1

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CDM3_FS_RINF_LSB															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CDM3_FS_RINF_LSB															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CDM3_FS_RINF_LSB	CDM3 fs packet info [31:0]

15100234 **FE_CDM3_DBG2** FE CDM3 Debug part2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CDM3_FS_RINF_MSB															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CDM3_FS_RINF_MSB															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CDM3_FS_RINF_MSB	CDM3 fs packet info [63:32]

15100238 **FE_CDM3_FSM** FE CDM3 FSM status 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					FS_PARSER_FSM								FS_FSM			
Type					RO								RO			
Reset					0	0	0	0					0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				TS_PARSER_FSM									TS_FSM			
Type				RO									RO			
Reset				0	0	0	0	0					0	0	0	0

Bit(s)	Name	Description
27:24	FS_PARSER_FSM	FSM status in cdm_fs_parser
19:16	FS_FSM	FSM status in cdm_fs_fsm
12:8	TS_PARSER_FSM	FSM status in cdm_ts_parser
3:0	TS_FSM	FSM status in cdm_ts_fsm

15100240 FE_PSE_FREE PSE Free Page Count 01FF01FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								FQ_PCNT_MIN								
Type								RC								
Reset								1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								FQ_PCNT								
Type								RO								
Reset								1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
24:16	FQ_PCNT_MIN	Free queue minimum page count since the last read The minimum free page count will update the value whenever the free page is lower than the current record. The field will be reset to FF after MCU reads it.
8:0	FQ_PCNT	Free queue page count

15100244 FE_DROP_FQ FE Packet Drop by Free Queue 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PSE_DROP_FQ															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PSE_DROP_FQ															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	PSE_DROP_FQ	Packet dropped by PSE when the free queue is low. When GDM is receiving a packets and the free buffer is almost exhausted, PSE will drop any received packet no matter if FC is on or off. The filed is reset to 0 after MCU reads it.

15100248 FE_DROP_FC FE Packet Drop by Flow Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PSE_DROP_FC															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PSE_DROP_FC															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	PSE_DROP_FC	Packet dropped by PSE when the flow control is off When GDM receive the packets over the FC threshold and the flow control is off, PSE will drop the received packet to prevent the free buffer from being exhausted. The filed is reset to 0 after MCU reads it.

1510024C FE_DROP_PPE1 FE Packet Drop by PPE1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PSE_DROP_PPE1															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	PSE_DROP_PPE1															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	PSE_DROP_PPE1	Packet dropped by PPE1 The PPE1 forwarded packet is dropped due to PDMA RX Ring is almost full when PSE_MIR_PORT.PO_DROP_PPE is enabled. The filed is reset to 0 after MCU reads it.

15100250 FE_DROP_PD_6 FE Packet Drop by Port 6 Disabled 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PSE_DROP_P6															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	PSE_DROP_P6	MIB counter for packet dropped by destination port P6 is disabled Packet dropped by PSE due to FE_GLO_CFG.LINK_DWN[6] = 1 The filed is reset to 0 after MCU reads it.

15100254 FE_DROP_PD_5 FE Packet Drop by Port 5 Disabled 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PSE_DROP_P5															

Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	PSE_DROP_P5	MIB counter for packet dropped by destination port P5 is disabled Packet dropped by PSE due to FE_GLO_CFG.LINK_DWN[5] = 1 The filed is reset to 0 after MCU reads it.

15100258 FE_DROP_PD_4 FE Packet Drop by Port 4 Disabled 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PSE_DROP_P4															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	PSE_DROP_P4	MIB counter for packet dropped by destination port P4 is disabled Packet dropped by PSE due to FE_GLO_CFG.LINK_DWN[4] = 1 or PPE_GLO_CFG.PPE_EN = 0 The filed is reset to 0 after MCU reads it.

1510025C FE_DROP_PD_3 FE Packet Drop by Port 3 Disabled 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PSE_DROP_P3															
Type	RC															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	PSE_DROP_P3	MIB counter for packet dropped by destination port P3 is disabled Packet dropped by PSE due to FE_GLO_CFG.LINK_DWN[3] = 1 The filed is reset to 0 after MCU reads it.

15100260 FE_DROP_PD_2 FE Packet Drop by Port 2 Disabled 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PSE_DROP_P2															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	PSE_DROP_P2	MIB counter for packet dropped by destination port P2 is disabled Packet dropped by PSE due to FE_GLO_CFG.LINK_DWN[2] = 1 or MAC_P2_SR.LINK_STATUS = 0 The filed is reset to 0 after MCU reads it.

15100264 FE_DROP_PD_1 FE Packet Drop by Port 1 Disabled 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PSE_DROP_P1															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	PSE_DROP_P1	MIB counter for packet dropped by destination port P1 is disabled Packet dropped by PSE due to FE_GLO_CFG.LINK_DWN[1] = 1 or MAC_P1_SR.LINK_STATUS = 0 The filed is reset to 0 after MCU reads it.

15100268 FE_DROP_PD_0 FE Packet Drop by Port 0 Disabled 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PSE_DROP_P0															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	PSE_DROP_P0	MIB counter for packet dropped by destination port P0 is disabled Packet dropped by PSE due to FE_GLO_CFG.LINK_DWN[0] = 1 The filed is reset to 0 after MCU reads it.

15100270 FE_DROP_PD_14 FE Packet Drop by Port 14 Disabled 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PSE_DROP_P14															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	PSE_DROP_P14	MIB counter for packet dropped by destination port P14 is disabled Packet dropped by PSE due to FE_GLO_CFG2.LINK_DWN[6] = 1

Bit(s)	Name	Description
		The filed is reset to 0 after MCU reads it.

15100274 FE_DROP_PD_13 FE Packet Drop by Port 13 Disabled 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PSE_DROP_P13															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	PSE_DROP_P13	MIB counter for packet dropped by destination port P13 is disabled Packet dropped by PSE due to FE_GLO_CFG2.LINK_DWN[5] = 1 The filed is reset to 0 after MCU reads it.

15100278 FE_DROP_PD_12 FE Packet Drop by Port 12 Disabled 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PSE_DROP_P12															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	PSE_DROP_P12	MIB counter for packet dropped by destination port P12 is disabled Packet dropped by PSE due to FE_GLO_CFG2.LINK_DWN[4] = 1 The filed is reset to 0 after MCU reads it.

1510027C FE_DROP_PD_11 FE Packet Drop by Port 11 Disabled 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PSE_DROP_P11															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	PSE_DROP_P11	MIB counter for packet dropped by destination port P11 is disabled Packet dropped by PSE due to FE_GLO_CFG2.LINK_DWN[3] = 1 The filed is reset to 0 after MCU reads it.

15100280 FE_DROP_PD_10 FE Packet Drop by Port 10 Disabled 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PSE_DROP_P10															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	PSE_DROP_P10	MIB counter for packet dropped by destination port P10 is disabled Packet dropped by PSE due to FE_GLO_CFG2.LINK_DWN[2] = 1 The filed is reset to 0 after MCU reads it.

15100284 FE_DROP_PD_9 FE Packet Drop by Port 9 Disabled 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PSE_DROP_P9															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	PSE_DROP_P9	MIB counter for packet dropped by destination port P9 is disabled Packet dropped by PSE due to FE_GLO_CFG2.LINK_DWN[1] = 1 The filed is reset to 0 after MCU reads it.

15100288 FE_DROP_PD_8 FE Packet Drop by Port 8 Disabled 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PSE_DROP_P8															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	PSE_DROP_P8	MIB counter for packet dropped by destination port P8 is disabled Packet dropped by PSE due to FE_GLO_CFG2.LINK_DWN[0] = 1 The filed is reset to 0 after MCU reads it.

1510028C FE_DROP_PD_7 FE Packet Drop by Port 7 Disabled 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																

Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PSE_DROP_P7															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	PSE_DROP_P7	MIB counter for packet dropped by destination port P7 is disabled Packet dropped by PSE due to FE_GLO_CFG.LINK_DWN[7] = 1 The filed is reset to 0 after MCU reads it.

15100290 FE_CDM4_DBG1 FE CDM4 Debug part1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CDM4_FS_RINF_LSB															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CDM4_FS_RINF_LSB															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CDM4_FS_RINF_LSB	CDM4 fs packet info [31:0]

15100294 FE_CDM4_DBG2 FE CDM4 Debug part2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CDM4_FS_RINF_MSB															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	CDM4_FS_RINF_MSB															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CDM4_FS_RINF_MSB	CDM4 fs packet info [63:32]

15100298 FE_CDM4_FSM FE CDM4 FSM status 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					FS_PARSER_FSM								FS_FSM			
Type					RO								RO			
Reset					0	0	0	0					0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					TS_PARSER_FSM								TS_FSM			
Type					RO								RO			
Reset				0	0	0	0	0					0	0	0	0

Bit(s)	Name	Description
27:24	FS_PARSER_FSM	FSM status in cdm_fs_parser
19:16	FS_FSM	FSM status in cdm_fs_fsm
12:8	TS_PARSER_FSM	FSM status in cdm_ts_parser
3:0	TS_FSM	FSM status in cdm_ts_fsm

151002A0 FE_DROP_PPE0 FE Packet Drop by PPE0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PSE_DROP_PPE0															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PSE_DROP_PPE0															
Type	RC															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	PSE_DROP_PPE0	Packet dropped by PPE0 The PPE0 forwarded packet is dropped due to PDMA RX Ring is almost full when PSE_MIR_PORT.P0_DROP_PPE is enabled. The filed is reset to 0 after MCU reads it.

151002A4 FE_DROP_PPE0_P0_R01 FE Packet To Port0 Ring 0&1 Drop by PPE0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PSE_DROP_PPE0_P0_R1															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PSE_DROP_PPE0_P0_R0															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	PSE_DROP_PPE0_P0_R1	Packet to ADMA Ring 1 dropped by PPE0 The PPE0 forwarded packet is dropped due to ADMA RX Ring 1 is almost full when FE_DROP_PPE0.P0_DROP_PPE is enabled. The filed is reset to 0 after MCU reads it.
15:0	PSE_DROP_PPE0_P0_R0	Packet to ADMA Ring 0 dropped by PPE0 The PPE0 forwarded packet is dropped due to ADMA RX Ring 0 is almost full when FE_DROP_PPE0.P0_DROP_PPE is enabled. The filed is reset to 0 after MCU reads it.

151002A8 FE_DROP_PPE0_P0_R23 FE Packet To Port0 Ring 2&3 Drop by PPE0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PSE_DROP_PPE0_P0_R3															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PSE_DROP_PPE0_P0_R2															

Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	PSE_DROP_PPE0_P0_R3	Packet to ADMA Ring 3 dropped by PPE0 The PPE0 forwarded packet is dropped due to ADMA RX Ring 3 is almost full when FE_DROP_PPE0.P0_DROP_PPE is enabled. The filed is reset to 0 after MCU reads it.
15:0	PSE_DROP_PPE0_P0_R2	Packet to ADMA Ring 2 dropped by PPE0 The PPE0 forwarded packet is dropped due to ADMA RX Ring 2 is almost full when FE_DROP_PPE0.P0_DROP_PPE is enabled. The filed is reset to 0 after MCU reads it.

151002AC		FE_DROP_PPE0_P5				FE Packet To Port5 Drop by PPE0											00000000	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16		
Name	PSE_DROP_PPE0_P5_R1																	
Type	RC																	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
Name	PSE_DROP_PPE0_P5_R0																	
Type	RC																	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

Bit(s)	Name	Description
31:16	PSE_DROP_PPE0_P5_R1	Packet to QDMA Ring 1 dropped by PPE0 The PPE0 forwarded packet is dropped due to QDMA RX Ring 1 is almost full when FE_DROP_PPE0.P5_DROP_PPE is enabled. The filed is reset to 0 after MCU reads it.
15:0	PSE_DROP_PPE0_P5_R0	Packet to QDMA Ring 0 dropped by PPE0 The PPE0 forwarded packet is dropped due to QDMA RX Ring 0 is almost full when FE_DROP_PPE0.P5_DROP_PPE is enabled. The filed is reset to 0 after MCU reads it.

151002B0		FE_DROP_PPE0_P8				FE Packet To Port8 Drop by PPE0											00000000	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16		
Name	PSE_DROP_PPE0_P8_R1																	
Type	RC																	

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PSE_DROP_PPE0_P8_R0															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	PSE_DROP_PPE0_P8_R1	Packet to WDMA0 Ring 1 dropped by PPE0 The PPE0 forwarded packet is dropped due to WDMA0 RX Ring 1 is almost full when FE_DROP_PPE0.P8_DROP_PPE is enabled. The filed is reset to 0 after MCU reads it.
15:0	PSE_DROP_PPE0_P8_R0	Packet to WDMA0 Ring 0 dropped by PPE0 The PPE0 forwarded packet is dropped due to WDMA0 RX Ring 0 is almost full when FE_DROP_PPE0.P8_DROP_PPE is enabled. The filed is reset to 0 after MCU reads it.

151002B4 FE_DROP_PPE0_P9 FE Packet To Port9 Drop by PPE0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PSE_DROP_PPE0_P9_R1															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PSE_DROP_PPE0_P9_R0															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	PSE_DROP_PPE0_P9_R1	Packet to WDMA1 Ring 1 dropped by PPE0 The PPE0 forwarded packet is dropped due to WDMA1 RX Ring 1 is almost full when FE_DROP_PPE0.P9_DROP_PPE is enabled. The filed is reset to 0 after MCU reads it.
15:0	PSE_DROP_PPE0_P9_R0	Packet to WDMA1 Ring 0 dropped by PPE0 The PPE0 forwarded packet is dropped due to WDMA1 RX Ring 0 is almost full when FE_DROP_PPE0.P9_DROP_PPE is enabled. The filed is reset to 0 after MCU reads it.

151002B8 FE_DROP_PPE0_P10 FE Packet To Port10 Drop by PPE0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PSE_DROP_PPE0_P10_R1															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PSE_DROP_PPE0_P10_R0															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	PSE_DROP_PPE0_P10_R1	Packet to MDMA Ring 1 dropped by PPE0 The PPE0 forwarded packet is dropped due to MDMA RX Ring 1 is almost full when FE_DROP_PPE0.P10_DROP_PPE is enabled. The filed is reset to 0 after MCU reads it.
15:0	PSE_DROP_PPE0_P10_R0	Packet to MDMA Ring 0 dropped by PPE0 The PPE0 forwarded packet is dropped due to MDMA RX Ring 0 is almost full when FE_DROP_PPE0.P10_DROP_PPE is enabled. The filed is reset to 0 after MCU reads it.

151002BC FE_DROP_PPE0_P11 FE Packet To Port11 Drop by PPE0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PSE_DROP_PPE0_P11_R1															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PSE_DROP_PPE0_P11_R0															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	PSE_DROP_PPE0_P11_R1	Packet to EDMA0 Ring 1 dropped by PPE0 The PPE0 forwarded packet is dropped due to GMAC0 RX Ring 1 is almost full when FE_DROP_PPE0.P11_DROP_PPE is enabled. The filed is reset to 0 after MCU reads it.
15:0	PSE_DROP_PPE0_P11_R0	Packet to EDMA0 Ring 0 dropped by PPE0

Bit(s)	Name	Description
		The PPE0 forwarded packet is dropped due to GMAC0 RX Ring 0 is almost full when FE_DROP_PPE0.P11_DROP_PPE is enabled. The filed is reset to 0 after MCU reads it.

151002C0 FE_DROP_PPE0_P12 FE Packet To Port12 Drop by PPE0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PSE_DROP_PPE0_P12_R1															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PSE_DROP_PPE0_P12_R0															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	PSE_DROP_PPE0_P12_R1	Packet to EDMA1 Ring 1 dropped by PPE0 The PPE0 forwarded packet is dropped due to GMAC1 RX Ring 1 is almost full when FE_DROP_PPE0.P12_DROP_PPE is enabled. The filed is reset to 0 after MCU reads it.
15:0	PSE_DROP_PPE0_P12_R0	Packet to EDMA1 Ring 0 dropped by PPE0 The PPE0 forwarded packet is dropped due to GMAC1 RX Ring 0 is almost full when FE_DROP_PPE0.P12_DROP_PPE is enabled. The filed is reset to 0 after MCU reads it.

151002C4 FE_DROP_PPE1_P0_R01 FE Packet To Port0 Ring 0&1 Drop by PPE1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PSE_DROP_PPE1_P0_R1															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PSE_DROP_PPE1_P0_R0															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	PSE_DROP_PPE1_PO_R1	Packet to ADMA Ring 1 dropped by PPE1 The PPE1 forwarded packet is dropped due to ADMA RX Ring 1 is almost full when FE_DROP_PPE1.PO_DROP_PPE is enabled. The filed is reset to 0 after MCU reads it.
15:0	PSE_DROP_PPE1_PO_R0	Packet to ADMA Ring 0 dropped by PPE1 The PPE1 forwarded packet is dropped due to ADMA RX Ring 0 is almost full when FE_DROP_PPE1.PO_DROP_PPE is enabled. The filed is reset to 0 after MCU reads it.

151002C8 FE_DROP_PPE1_PO_R23 FE Packet To Port0 Ring 2&3 Drop by PPE1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PSE_DROP_PPE1_PO_R3															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PSE_DROP_PPE1_PO_R2															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	PSE_DROP_PPE1_PO_R3	Packet to ADMA Ring 3 dropped by PPE1 The PPE1 forwarded packet is dropped due to ADMA RX Ring 3 is almost full when FE_DROP_PPE1.PO_DROP_PPE is enabled. The filed is reset to 0 after MCU reads it.
15:0	PSE_DROP_PPE1_PO_R2	Packet to ADMA Ring 2 dropped by PPE1 The PPE1 forwarded packet is dropped due to ADMA RX Ring 2 is almost full when FE_DROP_PPE1.PO_DROP_PPE is enabled. The filed is reset to 0 after MCU reads it.

151002CC FE_DROP_PPE1_P5 FE Packet To Port5 Drop by PPE1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PSE_DROP_PPE1_P5_R1															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PSE_DROP_PPE1_P5_R0															

Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	PSE_DROP_PPE1_P5_R1	Packet to QDMA Ring 1 dropped by PPE1 The PPE1 forwarded packet is dropped due to QDMA RX Ring 1 is almost full when FE_DROP_PPE1.P5_DROP_PPE is enabled. The filed is reset to 0 after MCU reads it.
15:0	PSE_DROP_PPE1_P5_R0	Packet to QDMA Ring 0 dropped by PPE1 The PPE1 forwarded packet is dropped due to QDMA RX Ring 0 is almost full when FE_DROP_PPE1.P5_DROP_PPE is enabled. The filed is reset to 0 after MCU reads it.

151002D0 FE_DROP_PPE1_P8 FE Packet To Port8 Drop by PPE1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PSE_DROP_PPE1_P8_R1															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PSE_DROP_PPE1_P8_R0															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	PSE_DROP_PPE1_P8_R1	Packet to WDMA0 Ring 1 dropped by PPE1 The PPE1 forwarded packet is dropped due to WDMA0 RX Ring 1 is almost full when FE_DROP_PPE1.P8_DROP_PPE is enabled. The filed is reset to 0 after MCU reads it.
15:0	PSE_DROP_PPE1_P8_R0	Packet to WDMA0 Ring 0 dropped by PPE1 The PPE1 forwarded packet is dropped due to WDMA0 RX Ring 0 is almost full when FE_DROP_PPE1.P8_DROP_PPE is enabled. The filed is reset to 0 after MCU reads it.

151002D4 FE_DROP_PPE1_P9 FE Packet To Port9 Drop by PPE1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PSE_DROP_PPE1_P9_R1															
Type	RC															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PSE_DROP_PPE1_P9_R0															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	PSE_DROP_PPE1_P9_R1	Packet to WDMA1 Ring 1 dropped by PPE1 The PPE1 forwarded packet is dropped due to WDMA1 RX Ring 1 is almost full when FE_DROP_PPE1.P9_DROP_PPE is enabled. The filed is reset to 0 after MCU reads it.
15:0	PSE_DROP_PPE1_P9_R0	Packet to WDMA1 Ring 0 dropped by PPE1 The PPE1 forwarded packet is dropped due to WDMA1 RX Ring 0 is almost full when FE_DROP_PPE1.P9_DROP_PPE is enabled. The filed is reset to 0 after MCU reads it.

151002D8 FE_DROP_PPE1_P10 FE Packet To Port10 Drop by PPE1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PSE_DROP_PPE1_P10_R1															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PSE_DROP_PPE1_P10_R0															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	PSE_DROP_PPE1_P10_R1	Packet to MDMA Ring 1 dropped by PPE1 The PPE1 forwarded packet is dropped due to MDMA RX Ring 1 is almost full when FE_DROP_PPE1.P10_DROP_PPE is enabled. The filed is reset to 0 after MCU reads it.
15:0	PSE_DROP_PPE1_P10_R0	Packet to MDMA Ring 0 dropped by PPE1 The PPE1 forwarded packet is dropped due to MDMA RX Ring 0 is almost full when FE_DROP_PPE1.P10_DROP_PPE is enabled. The filed is reset to 0 after MCU reads it.

151002DC FE_DROP_PPE1_P11 FE Packet To Port11 Drop by PPE1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PSE_DROP_PPE1_P11_R1															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PSE_DROP_PPE1_P11_R0															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	PSE_DROP_PPE1_P11_R1	Packet to EDMA0 Ring 1 dropped by PPE1 The PPE1 forwarded packet is dropped due to GMAC0 RX Ring 1 is almost full when FE_DROP_PPE1.P11_DROP_PPE is enabled. The filed is reset to 0 after MCU reads it.
15:0	PSE_DROP_PPE1_P11_R0	Packet to EDMA0 Ring 0 dropped by PPE1 The PPE1 forwarded packet is dropped due to GMAC0 RX Ring 0 is almost full when FE_DROP_PPE1.P11_DROP_PPE is enabled. The filed is reset to 0 after MCU reads it.

151002E0 FE_DROP_PPE1_P12 FE Packet To Port12 Drop by PPE1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PSE_DROP_PPE1_P12_R1															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PSE_DROP_PPE1_P12_R0															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	PSE_DROP_PPE1_P12_R1	Packet to EDMA1 Ring 1 dropped by PPE1 The PPE1 forwarded packet is dropped due to GMAC1 RX Ring 1 is almost full when FE_DROP_PPE1.P12_DROP_PPE is enabled. The filed is reset to 0 after MCU reads it.
15:0	PSE_DROP_PPE1_P12_R0	Packet to EDMA1 Ring 0 dropped by PPE1

Bit(s)	Name	Description
		The PPE1 forwarded packet is dropped due to GMAC1 RX Ring 0 is almost full when FE_DROP_PPE1.P12_DROP_PPE is enabled. The field is reset to 0 after MCU reads it.

15100300 FE_ALT_CF8 ALT Entry Base Address 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

15100304 FE_ALT_SGL_CFC ALT Single DW read 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

15100308 FE_ALT_SEQ_CFC ALT Sequential DW read 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

1510030C FE_ALT_SEQ_CFC_OFS ALT Sequential DW read 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

15100310 FE_CDM5_DBG1 FE CDM5 Debug part1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CDM5_FS_RINF_LSB															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	CDM5_FS_RINF_LSB															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CDM5_FS_RINF_LSB	CDM5 fs packet info [31:0]

15100314 FE_CDM5_DBG2 FE CDM5 Debug part2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CDM5_FS_RINF_MSB															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CDM5_FS_RINF_MSB															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CDM5_FS_RINF_MSB	CDM5 fs packet info [63:32]

15100318 FE_CDM5_FSM FE CDM5 FSM status 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					FS_PARSER_FSM								FS_FSM			
Type					RO								RO			
Reset					0	0	0	0					0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					TS_PARSER_FSM								TS_FSM			
Type					RO								RO			
Reset					0	0	0	0	0					0	0	0

Bit(s)	Name	Description
27:24	FS_PARSER_FSM	FSM status in cdm_fs_parser
19:16	FS_FSM	FSM status in cdm_fs_fsm
12:8	TS_PARSER_FSM	FSM status in cdm_ts_parser
3:0	TS_FSM	FSM status in cdm_ts_fsm

15100320 FE_CDM6_DBG1 FE CDM6 Debug part1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CDM6_FS_RINF_LSB															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CDM6_FS_RINF_LSB															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CDM6_FS_RINF_LSB	CDM6 fs packet info [31:0]

15100324 FE_CDM6_DBG2 FE CDM6 Debug part2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CDM6_FS_RINF_MSB															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CDM6_FS_RINF_MSB															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CDM6_FS_RINF_MSB	CDM6 fs packet info [63:32]

15100328 FE_CDM6_FSM FE CDM6 FSM status 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					FS_PARSER_FSM								FS_FSM			
Type					RO								RO			
Reset					0	0	0	0					0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					TS_PARSER_FSM								TS_FSM			
Type					RO								RO			
Reset					0	0	0	0	0				0	0	0	0

Bit(s)	Name	Description
27:24	FS_PARSER_FSM	FSM status in cdm_fs_parser
19:16	FS_FSM	FSM status in cdm_fs_fsm
12:8	TS_PARSER_FSM	FSM status in cdm_ts_parser
3:0	TS_FSM	FSM status in cdm_ts_fsm

15100330 FE_CDM7_DBG1 FE CDM7 Debug part1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CDM7_FS_RINF_LSB															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CDM7_FS_RINF_LSB															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CDM7_FS_RINF_LSB	CDM7 fs packet info [31:0]

15100334 FE_CDM7_DBG2 FE CDM7 Debug part2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CDM7_FS_RINF_MSB															

Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CDM7_FS_RINF_MSB															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CDM7_FS_RINF_MSB	CDM7 fs packet info [63:32]

15100338 FE_CDM7_FSM FE CDM7 FSM status 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FS_PARSER_FSM								FS_FSM							
Type	RO								RO							
Reset					0	0	0	0					0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TS_PARSER_FSM								TS_FSM							
Type	RO								RO							
Reset				0	0	0	0	0					0	0	0	0

Bit(s)	Name	Description
27:24	FS_PARSER_FSM	FSM status in cdm_fs_parser
19:16	FS_FSM	FSM status in cdm_fs_fsm
12:8	TS_PARSER_FSM	FSM status in cdm_ts_parser
3:0	TS_FSM	FSM status in cdm_ts_fsm

15100400 CDMP_IG_CTRL CDM Ingress Control 81000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CDM_TPID															
Type	RW															
Reset	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																STAG_EN
Type																RW
Reset																0

Bit(s)	Name	Description
31:16	CDM_TPID	Inserted VLAN TPID
0	STAG_EN	Special tag indication Indicate that the received packets is carrying the special tag from CPU.

15100404 CDM EG_CTRL CDM Egress Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											TACK2RING_ID		TACK2RING_EN			UNTAG_EN
Type											RW		RW			RW
Reset											0	0	0	0		0

Bit(s)	Name	Description
5:4	TACK2RING_ID	Force mode ring selection of TCP ACK to dedicate Rx Ring function
3:2	TACK2RING_EN	Enable TCP ACK to dedicate Rx Ring function
0	UNTAG_EN	VLAN un-tag Un-tag the egress packets which are transmitted from CDM to CPU

15100408 CDM PPE_GEN CDM PPPoE Generation 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																PPP_IN_S
Type																RW
Reset																0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SESS_ID															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	PPP_INS	PPPoE Header Insertion
15:0	SESS_ID	PPPoE Session ID

15100500 GDM1_IG_CTRL GDM Ingress Control 20717777

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REVO						INSV_EN	STAG_EN		GDM_ICSEN	GDM_TCSEN	GDM_UCSEN	DROP_256B			STRP_CRC
Type	RW						RW	RW		RW	RW	RW	RW			RW
Reset	0	0	1	0			0	0		1	1	1	0			1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MYMAC_DP				BC_DP				MC_DP				UN_DP			
Type	RW				RW				RW				RW			
Reset	0	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1

Bit(s)	Name	Description
31:28	REVO	Reserved
25	INSV_EN	VLAN insertion
24	STAG_EN	Insert Port VID on the received packets on the corresponding GDM port. Special tag indication Indicate that the received packets is carrying the special tag from GDM port.
22	GDM_ICSEN	IPv4 header checksum error drop
21	GDM_TCSEN	TCP checksum error drop
20	GDM_UCSEN	UDP checksum error drop
19	DROP_256B	A special mode to drop packets with payload > 256-bytes
16	STRP_CRC	GDM RX Stripping
15:12	MYMAC_DP	MY_MAC frames destination port
11:8	BC_DP	Broadcast frame destination port
7:4	MC_DP	Multicast frame destination port
3:0	UN_DP	Other frame destination port

15100504 GDM1 EG_CTRL GDM Egress Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		UNTAG_EN	DIS_PAD	DIS_CRC				SHPR_EN	BK_SIZE							
Type		RW	RW	RW				RW	RW							
Reset		0	0	0				0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TK_TICK		TK_RATE													
Type	RW		RW													
Reset	0		0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
30	UNTAG_EN	VLAN un-tag Un-tag the egress packets which are transmitted from GDM.
29	DIS_PAD	GMAC TX padding function
28	DIS_CRC	GMAC TX CRC generation
24	SHPR_EN	GDM output shaper enable
23:16	BK_SIZE	GDM output shaper bucket size. This unit is 1K-byte
15	TK_TICK	GDM shaper token period
13:0	TK_RATE	GDM output shaper token rate The unit is 8-Byte/ms or 8-Byte/20us according to TK_TICK.

15100508 GDM1 MAC_LSB GDM MY_MAC Address LSB 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAC_ADR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAC_ADR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MAC_ADR	MY_MAC Address [31:0]

Bit(s)	Name	Description

1510050C	GDM1 MAC_MSB				GDM MY_MAC Address_MSB								00000000			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAC_ADR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	MAC_ADR	MY_MAC Address [47:32]

15100510	GDM1 VLAN_GEN				GDM VLAN Generation								81000000			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GDM_TPID															
Type	RW															
Reset	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GDM_PRI			GDM_CFI	GDM_VID											
Type	RW			RW	RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	GDM_TPID	Inserted VLAN TPID
15:13	GDM_PRI	Inserted PRI
12	GDM_CFI	Inserted CFI
11:0	GDM_VID	Inserted VLAN ID

15100520 GDM1 DOS CFG 0

GDM DOS Configuration 0

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SPD_2P5G_MODE	ICMP_AND_TOS_EQ_ZERO	MY_MAC_CHECK						TCP_DROP_INTERRUPT_STATUS	TCP_RATE_LIMITER_RST	TCP_DROP_INTERRUPT_EN	TCP_SYN_PKT_DROP_EN	TCP_SYN_LIMIT_MODE	TCP_SYN_LIMIT_UNIT		
Type	RW	RW	RW						W1C	RW	RW	RW	RW	RW		
Reset	0	0	0						0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	UDP_DROP_INTERRUPT_STATUS	UDP_RATE_LIMITER_RST	UDP_DROP_INTERRUPT_EN	UDP_PKT_DROP_EN	UDP_LIMIT_MODE	UDP_LIMIT_UNIT			ICMP_DROP_INTERRUPT_STATUS	ICMP_RATE_LIMITER_RST	ICMP_DROP_INTERRUPT_EN	ICMP_PKT_DROP_EN	ICMP_LIMIT_MODE	ICMP_LIMIT_UNIT		
Type	W1C	RW	RW	RW	RW	RW			W1C	RW	RW	RW	RW	RW		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	SPD_2P5G_MODE	Reference *_LIMIT_2P5G Setting for Rate Limitation
30	ICMP_AND_TOS_EQ_ZERO	IPv4 ICMP Packet Recognition Control
29	MY_MAC_CHECK	MY MAC Address Check Control
23	TCP_DROP_INTERRUPT_STATUS	TCP Packet Drop Interrupt Event Status
22	TCP_RATE_LIMITER_RST	TCP Rate Limiter Reset Control
21	TCP_DROP_INTERRUPT_EN	TCP Packet Drop Interrupt Event Control
20	TCP_SYN_PKT_DROP_EN	TCP SYN Packet Drop Control when Reaching Rate Limitation
19	TCP_SYN_LIMIT_MODE	TCP SYN Rate Limitation Mode
18:16	TCP_SYN_LIMIT_UNIT	Unit of TCP SYN Rate Limitation
15	UDP_DROP_INTERRUPT_STATUS	UDP Packet Drop Interrupt Event Status
14	UDP_RATE_LIMITER_RST	UDP Rate Limiter Reset Control
13	UDP_DROP_INTERRUPT_EN	UDP Packet Drop Interrupt Event Control
12	UDP_PKT_DROP_EN	UDP Packet Drop Control when Reaching Rate Limitation
11	UDP_LIMIT_MODE	UDP Rate Limitation Mode
10:8	UDP_LIMIT_UNIT	Unit of UDP Rate Limitation
7	ICMP_DROP_INTERRUPT_STATUS	ICMP Packet Drop Interrupt Event Status
6	ICMP_RATE_LIMITER_RST	ICMP Rate Limiter Reset Control
5	ICMP_DROP_INTERRUPT_EN	ICMP Packet Drop Interrupt Event Control
4	ICMP_PKT_DROP_EN	ICMP Packet Drop Control when Reaching Rate Limitation
3	ICMP_LIMIT_MODE	ICMP Rate Limitation Mode
2:0	ICMP_LIMIT_UNIT	Unit of ICMP Rate Limitation

15100524 GDM1 DOS CFG 1

GDM DOS Configuration 1

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TCP_SYN_LIMIT_2P5G								TCP_SYN_LIMIT_1G							

Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TCP_SYN_LIMIT_100M								TCP_SYN_LIMIT_10M							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	TCP_SYN_LIMIT_2P5G	2500 Mbps TCP_SYN Rate Limit Control The TCP_SYN rate limit for 2500 Mbps link speed
23:16	TCP_SYN_LIMIT_1G	1000 Mbps TCP_SYN Rate Limit Control The TCP_SYN rate limit for 1000 Mbps link speed
15:8	TCP_SYN_LIMIT_100M	100 Mbps TCP_SYN Rate Limit Control The TCP_SYN rate limit for 100 Mbps link speed
7:0	TCP_SYN_LIMIT_10M	10 Mbps TCP_SYN Rate Limit Control The TCP_SYN rate limit for 10 Mbps link speed

15100528 GDM1_DOS_CFG_2 GDM DOS Configuration 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	UDP_LIMIT_2P5G								UDP_LIMIT_1G							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	UDP_LIMIT_100M								UDP_LIMIT_10M							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	UDP_LIMIT_2P5G	2500 Mbps UDP Rate Limit Control The UDP rate limit for 2500 Mbps link speed
23:16	UDP_LIMIT_1G	1000 Mbps UDP Rate Limit Control The UDP rate limit for 1000 Mbps link speed
15:8	UDP_LIMIT_100M	100 Mbps UDP Rate Limit Control The UDP rate limit for 100 Mbps link speed
7:0	UDP_LIMIT_10M	10 Mbps UDP Rate Limit Control The UDP rate limit for 10 Mbps link speed

1510052C GDM1_DOS_CFG_3 GDM DOS Configuration 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ICMP_LIMIT_2P5G								ICMP_LIMIT_1G							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ICMP_LIMIT_100M								ICMP_LIMIT_10M							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	ICMP_LIMIT_2P5G	2500 Mbps ICMP Rate Limit Control The ICMP rate limit for 2500 Mbps link speed
23:16	ICMP_LIMIT_1G	1000 Mbps ICMP Rate Limit Control The ICMP rate limit for 1000 Mbps link speed
15:8	ICMP_LIMIT_100M	100 Mbps ICMP Rate Limit Control The ICMP rate limit for 100 Mbps link speed
7:0	ICMP_LIMIT_10M	10 Mbps ICMP Rate Limit Control The ICMP rate limit for 10 Mbps link speed

15100C00 PFC_CFG_0 PFC GMAC1 Input Priority ReMap 0 08040201

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GMAC1_IN_PRI_3								GMAC1_IN_PRI_2							
Type	RW								RW							
Reset	0	0	0	0	1	0	0	0	0	0	0	0	0	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GMAC1_IN_PRI_1								GMAC1_IN_PRI_0							
Type	RW								RW							
Reset	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
31:24	GMAC1_IN_PRI_3	GMAC1 Input Priority Re-Map Selection for Priority 3
23:16	GMAC1_IN_PRI_2	GMAC1 Input Priority Re-Map Selection for Priority 2
15:8	GMAC1_IN_PRI_1	GMAC1 Input Priority Re-Map Selection for Priority 1
7:0	GMAC1_IN_PRI_0	GMAC1 Input Priority Re-Map Selection for Priority 0

15100C04 PFC_CFG_1 PFC GMAC1 Input Priority ReMap 1 80402010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GMAC1_IN_PRI_7								GMAC1_IN_PRI_6							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GMAC1_IN_PRI_5								GMAC1_IN_PRI_4							
Type	RW								RW							
Reset	0	0	1	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
31:24	GMAC1_IN_PRI_7	GMAC1 Input Priority Re-Map Selection for Priority 7
23:16	GMAC1_IN_PRI_6	GMAC1 Input Priority Re-Map Selection for Priority 6
15:8	GMAC1_IN_PRI_5	GMAC1 Input Priority Re-Map Selection for Priority 5
7:0	GMAC1_IN_PRI_4	GMAC1 Input Priority Re-Map Selection for Priority 4

15100C08 PFC_CFG_2 PFC GMAC2 Input Priority ReMap 0 08040201

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GMAC2_IN_PRI_3								GMAC2_IN_PRI_2							
Type	RW								RW							
Reset	0	0	0	0	1	0	0	0	0	0	0	0	0	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GMAC2_IN_PRI_1								GMAC2_IN_PRI_0							
Type	RW								RW							
Reset	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
31:24	GMAC2_IN_PRI_3	GMAC2 Input Priority Re-Map Selection for Priority 3
23:16	GMAC2_IN_PRI_2	GMAC2 Input Priority Re-Map Selection for Priority 2
15:8	GMAC2_IN_PRI_1	GMAC2 Input Priority Re-Map Selection for Priority 1
7:0	GMAC2_IN_PRI_0	GMAC2 Input Priority Re-Map Selection for Priority 0

15100C0C PFC_CFG_3 PFC GMAC2 Input Priority ReMap 1 80402010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GMAC2_IN_PRI_7								GMAC2_IN_PRI_6							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GMAC2_IN_PRI_5								GMAC2_IN_PRI_4							
Type	RW								RW							
Reset	0	0	1	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
31:24	GMAC2_IN_PRI_7	GMAC2 Input Priority Re-Map Selection for Priority 7
23:16	GMAC2_IN_PRI_6	GMAC2 Input Priority Re-Map Selection for Priority 6
15:8	GMAC2_IN_PRI_5	GMAC2 Input Priority Re-Map Selection for Priority 5
7:0	GMAC2_IN_PRI_4	GMAC2 Input Priority Re-Map Selection for Priority 4

15100C10 PFC_CFG_4 PFC_WDMA0_1 Input Priority ReMap 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WDMA1_IN_P RI_7		WDMA1_IN_P RI_6		WDMA1_IN_P RI_5		WDMA1_IN_P RI_4		WDMA1_IN_P RI_3		WDMA1_IN_P RI_2		WDMA1_IN_P RI_1		WDMA1_IN_P RI_0	
Type	RW		RW		RW		RW		RW		RW		RW		RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WDMA0_IN_P RI_7		WDMA0_IN_P RI_6		WDMA0_IN_P RI_5		WDMA0_IN_P RI_4		WDMA0_IN_P RI_3		WDMA0_IN_P RI_2		WDMA0_IN_P RI_1		WDMA0_IN_P RI_0	
Type	RW		RW		RW		RW		RW		RW		RW		RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:30	WDMA1_IN_PRI_7	WDMA1 Input Priority Re-Map Selection for Priority 7
29:28	WDMA1_IN_PRI_6	WDMA1 Input Priority Re-Map Selection for Priority 6
27:26	WDMA1_IN_PRI_5	WDMA1 Input Priority Re-Map Selection for Priority 5
25:24	WDMA1_IN_PRI_4	WDMA1 Input Priority Re-Map Selection for Priority 4
23:22	WDMA1_IN_PRI_3	WDMA1 Input Priority Re-Map Selection for Priority 3
21:20	WDMA1_IN_PRI_2	WDMA1 Input Priority Re-Map Selection for Priority 2
19:18	WDMA1_IN_PRI_1	WDMA1 Input Priority Re-Map Selection for Priority 1
17:16	WDMA1_IN_PRI_0	WDMA1 Input Priority Re-Map Selection for Priority 0
15:14	WDMA0_IN_PRI_7	WDMA0 Input Priority Re-Map Selection for Priority 7

Bit(s)	Name	Description
13:12	WDMA0_IN_PRI_6	WDMA0 Input Priority Re-Map Selection for Priority 6
11:10	WDMA0_IN_PRI_5	WDMA0 Input Priority Re-Map Selection for Priority 5
9:8	WDMA0_IN_PRI_4	WDMA0 Input Priority Re-Map Selection for Priority 4
7:6	WDMA0_IN_PRI_3	WDMA0 Input Priority Re-Map Selection for Priority 3
5:4	WDMA0_IN_PRI_2	WDMA0 Input Priority Re-Map Selection for Priority 2
3:2	WDMA0_IN_PRI_1	WDMA0 Input Priority Re-Map Selection for Priority 1
1:0	WDMA0_IN_PRI_0	WDMA0 Input Priority Re-Map Selection for Priority 0

15100C60 PFC_CFG_5 PFC QDMA Input Priority ReMap 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_IN_PRI_0_31_0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_IN_PRI_0_31_0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	QDMA_IN_PRI_0_31_0	QDMA Input Priority Re-Map Selection for Priority 0 [31:0]

15100C64 PFC_CFG_6 PFC QDMA Input Priority ReMap 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_IN_PRI_0_63_32															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_IN_PRI_0_63_32															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	QDMA_IN_PRI_0_63_32	QDMA Input Priority Re-Map Selection for Priority 0 [63:32]

Bit(s)	Name	Description

15100C68 PFC_CFG_7 PFC QDMA Input Priority ReMap 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_IN_PRI_0_95_64															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_IN_PRI_0_95_64															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	QDMA_IN_PRI_0_95_64	QDMA Input Priority Re-Map Selection for Priority 0 [95:64]

15100C6C PFC_CFG_8 PFC QDMA Input Priority ReMap 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_IN_PRI_0_127_96															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_IN_PRI_0_127_96															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	QDMA_IN_PRI_0_127_96	QDMA Input Priority Re-Map Selection for Priority 0 [127:96]

15100C70 PFC_CFG_9 PFC QDMA Input Priority ReMap 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	QDMA_IN_PRI_1_31_0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_IN_PRI_1_31_0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	QDMA_IN_PRI_1_31_0	QDMA Input Priority Re-Map Selection for Priority 1 [31:0]

15100C74 PFC_CFG_10 PFC QDMA Input Priority ReMap 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_IN_PRI_1_63_32															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_IN_PRI_1_63_32															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	QDMA_IN_PRI_1_63_32	QDMA Input Priority Re-Map Selection for Priority 1 [63:32]

15100C78 PFC_CFG_11 PFC QDMA Input Priority ReMap 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_IN_PRI_1_95_64															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	QDMA_IN_PRI_1_95_64															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	QDMA_IN_PRI_1_95_64	QDMA Input Priority Re-Map Selection for Priority 1 [95:64]

15100C7C PFC_CFG_12 PFC QDMA Input Priority ReMap 7 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_IN_PRI_1_127_96															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_IN_PRI_1_127_96															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	QDMA_IN_PRI_1_127_96	QDMA Input Priority Re-Map Selection for Priority 1 [127:96]

15100C80 PFC_CFG_13 PFC QDMA Input Priority ReMap 8 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_IN_PRI_2_31_0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_IN_PRI_2_31_0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	QDMA_IN_PRI_2_31_0	QDMA Input Priority Re-Map Selection for Priority 2 [31:0]

15100C84 PFC_CFG_14 PFC QDMA Input Priority ReMap 9 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_IN_PRI_2_63_32															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_IN_PRI_2_63_32															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	QDMA_IN_PRI_2_63_32	QDMA Input Priority Re-Map Selection for Priority 2 [63:32]

15100C88 PFC_CFG_15 PFC QDMA Input Priority ReMap 10 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_IN_PRI_2_95_64															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_IN_PRI_2_95_64															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	QDMA_IN_PRI_2_95_64	QDMA Input Priority Re-Map Selection for Priority 2 [95:64]

15100C8C PFC_CFG_16 PFC QDMA Input Priority ReMap 11 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	QDMA_IN_PRI_2_127_96															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_IN_PRI_2_127_96															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	QDMA_IN_PRI_2_127_96	QDMA Input Priority Re-Map Selection for Priority 2 [127:96]

15100C90 PFC_CFG_17 PFC QDMA Input Priority ReMap 12 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_IN_PRI_3_31_0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_IN_PRI_3_31_0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	QDMA_IN_PRI_3_31_0	QDMA Input Priority Re-Map Selection for Priority 3 [31:0]

15100C94 PFC_CFG_18 PFC QDMA Input Priority ReMap 13 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_IN_PRI_3_63_32															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	QDMA_IN_PRI_3_63_32															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	QDMA_IN_PRI_3_63_32	QDMA Input Priority Re-Map Selection for Priority 3 [63:32]

15100C98 PFC_CFG_19 PFC QDMA Input Priority ReMap 14 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_IN_PRI_3_95_64															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_IN_PRI_3_95_64															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	QDMA_IN_PRI_3_95_64	QDMA Input Priority Re-Map Selection for Priority 3 [95:64]

15100C9C PFC_CFG_20 PFC QDMA Input Priority ReMap 15 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_IN_PRI_3_127_96															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_IN_PRI_3_127_96															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	QDMA_IN_PRI_3_127_96	QDMA Input Priority Re-Map Selection for Priority 3 [127:96]

15100CA0 PFC_CFG_21 PFC QDMA Input Priority ReMap 16 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_IN_PRI_4_31_0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_IN_PRI_4_31_0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	QDMA_IN_PRI_4_31_0	QDMA Input Priority Re-Map Selection for Priority 4 [31:0]

15100CA4 PFC_CFG_22 PFC QDMA Input Priority ReMap 17 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_IN_PRI_4_63_32															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_IN_PRI_4_63_32															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	QDMA_IN_PRI_4_63_32	QDMA Input Priority Re-Map Selection for Priority 4 [63:32]

15100CA8 PFC_CFG_23 PFC QDMA Input Priority ReMap 18 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	QDMA_IN_PRI_4_95_64															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_IN_PRI_4_95_64															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	QDMA_IN_PRI_4_95_64	QDMA Input Priority Re-Map Selection for Priority 4 [95:64]

15100CAC PFC_CFG_24 PFC QDMA Input Priority ReMap 19 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_IN_PRI_4_127_96															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_IN_PRI_4_127_96															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	QDMA_IN_PRI_4_127_96	QDMA Input Priority Re-Map Selection for Priority 4 [127:96]

15100CB0 PFC_CFG_25 PFC QDMA Input Priority ReMap 20 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_IN_PRI_5_31_0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	QDMA_IN_PRI_5_31_0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	QDMA_IN_PRI_5_31_0	QDMA Input Priority Re-Map Selection for Priority 5 [31:0]

15100CB4 PFC_CFG_26 PFC QDMA Input Priority ReMap 21 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_IN_PRI_5_63_32															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_IN_PRI_5_63_32															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	QDMA_IN_PRI_5_63_32	QDMA Input Priority Re-Map Selection for Priority 5 [63:32]

15100CB8 PFC_CFG_27 PFC QDMA Input Priority ReMap 22 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_IN_PRI_5_95_64															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_IN_PRI_5_95_64															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	QDMA_IN_PRI_5_95_64	QDMA Input Priority Re-Map Selection for Priority 5 [95:64]

15100CBC PFC_CFG_28 PFC QDMA Input Priority ReMap 23 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_IN_PRI_5_127_96															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_IN_PRI_5_127_96															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	QDMA_IN_PRI_5_127_96	QDMA Input Priority Re-Map Selection for Priority 5 [127:96]

15100CC0 PFC_CFG_29 PFC QDMA Input Priority ReMap 24 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_IN_PRI_6_31_0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_IN_PRI_6_31_0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	QDMA_IN_PRI_6_31_0	QDMA Input Priority Re-Map Selection for Priority 6 [31:0]

15100CC4 PFC_CFG_30 PFC QDMA Input Priority ReMap 25 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	QDMA_IN_PRI_6_63_32															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_IN_PRI_6_63_32															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	QDMA_IN_PRI_6_63_32	QDMA Input Priority Re-Map Selection for Priority 6 [63:32]

15100CC8 PFC_CFG_31 PFC QDMA Input Priority ReMap 26 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_IN_PRI_6_95_64															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_IN_PRI_6_95_64															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	QDMA_IN_PRI_6_95_64	QDMA Input Priority Re-Map Selection for Priority 6 [95:64]

15100CCC PFC_CFG_32 PFC QDMA Input Priority ReMap 27 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_IN_PRI_6_127_96															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	QDMA_IN_PRI_6_127_96															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	QDMA_IN_PRI_6_127_96	QDMA Input Priority Re-Map Selection for Priority 6 [127:96]

15100CD0 PFC_CFG 33 PFC QDMA Input Priority ReMap 28 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_IN_PRI_7_31_0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_IN_PRI_7_31_0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	QDMA_IN_PRI_7_31_0	QDMA Input Priority Re-Map Selection for Priority 7 [31:0]

15100CD4 PFC_CFG 34 PFC QDMA Input Priority ReMap 29 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_IN_PRI_7_63_32															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_IN_PRI_7_63_32															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	QDMA_IN_PRI_7_63_32	QDMA Input Priority Re-Map Selection for Priority 7 [63:32]

15100CD8 PFC_CFG_35 PFC QDMA Input Priority ReMap 30 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_IN_PRI_7_95_64															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_IN_PRI_7_95_64															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	QDMA_IN_PRI_7_95_64	QDMA Input Priority Re-Map Selection for Priority 7 [95:64]

15100CDC PFC_CFG_36 PFC QDMA Input Priority ReMap 31 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_IN_PRI_7_127_96															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_IN_PRI_7_127_96															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	QDMA_IN_PRI_7_127_96	QDMA Input Priority Re-Map Selection for Priority 7 [127:96]

15100D60 PFC_CFG_37 PFC GMAC1 Output Priority ReMap 0 08040201

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	GMAC1_OUT_PRI_Q_3								GMAC1_OUT_PRI_Q_2							
Type	RW								RW							
Reset	0	0	0	0	1	0	0	0	0	0	0	0	0	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GMAC1_OUT_PRI_Q_1								GMAC1_OUT_PRI_Q_0							
Type	RW								RW							
Reset	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
31:24	GMAC1_OUT_PRI_Q_3	GMAC1 Output Priority Queue 3 Re-Map Selection
23:16	GMAC1_OUT_PRI_Q_2	GMAC1 Output Priority Queue 2 Re-Map Selection
15:8	GMAC1_OUT_PRI_Q_1	GMAC1 Output Priority Queue 1 Re-Map Selection
7:0	GMAC1_OUT_PRI_Q_0	GMAC1 Output Priority Queue 0 Re-Map Selection

15100D64 PFC_CFG_38 PFC GMAC1 Output Priority ReMap 1 80402010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GMAC1_OUT_PRI_Q_7								GMAC1_OUT_PRI_Q_6							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GMAC1_OUT_PRI_Q_5								GMAC1_OUT_PRI_Q_4							
Type	RW								RW							
Reset	0	0	1	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
31:24	GMAC1_OUT_PRI_Q_7	GMAC1 Output Priority Queue 7 Re-Map Selection
23:16	GMAC1_OUT_PRI_Q_6	GMAC1 Output Priority Queue 6 Re-Map Selection
15:8	GMAC1_OUT_PRI_Q_5	GMAC1 Output Priority Queue 5 Re-Map Selection
7:0	GMAC1_OUT_PRI_Q_4	GMAC1 Output Priority Queue 4 Re-Map Selection

15100D68 PFC_CFG_39 PFC GMAC2 Output Priority ReMap 0 08040201

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GMAC2_OUT_PRI_Q_3								GMAC2_OUT_PRI_Q_2							

Type	RW								RW							
Reset	0	0	0	0	1	0	0	0	0	0	0	0	0	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GMAC2_OUT_PRI_Q_1								GMAC2_OUT_PRI_Q_0							
Type	RW								RW							
Reset	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
31:24	GMAC2_OUT_PRI_Q_3	GMAC2 Output Priority Queue 3 Re-Map Selection
23:16	GMAC2_OUT_PRI_Q_2	GMAC2 Output Priority Queue 2 Re-Map Selection
15:8	GMAC2_OUT_PRI_Q_1	GMAC2 Output Priority Queue 1 Re-Map Selection
7:0	GMAC2_OUT_PRI_Q_0	GMAC2 Output Priority Queue 0 Re-Map Selection

15100D6C PFC_CFG_40 PFC GMAC2 Output Priority ReMap 1 80402010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GMAC2_OUT_PRI_Q_7								GMAC2_OUT_PRI_Q_6							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GMAC2_OUT_PRI_Q_5								GMAC2_OUT_PRI_Q_4							
Type	RW								RW							
Reset	0	0	1	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
31:24	GMAC2_OUT_PRI_Q_7	GMAC2 Output Priority Queue 7 Re-Map Selection
23:16	GMAC2_OUT_PRI_Q_6	GMAC2 Output Priority Queue 6 Re-Map Selection
15:8	GMAC2_OUT_PRI_Q_5	GMAC2 Output Priority Queue 5 Re-Map Selection
7:0	GMAC2_OUT_PRI_Q_4	GMAC2 Output Priority Queue 4 Re-Map Selection

15100D70 PFC_CFG_41 PFC WDMA0 Output Priority ReMap 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WDMA0_OUT_PRI_Q_3								WDMA0_OUT_PRI_Q_2							
Type	RW								RW							

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WDMA0_OUT_PRI_Q_1								WDMA0_OUT_PRI_Q_0							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	WDMA0_OUT_PRI_Q_3	WDMA0 Output Priority Queue 3 Re-Map Selection
23:16	WDMA0_OUT_PRI_Q_2	WDMA0 Output Priority Queue 2 Re-Map Selection
15:8	WDMA0_OUT_PRI_Q_1	WDMA0 Output Priority Queue 1 Re-Map Selection
7:0	WDMA0_OUT_PRI_Q_0	WDMA0 Output Priority Queue 0 Re-Map Selection

15100D74 PFC_CFG_42 PFC WDMA1 Output Priority ReMap 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WDMA1_OUT_PRI_Q_3								WDMA1_OUT_PRI_Q_2							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WDMA1_OUT_PRI_Q_1								WDMA1_OUT_PRI_Q_0							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	WDMA1_OUT_PRI_Q_3	WDMA1 Output Priority Queue 3 Re-Map Selection
23:16	WDMA1_OUT_PRI_Q_2	WDMA1 Output Priority Queue 2 Re-Map Selection
15:8	WDMA1_OUT_PRI_Q_1	WDMA1 Output Priority Queue 1 Re-Map Selection
7:0	WDMA1_OUT_PRI_Q_0	WDMA1 Output Priority Queue 0 Re-Map Selection

15100DA0 PFC_CFG_43 PFC QDMA Output Priority ReMap 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_OUT_PRI_Q_3								QDMA_OUT_PRI_Q_2							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_OUT_PRI_Q_1								QDMA_OUT_PRI_Q_0							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	QDMA_OUT_PRI_Q_3	QDMA Output Priority Queue 3 Re-Map Selection
23:16	QDMA_OUT_PRI_Q_2	QDMA Output Priority Queue 2 Re-Map Selection
15:8	QDMA_OUT_PRI_Q_1	QDMA Output Priority Queue 1 Re-Map Selection
7:0	QDMA_OUT_PRI_Q_0	QDMA Output Priority Queue 0 Re-Map Selection

15100DA4 PFC_CFG_44 PFC QDMA Output Priority ReMap 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_OUT_PRI_Q_7								QDMA_OUT_PRI_Q_6							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_OUT_PRI_Q_5								QDMA_OUT_PRI_Q_4							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	QDMA_OUT_PRI_Q_7	QDMA Output Priority Queue 7 Re-Map Selection
23:16	QDMA_OUT_PRI_Q_6	QDMA Output Priority Queue 6 Re-Map Selection
15:8	QDMA_OUT_PRI_Q_5	QDMA Output Priority Queue 5 Re-Map Selection
7:0	QDMA_OUT_PRI_Q_4	QDMA Output Priority Queue 4 Re-Map Selection

15100DA8 PFC_CFG_45 PFC QDMA Output Priority ReMap 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_OUT_PRI_Q_11								QDMA_OUT_PRI_Q_10							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	QDMA_OUT_PRI_Q_9								QDMA_OUT_PRI_Q_8							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	QDMA_OUT_PRI_Q_11	QDMA Output Priority Queue 11 Re-Map Selection
23:16	QDMA_OUT_PRI_Q_10	QDMA Output Priority Queue 10 Re-Map Selection
15:8	QDMA_OUT_PRI_Q_9	QDMA Output Priority Queue 9 Re-Map Selection
7:0	QDMA_OUT_PRI_Q_8	QDMA Output Priority Queue 8 Re-Map Selection

15100DAC PFC_CFG_46 PFC QDMA Output Priority ReMap 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_OUT_PRI_Q_15								QDMA_OUT_PRI_Q_14							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_OUT_PRI_Q_13								QDMA_OUT_PRI_Q_12							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	QDMA_OUT_PRI_Q_15	QDMA Output Priority Queue 15 Re-Map Selection
23:16	QDMA_OUT_PRI_Q_14	QDMA Output Priority Queue 14 Re-Map Selection
15:8	QDMA_OUT_PRI_Q_13	QDMA Output Priority Queue 13 Re-Map Selection
7:0	QDMA_OUT_PRI_Q_12	QDMA Output Priority Queue 12 Re-Map Selection

15100DB0 PFC_CFG_47 PFC QDMA Output Priority ReMap 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_OUT_PRI_Q_19								QDMA_OUT_PRI_Q_18							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_OUT_PRI_Q_17								QDMA_OUT_PRI_Q_16							

Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	QDMA_OUT_PRI_Q_19	QDMA Output Priority Queue 19 Re-Map Selection
23:16	QDMA_OUT_PRI_Q_18	QDMA Output Priority Queue 18 Re-Map Selection
15:8	QDMA_OUT_PRI_Q_17	QDMA Output Priority Queue 17 Re-Map Selection
7:0	QDMA_OUT_PRI_Q_16	QDMA Output Priority Queue 16 Re-Map Selection

15100DB4 PFC_CFG_48 PFC QDMA Output Priority ReMap 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_OUT_PRI_Q_23								QDMA_OUT_PRI_Q_22							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_OUT_PRI_Q_21								QDMA_OUT_PRI_Q_20							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	QDMA_OUT_PRI_Q_23	QDMA Output Priority Queue 23 Re-Map Selection
23:16	QDMA_OUT_PRI_Q_22	QDMA Output Priority Queue 22 Re-Map Selection
15:8	QDMA_OUT_PRI_Q_21	QDMA Output Priority Queue 21 Re-Map Selection
7:0	QDMA_OUT_PRI_Q_20	QDMA Output Priority Queue 20 Re-Map Selection

15100DB8 PFC_CFG_49 PFC QDMA Output Priority ReMap 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_OUT_PRI_Q_27								QDMA_OUT_PRI_Q_26							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_OUT_PRI_Q_25								QDMA_OUT_PRI_Q_24							
Type	RW								RW							

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	QDMA_OUT_PRI_Q_27	QDMA Output Priority Queue 27 Re-Map Selection
23:16	QDMA_OUT_PRI_Q_26	QDMA Output Priority Queue 26 Re-Map Selection
15:8	QDMA_OUT_PRI_Q_25	QDMA Output Priority Queue 25 Re-Map Selection
7:0	QDMA_OUT_PRI_Q_24	QDMA Output Priority Queue 24 Re-Map Selection

15100DBC PFC_CFG_50 PFC QDMA Output Priority ReMap 7 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_OUT_PRI_Q_31								QDMA_OUT_PRI_Q_30							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_OUT_PRI_Q_29								QDMA_OUT_PRI_Q_28							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	QDMA_OUT_PRI_Q_31	QDMA Output Priority Queue 31 Re-Map Selection
23:16	QDMA_OUT_PRI_Q_30	QDMA Output Priority Queue 30 Re-Map Selection
15:8	QDMA_OUT_PRI_Q_29	QDMA Output Priority Queue 29 Re-Map Selection
7:0	QDMA_OUT_PRI_Q_28	QDMA Output Priority Queue 28 Re-Map Selection

15100DC0 PFC_CFG_51 PFC QDMA Output Priority ReMap 8 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_OUT_PRI_Q_35								QDMA_OUT_PRI_Q_34							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_OUT_PRI_Q_33								QDMA_OUT_PRI_Q_32							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	QDMA_OUT_PRI_Q_35	QDMA Output Priority Queue 35 Re-Map Selection
23:16	QDMA_OUT_PRI_Q_34	QDMA Output Priority Queue 34 Re-Map Selection
15:8	QDMA_OUT_PRI_Q_33	QDMA Output Priority Queue 33 Re-Map Selection
7:0	QDMA_OUT_PRI_Q_32	QDMA Output Priority Queue 32 Re-Map Selection

15100DC4 PFC_CFG_52 PFC QDMA Output Priority ReMap 9 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_OUT_PRI_Q_39								QDMA_OUT_PRI_Q_38							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_OUT_PRI_Q_37								QDMA_OUT_PRI_Q_36							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	QDMA_OUT_PRI_Q_39	QDMA Output Priority Queue 39 Re-Map Selection
23:16	QDMA_OUT_PRI_Q_38	QDMA Output Priority Queue 38 Re-Map Selection
15:8	QDMA_OUT_PRI_Q_37	QDMA Output Priority Queue 37 Re-Map Selection
7:0	QDMA_OUT_PRI_Q_36	QDMA Output Priority Queue 36 Re-Map Selection

15100DC8 PFC_CFG_53 PFC QDMA Output Priority ReMap 10 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_OUT_PRI_Q_43								QDMA_OUT_PRI_Q_42							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_OUT_PRI_Q_41								QDMA_OUT_PRI_Q_40							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	QDMA_OUT_PRI_Q_43	QDMA Output Priority Queue 43 Re-Map Selection

Bit(s)	Name	Description
23:16	QDMA_OUT_PRI_Q_42	QDMA Output Priority Queue 42 Re-Map Selection
15:8	QDMA_OUT_PRI_Q_41	QDMA Output Priority Queue 41 Re-Map Selection
7:0	QDMA_OUT_PRI_Q_40	QDMA Output Priority Queue 40 Re-Map Selection

15100DCC PFC_CFG_54 PFC QDMA Output Priority ReMap 11 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_OUT_PRI_Q_47								QDMA_OUT_PRI_Q_46							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_OUT_PRI_Q_45								QDMA_OUT_PRI_Q_44							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	QDMA_OUT_PRI_Q_47	QDMA Output Priority Queue 47 Re-Map Selection
23:16	QDMA_OUT_PRI_Q_46	QDMA Output Priority Queue 46 Re-Map Selection
15:8	QDMA_OUT_PRI_Q_45	QDMA Output Priority Queue 45 Re-Map Selection
7:0	QDMA_OUT_PRI_Q_44	QDMA Output Priority Queue 44 Re-Map Selection

15100DD0 PFC_CFG_55 PFC QDMA Output Priority ReMap 12 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_OUT_PRI_Q_51								QDMA_OUT_PRI_Q_50							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_OUT_PRI_Q_49								QDMA_OUT_PRI_Q_48							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	QDMA_OUT_PRI_Q_51	QDMA Output Priority Queue 51 Re-Map Selection
23:16	QDMA_OUT_PRI_Q_50	QDMA Output Priority Queue 50 Re-Map Selection

Bit(s)	Name	Description
15:8	QDMA_OUT_PRI_Q_49	QDMA Output Priority Queue 49 Re-Map Selection
7:0	QDMA_OUT_PRI_Q_48	QDMA Output Priority Queue 48 Re-Map Selection

15100DD4 PFC_CFG_56 PFC QDMA Output Priority ReMap 13 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_OUT_PRI_Q_55								QDMA_OUT_PRI_Q_54							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_OUT_PRI_Q_53								QDMA_OUT_PRI_Q_52							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	QDMA_OUT_PRI_Q_55	QDMA Output Priority Queue 55 Re-Map Selection
23:16	QDMA_OUT_PRI_Q_54	QDMA Output Priority Queue 54 Re-Map Selection
15:8	QDMA_OUT_PRI_Q_53	QDMA Output Priority Queue 53 Re-Map Selection
7:0	QDMA_OUT_PRI_Q_52	QDMA Output Priority Queue 52 Re-Map Selection

15100DD8 PFC_CFG_57 PFC QDMA Output Priority ReMap 14 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_OUT_PRI_Q_59								QDMA_OUT_PRI_Q_58							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_OUT_PRI_Q_57								QDMA_OUT_PRI_Q_56							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	QDMA_OUT_PRI_Q_59	QDMA Output Priority Queue 59 Re-Map Selection
23:16	QDMA_OUT_PRI_Q_58	QDMA Output Priority Queue 58 Re-Map Selection
15:8	QDMA_OUT_PRI_Q_57	QDMA Output Priority Queue 57 Re-Map Selection

Bit(s)	Name	Description
7:0	QDMA_OUT_PRI_Q_56	QDMA Output Priority Queue 56 Re-Map Selection

15100DDC PFC_CFG_58 PFC QDMA Output Priority ReMap 15 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_OUT_PRI_Q_63								QDMA_OUT_PRI_Q_62							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_OUT_PRI_Q_61								QDMA_OUT_PRI_Q_60							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	QDMA_OUT_PRI_Q_63	QDMA Output Priority Queue 63 Re-Map Selection
23:16	QDMA_OUT_PRI_Q_62	QDMA Output Priority Queue 62 Re-Map Selection
15:8	QDMA_OUT_PRI_Q_61	QDMA Output Priority Queue 61 Re-Map Selection
7:0	QDMA_OUT_PRI_Q_60	QDMA Output Priority Queue 60 Re-Map Selection

15100DE0 PFC_CFG_59 PFC QDMA Output Priority ReMap 16 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_OUT_PRI_Q_67								QDMA_OUT_PRI_Q_66							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_OUT_PRI_Q_65								QDMA_OUT_PRI_Q_64							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	QDMA_OUT_PRI_Q_67	QDMA Output Priority Queue 67 Re-Map Selection
23:16	QDMA_OUT_PRI_Q_66	QDMA Output Priority Queue 66 Re-Map Selection
15:8	QDMA_OUT_PRI_Q_65	QDMA Output Priority Queue 65 Re-Map Selection
7:0	QDMA_OUT_PRI_Q_64	QDMA Output Priority Queue 64 Re-Map Selection

Bit(s)	Name	Description

15100DE4 PFC_CFG_60 PFC QDMA Output Priority ReMap 17 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_OUT_PRI_Q_71								QDMA_OUT_PRI_Q_70							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_OUT_PRI_Q_69								QDMA_OUT_PRI_Q_68							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	QDMA_OUT_PRI_Q_71	QDMA Output Priority Queue 71 Re-Map Selection
23:16	QDMA_OUT_PRI_Q_70	QDMA Output Priority Queue 70 Re-Map Selection
15:8	QDMA_OUT_PRI_Q_69	QDMA Output Priority Queue 69 Re-Map Selection
7:0	QDMA_OUT_PRI_Q_68	QDMA Output Priority Queue 68 Re-Map Selection

15100DE8 PFC_CFG_61 PFC QDMA Output Priority ReMap 18 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_OUT_PRI_Q_75								QDMA_OUT_PRI_Q_74							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_OUT_PRI_Q_73								QDMA_OUT_PRI_Q_72							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	QDMA_OUT_PRI_Q_75	QDMA Output Priority Queue 75 Re-Map Selection
23:16	QDMA_OUT_PRI_Q_74	QDMA Output Priority Queue 74 Re-Map Selection
15:8	QDMA_OUT_PRI_Q_73	QDMA Output Priority Queue 73 Re-Map Selection
7:0	QDMA_OUT_PRI_Q_72	QDMA Output Priority Queue 72 Re-Map Selection

15100DEC PFC_CFG_62 PFC QDMA Output Priority ReMap 19 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_OUT_PRI_Q_79								QDMA_OUT_PRI_Q_78							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_OUT_PRI_Q_77								QDMA_OUT_PRI_Q_76							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	QDMA_OUT_PRI_Q_79	QDMA Output Priority Queue 79 Re-Map Selection
23:16	QDMA_OUT_PRI_Q_78	QDMA Output Priority Queue 78 Re-Map Selection
15:8	QDMA_OUT_PRI_Q_77	QDMA Output Priority Queue 77 Re-Map Selection
7:0	QDMA_OUT_PRI_Q_76	QDMA Output Priority Queue 76 Re-Map Selection

15100DF0 PFC_CFG_63 PFC QDMA Output Priority ReMap 20 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_OUT_PRI_Q_83								QDMA_OUT_PRI_Q_82							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_OUT_PRI_Q_81								QDMA_OUT_PRI_Q_80							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	QDMA_OUT_PRI_Q_83	QDMA Output Priority Queue 83 Re-Map Selection
23:16	QDMA_OUT_PRI_Q_82	QDMA Output Priority Queue 82 Re-Map Selection
15:8	QDMA_OUT_PRI_Q_81	QDMA Output Priority Queue 81 Re-Map Selection
7:0	QDMA_OUT_PRI_Q_80	QDMA Output Priority Queue 80 Re-Map Selection

15100DF4 PFC_CFG_64 PFC QDMA Output Priority ReMap 21 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_OUT_PRI_Q_87								QDMA_OUT_PRI_Q_86							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_OUT_PRI_Q_85								QDMA_OUT_PRI_Q_84							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	QDMA_OUT_PRI_Q_87	QDMA Output Priority Queue 87 Re-Map Selection
23:16	QDMA_OUT_PRI_Q_86	QDMA Output Priority Queue 86 Re-Map Selection
15:8	QDMA_OUT_PRI_Q_85	QDMA Output Priority Queue 85 Re-Map Selection
7:0	QDMA_OUT_PRI_Q_84	QDMA Output Priority Queue 84 Re-Map Selection

15100DF8 PFC_CFG_65 PFC QDMA Output Priority ReMap 22 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_OUT_PRI_Q_91								QDMA_OUT_PRI_Q_90							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_OUT_PRI_Q_89								QDMA_OUT_PRI_Q_88							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	QDMA_OUT_PRI_Q_91	QDMA Output Priority Queue 91 Re-Map Selection
23:16	QDMA_OUT_PRI_Q_90	QDMA Output Priority Queue 90 Re-Map Selection
15:8	QDMA_OUT_PRI_Q_89	QDMA Output Priority Queue 89 Re-Map Selection
7:0	QDMA_OUT_PRI_Q_88	QDMA Output Priority Queue 88 Re-Map Selection

15100DFC PFC_CFG_66 PFC QDMA Output Priority ReMap 23 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	QDMA_OUT_PRI_Q_95								QDMA_OUT_PRI_Q_94							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_OUT_PRI_Q_93								QDMA_OUT_PRI_Q_92							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	QDMA_OUT_PRI_Q_95	QDMA Output Priority Queue 95 Re-Map Selection
23:16	QDMA_OUT_PRI_Q_94	QDMA Output Priority Queue 94 Re-Map Selection
15:8	QDMA_OUT_PRI_Q_93	QDMA Output Priority Queue 93 Re-Map Selection
7:0	QDMA_OUT_PRI_Q_92	QDMA Output Priority Queue 92 Re-Map Selection

15100E00 PFC_CFG_67 PFC QDMA Output Priority ReMap 24 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_OUT_PRI_Q_99								QDMA_OUT_PRI_Q_98							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_OUT_PRI_Q_97								QDMA_OUT_PRI_Q_96							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	QDMA_OUT_PRI_Q_99	QDMA Output Priority Queue 99 Re-Map Selection
23:16	QDMA_OUT_PRI_Q_98	QDMA Output Priority Queue 98 Re-Map Selection
15:8	QDMA_OUT_PRI_Q_97	QDMA Output Priority Queue 97 Re-Map Selection
7:0	QDMA_OUT_PRI_Q_96	QDMA Output Priority Queue 96 Re-Map Selection

15100E04 PFC_CFG_68 PFC QDMA Output Priority ReMap 25 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_OUT_PRI_Q_103								QDMA_OUT_PRI_Q_102							

Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_OUT_PRI_Q_101								QDMA_OUT_PRI_Q_100							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	QDMA_OUT_PRI_Q_103	QDMA Output Priority Queue 103 Re-Map Selection
23:16	QDMA_OUT_PRI_Q_102	QDMA Output Priority Queue 102 Re-Map Selection
15:8	QDMA_OUT_PRI_Q_101	QDMA Output Priority Queue 101 Re-Map Selection
7:0	QDMA_OUT_PRI_Q_100	QDMA Output Priority Queue 100 Re-Map Selection

15100E08 PFC_CFG_69 PFC QDMA Output Priority ReMap 26 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_OUT_PRI_Q_107								QDMA_OUT_PRI_Q_106							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_OUT_PRI_Q_105								QDMA_OUT_PRI_Q_104							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	QDMA_OUT_PRI_Q_107	QDMA Output Priority Queue 107 Re-Map Selection
23:16	QDMA_OUT_PRI_Q_106	QDMA Output Priority Queue 106 Re-Map Selection
15:8	QDMA_OUT_PRI_Q_105	QDMA Output Priority Queue 105 Re-Map Selection
7:0	QDMA_OUT_PRI_Q_104	QDMA Output Priority Queue 104 Re-Map Selection

15100E0C PFC_CFG_70 PFC QDMA Output Priority ReMap 27 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_OUT_PRI_Q_111								QDMA_OUT_PRI_Q_110							
Type	RW								RW							

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_OUT_PRI_Q_109								QDMA_OUT_PRI_Q_108							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	QDMA_OUT_PRI_Q_111	QDMA Output Priority Queue 111 Re-Map Selection
23:16	QDMA_OUT_PRI_Q_110	QDMA Output Priority Queue 110 Re-Map Selection
15:8	QDMA_OUT_PRI_Q_109	QDMA Output Priority Queue 109 Re-Map Selection
7:0	QDMA_OUT_PRI_Q_108	QDMA Output Priority Queue 108 Re-Map Selection

15100E10 PFC_CFG_71 PFC QDMA Output Priority ReMap 28 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_OUT_PRI_Q_115								QDMA_OUT_PRI_Q_114							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_OUT_PRI_Q_113								QDMA_OUT_PRI_Q_112							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	QDMA_OUT_PRI_Q_115	QDMA Output Priority Queue 115 Re-Map Selection
23:16	QDMA_OUT_PRI_Q_114	QDMA Output Priority Queue 114 Re-Map Selection
15:8	QDMA_OUT_PRI_Q_113	QDMA Output Priority Queue 113 Re-Map Selection
7:0	QDMA_OUT_PRI_Q_112	QDMA Output Priority Queue 112 Re-Map Selection

15100E14 PFC_CFG_72 PFC QDMA Output Priority ReMap 29 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_OUT_PRI_Q_119								QDMA_OUT_PRI_Q_118							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_OUT_PRI_Q_117								QDMA_OUT_PRI_Q_116							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	QDMA_OUT_PRI_Q_119	QDMA Output Priority Queue 119 Re-Map Selection
23:16	QDMA_OUT_PRI_Q_118	QDMA Output Priority Queue 118 Re-Map Selection
15:8	QDMA_OUT_PRI_Q_117	QDMA Output Priority Queue 117 Re-Map Selection
7:0	QDMA_OUT_PRI_Q_116	QDMA Output Priority Queue 116 Re-Map Selection

15100E18 PFC_CFG_73 PFC QDMA Output Priority ReMap 30 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_OUT_PRI_Q_123								QDMA_OUT_PRI_Q_122							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_OUT_PRI_Q_121								QDMA_OUT_PRI_Q_120							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	QDMA_OUT_PRI_Q_123	QDMA Output Priority Queue 123 Re-Map Selection
23:16	QDMA_OUT_PRI_Q_122	QDMA Output Priority Queue 122 Re-Map Selection
15:8	QDMA_OUT_PRI_Q_121	QDMA Output Priority Queue 121 Re-Map Selection
7:0	QDMA_OUT_PRI_Q_120	QDMA Output Priority Queue 120 Re-Map Selection

15100E1C PFC_CFG_74 PFC QDMA Output Priority ReMap 31 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_OUT_PRI_Q_127								QDMA_OUT_PRI_Q_126							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	QDMA_OUT_PRI_Q_125								QDMA_OUT_PRI_Q_124							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	QDMA_OUT_PRI_Q_127	QDMA Output Priority Queue 127 Re-Map Selection
23:16	QDMA_OUT_PRI_Q_126	QDMA Output Priority Queue 126 Re-Map Selection
15:8	QDMA_OUT_PRI_Q_125	QDMA Output Priority Queue 125 Re-Map Selection
7:0	QDMA_OUT_PRI_Q_124	QDMA Output Priority Queue 124 Re-Map Selection

15100EA0 PFC_CFG_75 PFC Enable Control to GMAC1 FFFFFFF0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EN_WDMA1_GMAC1								EN_WDMA0_GMAC1							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EN_GMAC2_GMAC1								EN_GMAC1_GMAC1							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	EN_WDMA1_GMAC1	Enable Control from WDMA1 to GMAC1
23:16	EN_WDMA0_GMAC1	Enable Control from WDMA0 to GMAC1
15:8	EN_GMAC2_GMAC1	Enable Control from GMAC2 to GMAC1
7:0	EN_GMAC1_GMAC1	Enable Control from GMAC1 to GMAC1

15100EA4 PFC_CFG_76 PFC Enable Control to GMAC1 000000FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									EN_QDMA_GMAC1							

Type									RW							
Reset									1	1	1	1	1	1	1	1

Bit(s)	Name	Description
7:0	EN_QDMA_GMAC1	Enable Control from QDMA to GMAC1

15100EA8 PFC_CFG_77 PFC Enable Control to GMAC2 FFFF00FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EN_WDMA1_GMAC2								EN_WDMA0_GMAC2							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EN_GMAC2_GMAC2								EN_GMAC1_GMAC2							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:24	EN_WDMA1_GMAC2	Enable Control from WDMA1 to GMAC2
23:16	EN_WDMA0_GMAC2	Enable Control from WDMA0 to GMAC2
15:8	EN_GMAC2_GMAC2	Enable Control from GMAC2 to GMAC2
7:0	EN_GMAC1_GMAC2	Enable Control from GMAC1 to GMAC2

15100EAC PFC_CFG_78 PFC Enable Control to GMAC2 000000FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									EN_QDMA_GMAC2							
Type									RW							
Reset									1	1	1	1	1	1	1	1

Bit(s)	Name	Description
7:0	EN_QDMA_GMAC2	Enable Control from QDMA to GMAC2

15100EB0 PFC_CFG_79 PFC Enable Control to WDMA0 FF00FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EN_WDMA1_WDMA0								EN_WDMA0_WDMA0							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EN_GMAC2_WDMA0								EN_GMAC1_WDMA0							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:24	EN_WDMA1_WDMA0	Enable Control from WDMA1 to WDMA0
23:16	EN_WDMA0_WDMA0	Enable Control from WDMA0 to WDMA0
15:8	EN_GMAC2_WDMA0	Enable Control from GMAC2 to WDMA0
7:0	EN_GMAC1_WDMA0	Enable Control from GMAC1 to WDMA0

15100EB4 PFC_CFG_80 PFC Enable Control to WDMA0 000000FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									EN_QDMA_WDMA0							
Type									RW							
Reset									1	1	1	1	1	1	1	1

Bit(s)	Name	Description
7:0	EN_QDMA_WDMA0	Enable Control from QDMA to WDMA0

15100EB8 PFC_CFG_81 PFC Enable Control to WDMA1 00FFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EN_WDMA1_WDMA1								EN_WDMA0_WDMA1							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EN_GMAC2_WDMA1								EN_GMAC1_WDMA1							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:24	EN_WDMA1_WDMA1	Enable Control from WDMA1 to WDMA1
23:16	EN_WDMA0_WDMA1	Enable Control from WDMA0 to WDMA1
15:8	EN_GMAC2_WDMA1	Enable Control from GMAC2 to WDMA1
7:0	EN_GMAC1_WDMA1	Enable Control from GMAC1 to WDMA1

15100EBC PFC_CFG_82 PFC Enable Control to WDMA1 000000FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									EN_QDMA_WDMA1							
Type									RW							
Reset									1	1	1	1	1	1	1	1

Bit(s)	Name	Description
7:0	EN_QDMA_WDMA1	Enable Control from QDMA to WDMA1

15100EC0 PFC_CFG_83 PFC Enable Control to QDMA FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EN_WDMA1_QDMA								EN_WDMA0_QDMA							

Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EN_GMAC2_QDMA								EN_GMAC1_QDMA							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:24	EN_WDMA1_QDMA	Enable Control from WDMA1 to QDMA
23:16	EN_WDMA0_QDMA	Enable Control from WDMA0 to QDMA
15:8	EN_GMAC2_QDMA	Enable Control from GMAC2 to QDMA
7:0	EN_GMAC1_QDMA	Enable Control from GMAC1 to QDMA

15100EF0 PFC_CFG 85 PFC Debug 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEBUG_WDMA1								DEBUG_WDMA0							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEBUG_GMAC2								DEBUG_GMAC1							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	DEBUG_WDMA1	Debug for Output Module : WDMA1
23:16	DEBUG_WDMA0	Debug for Output Module : WDMA0
15:8	DEBUG_GMAC2	Debug for Output Module : GMAC2 This debug is for PFC vector source from MAC/QDMA/WDMA in central, MAC TX will ignore this event in half duplex mode
7:0	DEBUG_GMAC1	Debug for Output Module : GMAC1 This debug is for PFC vector source from MAC/QDMA/WDMA in central, MAC TX will ignore this event in half duplex mode

15100EF4 PFC_CFG 86 PFC Debug 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	DEBUG_QDMA_31_0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEBUG_QDMA_31_0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DEBUG_QDMA_31_0	Debug for Output Module : QDMA bit 31~0

15100EF8 PFC_CFG_87 PFC Debug 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEBUG_QDMA_63_32															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEBUG_QDMA_63_32															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DEBUG_QDMA_63_32	Debug for Output Module : QDMA bit 63~32

15100EFC PFC_CFG_88 PFC Debug 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEBUG_QDMA_95_64															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	DEBUG_QDMA_95_64															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DEBUG_QDMA_95_64	Debug for Output Module : QDMA bit 95~64

15100F00 PFC_CFG_89 PFC Debug 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEBUG_QDMA_127_96															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEBUG_QDMA_127_96															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DEBUG_QDMA_127_96	Debug for Output Module : QDMA bit 127~96

15100F04 PFC_CFG_90 PFC Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_IN_PRI_PAGE_SEL	QDMA_IN_PRI_PAGE_SEL	QDMA_IN_PRI_PAGE_SEL	QDMA_IN_PRI_PAGE_SEL	QDMA_OUT_PRI_PAGE_SEL	QDMA_OUT_PRI_PAGE_SEL	QDMA_OUT_PRI_PAGE_SEL	QDMA_OUT_PRI_PAGE_SEL	QDMA_OUT_PRI_PAGE_SEL	QDMA_OUT_PRI_PAGE_SEL	QDMA_OUT_PRI_PAGE_SEL	QDMA_OUT_PRI_PAGE_SEL	QDMA_OUT_PRI_PAGE_SEL	QDMA_OUT_PRI_PAGE_SEL	QDMA_OUT_PRI_PAGE_SEL	QDMA_OUT_PRI_PAGE_SEL
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	QDMA_IN_PRI_PAGE_WR	QDMA Input Priority Page Write Enable
14:12	QDMA_IN_PRI_PAGE_SEL	QDMA Input Priority Page Selection It will latch input priority remap setting(PFC_CFG_5~PFC_CFG_36) to selected page when QDMA_IN_PRI_PAGE_WR = 1. It will be read back into PFC_CFG_5~PFC_CFG_36 according to select source when QDMA_IN_PRI_PAGE_WR = 0.
11	QDMA_OUT_PRI_PAGE_WR	QDMA Output Priority Page Write Enable
10:8	QDMA_OUT_PRI_PAGE_SEL	QDMA Output Priority Page Selection It will latch output priority remap setting(PFC_CFG_43~PFC_CFG_74) to selected page when QDMA_OUT_PRI_PAGE_WR = 1. It will be read back into PFC_CFG_43~PFC_CFG_74 according to select source when QDMA_OUT_PRI_PAGE_WR = 0.
2:0	STATUS_UPDATE_PERIOD_SEL	Status Update Period Selection

15101400	CDMQ_IG_CTRL				CDM_VLAN_Control								81000000			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CDM_TPID															
Type	RW															
Reset	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															UNTAG_EN	STAG_EN
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
31:16	CDM_TPID	Inserted VLAN TPID
1	UNTAG_EN	VLAN un-tag Un-tag the egress packets which are transmitted from CDM
0	STAG_EN	Special tag indication Indicate that the received packets is carrying the special tag from CPU

15101404	CDMQ_EG_CTRL				CDM Egress Control												00000000	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16		
Name																		
Type																		

Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																UNTAG_EN
Type																RW
Reset																0

Bit(s)	Name	Description
0	UNTAG_EN	VLAN un-tag Un-tag the egress packets which are transmitted from CDM to CPU

15101408 CDMQ_PPP_GEN CDM PPPoE Generation 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																PPP_INS
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SESS_ID															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	PPP_INS	PPPoE Header Insertion
15:0	SESS_ID	PPPoE Session ID

15101500 GDM2_IG_CTRL GDM Ingress Control 20717777

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0						INSV_EN	STAG_EN		GDM_ICSEN	GDM_TCSEN	GDM_UCSEN	DROP_256B			STRP_CRC
Type	RW						RW	RW		RW	RW	RW	RW			RW
Reset	0	0	1	0			0	0		1	1	1	0			1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MYMAC_DP				BC_DP				MC_DP				UN_DP			
Type	RW				RW				RW				RW			
Reset	0	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1

Bit(s)	Name	Description
31:28	REVO	Reserved
25	INSV_EN	VLAN insertion Insert Port VID on the received packets on the corresponding GDM port.
24	STAG_EN	Special tag indication Indicate that the received packets is carrying the special tag from GDM port.
22	GDM_ICS_EN	IPv4 header checksum error drop
21	GDM_TCS_EN	TCP checksum error drop
20	GDM_UCS_EN	UDP checksum error drop
19	DROP_256B	A special mode to drop packets with payload > 256-bytes
16	STRP_CRC	GDM RX CRC Stripping
15:12	MYMAC_DP	MY_MAC frames destination port
11:8	BC_DP	Broadcast frame destination port
7:4	MC_DP	Multicast frame destination port
3:0	UN_DP	Other frame destination port

15101504 GDM2 EG_CTRL GDM Egress Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		UNTAG_EN	DIS_PAD	DIS_CRC				SHPR_EN	BK_SIZE							
Type		RW	RW	RW				RW	RW							
Reset		0	0	0				0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TK_TIC		TK_RATE													
Type	RW		RW													
Reset	0		0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
30	UNTAG_EN	VLAN un-tag Un-tag the egress packets which are transmitted from GDM.
29	DIS_PAD	GMAC TX padding function
28	DIS_CRC	GMAC TX CRC generation
24	SHPR_EN	GDM output shaper enable

Bit(s)	Name	Description
23:16	BK_SIZE	GDM output shaper bucket size. This unit is 1K-byte
15	TK_TICK	GDM shaper token period
13:0	TK_RATE	GDM output shaper token rate The unit is 8-Byte/ms or 8-Byte/20us according to TK_TICK.

15101508 GDM2_MAC_LSB GDM MY_MAC Address LSB 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAC_ADR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAC_ADR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MAC_ADR	MY_MAC Address [31:0]

1510150C GDM2_MAC_MSB GDM MY_MAC Address MSB 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAC_ADR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	MAC_ADR	MY_MAC Address [47:32]

15101510	<u>GDM2_VLAN_GEN</u>				GDM VLAN Generation								81000000			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GDM_TPID															
Type	RW															
Reset	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GDM_PRI			GDM_CFI	GDM_VID											
Type	RW			RW	RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	GDM_TPID	Inserted VLAN TPID
15:13	GDM_PRI	Inserted PRI
12	GDM_CFI	Inserted CFI
11:0	GDM_VID	Inserted VLAN ID

15101514	<u>GDM2_FILTER_CTRL</u>				GDM Filter Control								00000000			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													GDM_VIDF_EN	GMD_HASH_ALG	GDM_DAF_MODE	
Type													RW	RW	RW	
Reset													0	0	0	0

Bit(s)	Name	Description
3	GDM_VIDF_EN	GDM VLAN ID filter enable
2	GMD_HASH_ALG	Hash Algorithm setting
1:0	GDM_DAF_MODE	Receive packet with DA Filter function

15101518 GDM2_VIDF01 GDM VID Filter Control 01 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GDM2_VID1_VLD				GDM2_VID1											
Type	RW				RW											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GDM2_VID0_VLD				GDM2_VID0											
Type	RW				RW											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	GDM2_VID1_VLD	VLAN ID #1 valid bit
27:16	GDM2_VID1	VLAN ID #1
15	GDM2_VID0_VLD	VLAN ID #0 valid bit
11:0	GDM2_VID0	VLAN ID #0

1510151C GDM2_VIDF23 GDM VID Filter Control 23 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GDM2_VID3_VLD				GDM2_VID3											
Type	RW				RW											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GDM2_VID2_VLD				GDM2_VID2											
Type	RW				RW											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	GDM2_VID3_VLD	VLAN ID #3 valid bit
27:16	GDM2_VID3	VLAN ID #3
15	GDM2_VID2_VLD	VLAN ID #2 valid bit
11:0	GDM2_VID2	VLAN ID #2

15101520 GDM2_DOS_CFG_0 GDM DOS Configuration 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SPD_2P5G_MODE	ICMP_AND_TOS_EQ_ZERO	MY_MAC_CHECK						TCP_DROP_INTERRUPT_STATUS	TCP_RATE_LIMITER_RST	TCP_DROP_INTERRUPT_EN	TCP_SYN_PKT_DROP_EN	TCP_SYN_LIMIT_MODE	TCP_SYN_LIMIT_UNIT		
Type	RW	RW	RW						W1C	RW	RW	RW	RW	RW		
Reset	0	0	0						0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	UDP_DROP_INTERRUPT_STATUS	UDP_RATE_LIMITER_RST	UDP_DROP_INTERRUPT_EN	UDP_PKT_DROP_EN	UDP_LIMIT_MODE	UDP_LIMIT_UNIT			ICMP_DROP_INTERRUPT_STATUS	ICMP_RATE_LIMITER_RST	ICMP_DROP_INTERRUPT_EN	ICMP_PKT_DROP_EN	ICMP_LIMIT_MODE	ICMP_LIMIT_UNIT		
Type	W1C	RW	RW	RW	RW	RW			W1C	RW	RW	RW	RW	RW		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	SPD_2P5G_MODE	Reference *_LIMIT_2P5G Setting for Rate Limitation
30	ICMP_AND_TOS_EQ_ZERO	IPv4 ICMP Packet Recognition Control
29	MY_MAC_CHECK	MY MAC Address Check Control
23	TCP_DROP_INTERRUPT_STATUS	TCP Packet Drop Interrupt Event Status
22	TCP_RATE_LIMITER_RST	TCP Rate Limiter Reset Control
21	TCP_DROP_INTERRUPT_EN	TCP Packet Drop Interrupt Event Control
20	TCP_SYN_PKT_DROP_EN	TCP SYN Packet Drop Control when Reaching Rate Limitation
19	TCP_SYN_LIMIT_MODE	TCP SYN Rate Limitation Mode
18:16	TCP_SYN_LIMIT_UNIT	Unit of TCP SYN Rate Limitation
15	UDP_DROP_INTERRUPT_STATUS	UDP Packet Drop Interrupt Event Status
14	UDP_RATE_LIMITER_RST	UDP Rate Limiter Reset Control
13	UDP_DROP_INTERRUPT_EN	UDP Packet Drop Interrupt Event Control
12	UDP_PKT_DROP_EN	UDP Packet Drop Control when Reaching Rate Limitation
11	UDP_LIMIT_MODE	UDP Rate Limitation Mode
10:8	UDP_LIMIT_UNIT	Unit of UDP Rate Limitation
7	ICMP_DROP_INTERRUPT_STATUS	ICMP Packet Drop Interrupt Event Status
6	ICMP_RATE_LIMITER_RST	ICMP Rate Limiter Reset Control
5	ICMP_DROP_INTERRUPT_EN	ICMP Packet Drop Interrupt Event Control
4	ICMP_PKT_DROP_EN	ICMP Packet Drop Control when Reaching Rate Limitation
3	ICMP_LIMIT_MODE	ICMP Rate Limitation Mode
2:0	ICMP_LIMIT_UNIT	Unit of ICMP Rate Limitation

Bit(s)	Name	Description

15101524 GDM2_DOS_CFG_1 GDM DOS Configuration 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TCP_SYN_LIMIT_2P5G								TCP_SYN_LIMIT_1G							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TCP_SYN_LIMIT_100M								TCP_SYN_LIMIT_10M							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	TCP_SYN_LIMIT_2P5G	2500 Mbps TCP_SYN Rate Limit Control The TCP_SYN rate limit for 2500 Mbps link speed
23:16	TCP_SYN_LIMIT_1G	1000 Mbps TCP_SYN Rate Limit Control The TCP_SYN rate limit for 1000 Mbps link speed
15:8	TCP_SYN_LIMIT_100M	100 Mbps TCP_SYN Rate Limit Control The TCP_SYN rate limit for 100 Mbps link speed
7:0	TCP_SYN_LIMIT_10M	10 Mbps TCP_SYN Rate Limit Control The TCP_SYN rate limit for 10 Mbps link speed

15101528 GDM2_DOS_CFG_2 GDM DOS Configuration 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	UDP_LIMIT_2P5G								UDP_LIMIT_1G							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	UDP_LIMIT_100M								UDP_LIMIT_10M							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	UDP_LIMIT_2P5G	2500 Mbps UDP Rate Limit Control

Bit(s)	Name	Description
23:16	UDP_LIMIT_1G	The UDP rate limit for 2500 Mbps link speed 1000 Mbps UDP Rate Limit Control
15:8	UDP_LIMIT_100M	The UDP rate limit for 1000 Mbps link speed 100 Mbps UDP Rate Limit Control
7:0	UDP_LIMIT_10M	The UDP rate limit for 100 Mbps link speed 10 Mbps UDP Rate Limit Control
		The UDP rate limit for 10 Mbps link speed

1510152C		GDM2 DOS CFG 3					GDM DOS Configuration 3					00000000				
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ICMP_LIMIT_2P5G								ICMP_LIMIT_1G							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ICMP_LIMIT_100M								ICMP_LIMIT_10M							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	ICMP_LIMIT_2P5G	2500 Mbps ICMP Rate Limit Control The ICMP rate limit for 2500 Mbps link speed
23:16	ICMP_LIMIT_1G	1000 Mbps ICMP Rate Limit Control The ICMP rate limit for 1000 Mbps link speed
15:8	ICMP_LIMIT_100M	100 Mbps ICMP Rate Limit Control The ICMP rate limit for 100 Mbps link speed
7:0	ICMP_LIMIT_10M	10 Mbps ICMP Rate Limit Control The ICMP rate limit for 10 Mbps link speed

15101530		GDM2 THRES			GDM2 Threshold										00000008		
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
Name																	
Type																	
Reset																	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Name													high_threshold				

Type													RW			
Reset													1	0	0	0

Bit(s)	Name	Description
3:0	high_threshold	memory high threshold value

[illegible]

Bit(s)	Name	Description
31:16	CDM_TPID	Inserted VLAN TPID
0	STAG_EN	Special tag indication Indicate that the received packets is carrying the special tag from CPU

[illegible]

Bit(s)	Name	Description
0	UNTAG_EN	VLAN un-tag Un-tag the egress packets which are transmitted from CDM to CPU

15101608 CDMW0 PPP_GEN CDM PPPoE Generation 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																PPP_IN S
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SESS_ID															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	PPP_INS	PPPoE Header Insertion
15:0	SESS_ID	PPPoE Session ID

15101610 CDMW1 IG_CTRL CDM VLAN Control 81000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CDM_TPID															
Type	RW															
Reset	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																STAG_ EN
Type																RW
Reset																0

Bit(s)	Name	Description
31:16	CDM_TPID	Inserted VLAN TPID
0	STAG_EN	Special tag indication

Bit(s)	Name	Description
		Indicate that the received packets is carrying the special tag from CPU

15101614 CDMW1 EG_CTRL CDM Egress Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																UNTAG_EN
Type																RW
Reset																0

Bit(s)	Name	Description
0	UNTAG_EN	VLAN un-tag Un-tag the egress packets which are transmitted from CDM to CPU

15101618 CDMW1 PPP_GEN CDM PPPoE Generation 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																PPP_IN S
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SESS_ID															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	PPP_INS	PPPoE Header Insertion
15:0	SESS_ID	PPPoE Session ID

15101620 CDME0_IG_CTRL CDM VLAN Control 81000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CDM_TPID															
Type	RW															
Reset	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																STAG_EN
Type																RW
Reset																0

Bit(s)	Name	Description
31:16	CDM_TPID	Inserted VLAN TPID
0	STAG_EN	Special tag indication Indicate that the received packets is carrying the special tag from CPU

15101624 CDME0_EG_CTRL CDM Egress Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																UNTAG_EN
Type																RW
Reset																0

Bit(s)	Name	Description
0	UNTAG_EN	VLAN un-tag Un-tag the egress packets which are transmitted from CDM to CPU

15101628 CDME0_PPP_GEN CDM PPPoE Generation 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																PPP_INS
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SESS_ID															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	PPP_INS	PPPoE Header Insertion
15:0	SESS_ID	PPPoE Session ID

15101630 CDME1 IG_CTRL CDM VLAN Control 81000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CDM_TPID															
Type	RW															
Reset	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																STAG_EN
Type																RW
Reset																0

Bit(s)	Name	Description
31:16	CDM_TPID	Inserted VLAN TPID
0	STAG_EN	Special tag indication Indicate that the received packets is carrying the special tag from CPU

15101634 CDME1 EG_CTRL CDM Egress Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																UNTAG_EN
Type																RW
Reset																0

Bit(s)	Name	Description
0	UNTAG_EN	VLAN un-tag Un-tag the egress packets which are transmitted from CDM to CPU

15101638 CDME1 PPP_GEN CDM PPPoE Generation 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																PPP_INS
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SESS_ID															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	PPP_INS	PPPoE Header Insertion
15:0	SESS_ID	PPPoE Session ID

15101640 CDMM IG_CTRL CDM VLAN Control 81000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CDM_TPID															
Type	RW															

Reset	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																STAG_EN
Type																RW
Reset																0

Bit(s)	Name	Description
31:16	CDM_TPID	Inserted VLAN TPID
0	STAG_EN	Special tag indication Indicate that the received packets is carrying the special tag from CPU

15101644 CDMM EG_CTRL CDM Egress Control 00000002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														TACK2RING_ID	TACK2RING_EN	UNTAG_EN
Type														RW	RW	RW
Reset														0	1	0

Bit(s)	Name	Description
2	TACK2RING_ID	Ring selection of TCP ACK to dedicate Rx Ring
1	TACK2RING_EN	Enable TCP ACK to dedicate Rx Ring
0	UNTAG_EN	VLAN un-tag Un-tag the egress packets which are transmitted from CDM to CPU

15101648 CDMM PPP_GEN CDM PPPoE Generation 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																PPP_INS

Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SESS_ID															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	PPP_INS	PPPoE Header Insertion
15:0	SESS_ID	PPPoE Session ID

1510164C CDM_THRES0 CDM Threshold 0 08000008

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					cdma_high_threshold											
Type					RW											
Reset					1	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													cdmw0_high_threshold			
Type													RW			
Reset													1	0	0	0

Bit(s)	Name	Description
27:24	cdma_high_threshold	memory high threshold value
3:0	cdmw0_high_threshold	memory high threshold value

15101650 CDM_THRES1 CDM Threshold 1 00000008

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

[illegible]

Bit(s)	Name	Description
3:0	cdmw1_high_threshold	memory high threshold value

15101654	CDM THRES2	CDM Threshold 2	00000008

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													cdme0_high_threshold			
Type													RW			
Reset													1	0	0	0

Bit(s)	Name	Description
3:0	cdme0 high threshold	memory high threshold value

15101658	<u>CDM_THRES3</u>	CDM Threshold 3	00000008

[illegible]

Bit(s)	Name	Description
3:0	cdme1_high_threshold	memory high threshold value

1510165C CDM_THRES4 CDM Threshold 4 00000008

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													cdmm_high_threshold			
Type													RW			
Reset													1	0	0	0

Bit(s)	Name	Description
3:0	cdmm_high_threshold	memory high threshold value

15101660 CDM1_TS_DBG_CNT CDM1 TS Debug Counter 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

15101664 CDM1_FS_DBG_CNT CDM1 FS Debug Counter 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

15101668 CDM2 TS DBG CNT CDM2 TS Debug Counter 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

1510166C CDM2 FS DBG CNT CDM2 FS Debug Counter 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name																
Type																
Reset																

Bit(s)	Name	Description

15101670 CDM3 TS_DBG_CNT CDM3 TS Debug Counter 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

15101674 CDM3 FS_DBG_CNT CDM3 FS Debug Counter 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

15101678 CDM4 TS_DBG_CNT CDM4 TS Debug Counter 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

1510167C CDM4_FS_DBG_CNT CDM4 FS Debug Counter 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

15102800 RSS_GLO_CFG RSS Global Configuration 1F1F3370

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				IPV4_TUPLE_EN								IPV6_TUPLE_EN				

Type				RW								RW				
Reset				1	1	1	1	1				1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		IPV4_TYPE				IPV6_TYPE				INDR_TBL_SIZE			RSS_CFG_RDY	RSS_CFG_REQ	RSS_BUSY	RSS_ENABLE
Type		RW				RW				RW			RO	RW	RO	RW
Reset		0	1	1		0	1	1		1	1	1	0	0	0	0

Bit(s)	Name	Description
28:24	IPV4_TUPLE_EN	IPv4 Hash Tuple Global Enable This field controls which hash tuple is valid for IPv4 hash calculation. The invalid(disabled) tuple can be seen as 0x0 when calculating HASH. For example, when SIP is disabled, 2-tuple and 4-tuple hash will not consider SIP. Another example, when DPORT is disabled, 4-tuple hash will not consider DPORT. Bit Maps: {DPROT,SPORT,DIP,SIP,Reserved} Set the bits to 1 to enable corresponding hash tuple for hash calculation. Set the bits to 0 to disable corresponding hash tuple for hash calculation.
20:16	IPV6_TUPLE_EN	IPv6 Hash Tuple Global Enable This field controls which hash tuple is valid for IPv6 hash calculation. See description of IPV4_TUPLE_EN for more detail. Bit Maps: {DPROT,SPORT,DIP,SIP,Reserved} Set the bits to 1 to enable corresponding hash tuple for hash calculation. Set the bits to 0 to disable corresponding hash tuple for hash calculation.
14:12	IPV4_TYPE	IPv4 Hash Type Selection Flag This field controls the selection of hash 2-tuple and 4-tuple for different kinds of IPv4 packet. Bit Maps: {UDP 4-tuple,TCP4-tuple,IP 2-tuple} RSS performs the hash calculations as specified for the enabled case. For example, IPV4_TYPE=3'b011, RSS will use 4-tuple hash for IPv4 TCP packets and 2-tuple hash for IPv4 non-TCP packets (such as IPv4 fragment packet).
10:8	IPV6_TYPE	IPv6 Hash Type Selection Flag This field controls the selection of hash 2-tuple and 4-tuple for different kinds of IPv6 packet. Bit Maps: {UDP 4-tuple,TCP4-tuple,IP 2-tuple} See description of IPV4_TYPE for more detail.
6:4	INDR_TBL_SIZE	Change the size of indirection table. This register field affects how many bits of hash result will be used as the entry of indirection table. For example, INDR_TBL_SIZE=6 means RSS use only 6 bits of hash result as indirection table entry, which also means that indirection table has $2^6=64$ entries.
3	RSS_CFG_RDY	RSS is ready to accept new register configuration.

Bit(s)	Name	Description
2	RSS_CFG_REQ	This register will be asserted after RSS accepted the request from RSS_CFG_REQ. See description of RSS_CFG_REQ for more detail. Request to change RSS register configuration. When Request asserted, RSS will be paused after the process of current packet has finished. It is worth to notice that assert RSS_CFG_REQ is required before enable RSS or changing other register setting(such as indirection table). Must wait RSS_CFG_RDY=1 before changing RSS register value(including RSS_ENABLE).
1	RSS_BUSY	RSS is working or not
0	RSS_ENABLE	Enable/Disable RSS

15102804 RSS_GLO_CFG2 RSS Global Configuration2 C000001A

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

15102808 RSS_REV RSS REV 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

15102818 RSS_DBG_PROBE RSS DEBUG PROBE 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

1510281C RSS_FSM RSS FSM 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

15102820 RSS_HASH_KEY_DW0 RSS hash Key DW0 BEAC01FA

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	HASH_KEY_DW0															
Type	RW															
Reset	1	0	1	1	1	1	1	0	1	0	1	0	1	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HASH_KEY_DW0															
Type	RW															
Reset	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0

Bit(s)	Name	Description
31:0	HASH_KEY_DW0	Hash Key bit 31~0

15102824 RSS_HASH_KEY_DW1 RSS hash Key DW1 6A42B73B

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	HASH_KEY_DW1															
Type	RW															
Reset	0	1	1	0	1	0	1	0	0	1	0	0	0	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HASH_KEY_DW1															
Type	RW															
Reset	1	0	1	1	0	1	1	1	0	0	1	1	1	0	1	1

Bit(s)	Name	Description
31:0	HASH_KEY_DW1	Hash Key bit 63~32

15102828 RSS_HASH_KEY_DW2 RSS hash Key DW2 8030F20C

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	HASH_KEY_DW2															
Type	RW															
Reset	1	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	HASH_KEY_DW2															
Type	RW															
Reset	1	1	1	1	0	0	1	0	0	0	0	0	1	1	0	0

Bit(s)	Name	Description
31:0	HASH_KEY_DW2	Hash Key bit 95~64

1510282C RSS_HASH_KEY_DW3 RSS hash Key DW3 77CB2DA3

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	HASH_KEY_DW3															
Type	RW															
Reset	0	1	1	1	0	1	1	1	1	1	0	0	1	0	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HASH_KEY_DW3															
Type	RW															
Reset	0	0	1	0	1	1	0	1	1	0	1	0	0	0	1	1

Bit(s)	Name	Description
31:0	HASH_KEY_DW3	Hash Key bit 127~96

15102830 RSS_HASH_KEY_DW4 RSS hash Key DW4 AE7B30B4

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	HASH_KEY_DW4															
Type	RW															
Reset	1	0	1	0	1	1	1	0	0	1	1	1	1	0	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HASH_KEY_DW4															
Type	RW															
Reset	0	0	1	1	0	0	0	0	1	0	1	1	0	1	0	0

Bit(s)	Name	Description
31:0	HASH_KEY_DW4	Hash Key bit 159~128

15102834 RSS_HASH_KEY_DW5 RSS hash Key DW5 D0CA2BCB

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	HASH_KEY_DW5															
Type	RW															
Reset	1	1	0	1	0	0	0	0	1	1	0	0	1	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HASH_KEY_DW5															
Type	RW															
Reset	0	0	1	0	1	0	1	1	1	1	0	0	1	0	1	1

Bit(s)	Name	Description
31:0	HASH_KEY_DW5	Hash Key bit 191~160

15102838 RSS_HASH_KEY_DW6 RSS hash Key DW6 43A38FB0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	HASH_KEY_DW6															
Type	RW															
Reset	0	1	0	0	0	0	1	1	1	0	1	0	0	0	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HASH_KEY_DW6															
Type	RW															
Reset	1	0	0	0	1	1	1	1	1	0	1	1	0	0	0	0

Bit(s)	Name	Description
31:0	HASH_KEY_DW6	Hash Key bit 223~192

1510283C RSS_HASH_KEY_DW7 RSS hash Key DW7 4167253D

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	HASH_KEY_DW7															
Type	RW															
Reset	0	1	0	0	0	0	0	1	0	1	1	0	0	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HASH_KEY_DW7															
Type	RW															
Reset	0	0	1	0	0	1	0	1	0	0	1	1	1	1	0	1

Bit(s)	Name	Description
31:0	HASH_KEY_DW7	Hash Key bit 255~224

15102840 RSS_HASH_KEY_DW8 RSS hash Key DW8 255B0EC2

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	HASH_KEY_DW8															
Type	RW															
Reset	0	0	1	0	0	1	0	1	0	1	0	1	1	0	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HASH_KEY_DW8															
Type	RW															
Reset	0	0	0	0	1	1	1	0	1	1	0	0	0	0	1	0

Bit(s)	Name	Description
31:0	HASH_KEY_DW8	Hash Key bit 287~256

15102844 RSS_HASH_KEY_DW9 RSS hash Key DW9 6D5A56DA

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	HASH_KEY_DW9															
Type	RW															
Reset	0	1	1	0	1	1	0	1	0	1	0	1	1	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	HASH_KEY_DW9															
Type	RW															
Reset	0	1	0	1	0	1	1	0	1	1	0	1	1	0	1	0

Bit(s)	Name	Description
31:0	HASH_KEY_DW9	Hash Key bit 319~288

15102848 RSS_LFB_CFG0 RSS Low Flow Balance Configuration 0 00C7FF02

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TICK_TIMER															
Type	RW															
Reset	0	0	0	0	0	0	0	0	1	1	0	0	0	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AGE_TIMER													CMP_T CP_UD P	CMP_I PV4_IP V6	EN
Type	RW													RW	RW	RW
Reset	1	1	1	1	1	1	1	1						0	1	0

Bit(s)	Name	Description
31:16	TICK_TIMER	Low Flow Balance Table Age Tick Timer An internal generated timeout timer based on 20us tick time. When timeout, it will trigger a tick to age timer to count forward. If set to zero: tick timer is disabled and the trigger of age timer is the copy of raw 20us tick instead.
15:8	AGE_TIMER	Low Flow Balance Table Age Timer Entry ageout timer of low flow balance table. The applied age out timer is equal to (AGE_TIMER+1)*(TICK_TIMER)*20us
2	CMP_TCP_UDP	Low Flow Balance Table TCP/UDP Flow Compare When enabled, TCP flow and UDP flow will be seen as different flow even if these flow has same DPORT and SPORT.
1	CMP_IPV4_IPV6	Low Flow Balance Table IPv4/IPv6 Flow Compare When enabled, IPv4 flow and IPv6 flow will be seen as different flow even if these flow has same DIP and SIP.
0	EN	Low Flow Balance Table Enable

15102850 RSS_INDR_TABLE_DW0 RSS Indirection table DW0 DEADBEEF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	INDR_TABLE_DW0															
Type	RW															
Reset	1	1	0	1	1	1	1	0	1	0	1	0	1	1	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	INDR_TABLE_DW0															
Type	RW															
Reset	1	0	1	1	1	1	1	0	1	1	1	0	1	1	1	1

Bit(s)	Name	Description
31:0	INDR_TABLE_DW0	Indirection Table Entry 15~0 Each entry has 2bits

15102854 RSS INDR TABLE DW1 RSS Indirection table DW1 DEADBEEF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	INDR_TABLE_DW1															
Type	RW															
Reset	1	1	0	1	1	1	1	0	1	0	1	0	1	1	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	INDR_TABLE_DW1															
Type	RW															
Reset	1	0	1	1	1	1	1	0	1	1	1	0	1	1	1	1

Bit(s)	Name	Description
31:0	INDR_TABLE_DW1	Indirection Table Entry 31~16 Each entry has 2bits

15102858 RSS INDR TABLE DW2 RSS Indirection table DW2 DEADBEEF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	INDR_TABLE_DW2															
Type	RW															
Reset	1	1	0	1	1	1	1	0	1	0	1	0	1	1	0	1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	INDR_TABLE_DW2															
Type	RW															
Reset	1	0	1	1	1	1	1	0	1	1	1	0	1	1	1	1

Bit(s)	Name	Description
31:0	INDR_TABLE_DW2	Indirection Table Entry 47~32 Each entry has 2bits

1510285C RSS_INDR_TABLE_DW3 RSS Indirection table DW3 DEADBEEF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	INDR_TABLE_DW3															
Type	RW															
Reset	1	1	0	1	1	1	1	0	1	0	1	0	1	1	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	INDR_TABLE_DW3															
Type	RW															
Reset	1	0	1	1	1	1	1	0	1	1	1	0	1	1	1	1

Bit(s)	Name	Description
31:0	INDR_TABLE_DW3	Indirection Table Entry 63~48 Each entry has 2bits

15102860 RSS_INDR_TABLE_DW4 RSS Indirection table DW4 DEADBEEF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	INDR_TABLE_DW4															
Type	RW															
Reset	1	1	0	1	1	1	1	0	1	0	1	0	1	1	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	INDR_TABLE_DW4															
Type	RW															

Reset	1	0	1	1	1	1	1	0	1	1	1	0	1	1	1	1

Bit(s)	Name	Description
31:0	INDR_TABLE_DW4	Indirection Table Entry 79~64 Each entry has 2bits

15102864 RSS_INDR_TABLE_DW5 RSS Indirection table DW5 DEADBEEF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	INDR_TABLE_DW5															
Type	RW															
Reset	1	1	0	1	1	1	1	0	1	0	1	0	1	1	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	INDR_TABLE_DW5															
Type	RW															
Reset	1	0	1	1	1	1	1	0	1	1	1	0	1	1	1	1

Bit(s)	Name	Description
31:0	INDR_TABLE_DW5	Indirection Table Entry 95~80 Each entry has 2bits

15102868 RSS_INDR_TABLE_DW6 RSS Indirection table DW6 DEADBEEF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	INDR_TABLE_DW6															
Type	RW															
Reset	1	1	0	1	1	1	1	0	1	0	1	0	1	1	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	INDR_TABLE_DW6															
Type	RW															
Reset	1	0	1	1	1	1	1	0	1	1	1	0	1	1	1	1

Bit(s)	Name	Description
31:0	INDR_TABLE_DW6	Indirection Table Entry 111~96 Each entry has 2bits

Bit(s)	Name	Description

1510286C RSS_INDR_TABLE_DW7 RSS Indirection table DW7 DEADBEEF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	INDR_TABLE_DW7															
Type	RW															
Reset	1	1	0	1	1	1	1	0	1	0	1	0	1	1	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	INDR_TABLE_DW7															
Type	RW															
Reset	1	0	1	1	1	1	1	0	1	1	1	0	1	1	1	1

Bit(s)	Name	Description
31:0	INDR_TABLE_DW7	Indirection Table Entry 127~112 Each entry has 2bits

15104400 QTX_CFG_0 TX Queue #0, #(16 * n) Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HW_RESV_CNT								SW_RESV_CNT							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	TX_DES_CNT	TX descriptor count in Queue #
15:8	HW_RESV_CNT	Buffer Reserved for HW path The reserved buffer number is specified on QDMA_RES_THRES.
7:0	SW_RESV_CNT	Buffer Reserved for SW path The reserved buffer number is specified on QDMA_RES_THRES.

15104404 QTX_SCH_0 TX Queue #0, #(16 * n) Schedule 00100010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_SCH_SEL		BUCKET_DEP		MIN_RATE_EN	MIN_RATE_MAN							MIN_RATE_EXP			
Type	RW		RW		RW	RW							RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_WGHT				MAX_RATE_EN	MAX_RATE_MAN							MAX_RATE_EXP			
Type	RW				RW	RW							RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
31:30	TX_SCH_SEL	TX queue on scheduler no.
29:28	BUCKET_DEP	Bucket Depth
27	MIN_RATE_EN	TX Queue min. rate control enable [Note] Rate control is calculated by 125MHz bus clock, please multiply by a factor when the bus clock is not 125MHz.
26:20	MIN_RATE_MAN	Mantissa part of the max. rate control of the TX queue # Value range: 0~127
19:16	MIN_RATE_EXP	Exponent part of the max. rate control of the TX queue # value selection
15:12	MAX_RATE_WGHT	The weighted value of the WFQ for TX queue # maximum rate.
11	MAX_RATE_EN	TX Queue max. rate control enable. [Note] Rate control is calculated by 125MHz bus clock, please multiply by a factor when the bus clock is not 125MHz.
10:4	MAX_RATE_MAN	Mantissa part of the max. rate control of the TX queue # Value range: 0~127
3:0	MAX_RATE_EXP	Exponent part of the max. rate control of the TX queue # value selection

15104408 QTX_HEAD_0 TX Queue #0, #(16 * n) Head Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_HEAD															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	TX_DES_HEAD															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DES_HEAD	TX descriptor head pointer in Queue #

1510440C QTX_TAIL_0 TX Queue #0, #(16 * n) Tail Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_TAIL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DES_TAIL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DES_TAIL	TX descriptor tail pointer in Queue #

15104410 QTX_CFG_1 TX Queue #1, #(16 * n + 1) Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HW_RESV_CNT								SW_RESV_CNT							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	TX_DES_CNT	TX descriptor count in Queue #
15:8	HW_RESV_CNT	Buffer Reserved for HW path The reserved buffer number is specified on QDMA_RES_THRES.
7:0	SW_RESV_CNT	Buffer Reserved for SW path The reserved buffer number is specified on QDMA_RES_THRES.

15104414 QTX_SCH_1 TX Queue #1, #(16 * n + 1) Schedule 00100010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QTX_SCH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QTX_SCH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
31:0	QTX_SCH	Please refer the description of QTX_SCH_0, the same definition.

15104418 QTX_HEAD_1 TX Queue #1, #(16 * n + 1) Head Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_HEAD															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DES_HEAD															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DES_HEAD	TX descriptor head pointer in Queue #

1510441C QTX_TAIL_1 TX Queue #1, #(16 * n + 1) Tail Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_TAIL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DES_TAIL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DES_TAIL	TX descriptor tail pointer in Queue #

15104420 QTX_CFG_2 TX Queue #2, #(16 * n + 2) Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HW_RESV_CNT								SW_RESV_CNT							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	TX_DES_CNT	TX descriptor count in Queue #
15:8	HW_RESV_CNT	Buffer Reserved for HW path The reserved buffer number is specified on QDMA_RES_THRES.
7:0	SW_RESV_CNT	Buffer Reserved for SW path The reserved buffer number is specified on QDMA_RES_THRES.

15104424 QTX_SCH_2 TX Queue #2, #(16 * n + 2) Schedule 00100010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	QTX_SCH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QTX_SCH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
31:0	QTX_SCH	Please refer the description of QTX_SCH_0, the same definition.

15104428 QTX_HEAD_2 TX Queue #2, #(16 * n + 2) Head Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_HEAD															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DES_HEAD															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DES_HEAD	TX descriptor head pointer in Queue #

1510442C QTX_TAIL_2 TX Queue #2, #(16 * n + 2) Tail Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_TAIL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	TX_DES_TAIL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DES_TAIL	TX descriptor tail pointer in Queue #

15104430 QTX_CFG_3 TX Queue #3, #(16 * n + 3) Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HW_RESV_CNT								SW_RESV_CNT							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	TX_DES_CNT	TX descriptor count in Queue #
15:8	HW_RESV_CNT	Buffer Reserved for HW path The reserved buffer number is specified on QDMA_RES_THRES.
7:0	SW_RESV_CNT	Buffer Reserved for SW path The reserved buffer number is specified on QDMA_RES_THRES.

15104434 QTX_SCH_3 TX Queue #3, #(16 * n + 3) Schedule 00100010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QTX_SCH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QTX_SCH															
Type	RW															

Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
31:0	QTX_SCH	Please refer the description of QTX_SCH_0, the same definition.

15104438 QTX_HEAD_3 TX Queue #3, #(16 * n + 3) Head Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_HEAD															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DES_HEAD															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DES_HEAD	TX descriptor head pointer in Queue #

1510443C QTX_TAIL_3 TX Queue #3, #(16 * n + 3) Tail Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_TAIL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DES_TAIL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DES_TAIL	TX descriptor tail pointer in Queue #

15104440 QTX_CFG_4 TX Queue #4, #(16 * n + 4) Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HW_RESV_CNT								SW_RESV_CNT							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	TX_DES_CNT	TX descriptor count in Queue #
15:8	HW_RESV_CNT	Buffer Reserved for HW path The reserved buffer number is specified on QDMA_RES_THRES.
7:0	SW_RESV_CNT	Buffer Reserved for SW path The reserved buffer number is specified on QDMA_RES_THRES.

15104444 QTX_SCH_4 TX Queue #4, #(16 * n + 4) Schedule 00100010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QTX_SCH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QTX_SCH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
31:0	QTX_SCH	Please refer the description of QTX_SCH_0, the same definition.

15104448 QTX_HEAD_4 TX Queue #4, #(16 * n + 4) Head Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	TX_DES_HEAD															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DES_HEAD															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DES_HEAD	TX descriptor head pointer in Queue #

1510444C QTX_TAIL_4 TX Queue #4, #(16 * n + 4) Tail Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_TAIL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DES_TAIL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DES_TAIL	TX descriptor tail pointer in Queue #

15104450 QTX_CFG_5 TX Queue #5, #(16 * n + 5) Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	HW_RESV_CNT								SW_RESV_CNT							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	TX_DES_CNT	TX descriptor count in Queue #
15:8	HW_RESV_CNT	Buffer Reserved for HW path The reserved buffer number is specified on QDMA_RES_THRES.
7:0	SW_RESV_CNT	Buffer Reserved for SW path The reserved buffer number is specified on QDMA_RES_THRES.

15104454 QTX_SCH_5 TX Queue #5, #(16 * n + 5) Schedule 00100010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QTX_SCH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QTX_SCH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
31:0	QTX_SCH	Please refer the description of QTX_SCH_0, the same definition.

15104458 QTX_HEAD_5 TX Queue #5, #(16 * n + 5) Head Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_HEAD															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DES_HEAD															
Type	RO															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DES_HEAD	TX descriptor head pointer in Queue #

1510445C QTX_TAIL_5 TX Queue #5, #(16 * n + 5) Tail Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_TAIL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DES_TAIL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DES_TAIL	TX descriptor tail pointer in Queue #

15104460 QTX_CFG_6 TX Queue #6, #(16 * n + 6) Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HW_RESV_CNT								SW_RESV_CNT							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	TX_DES_CNT	TX descriptor count in Queue #
15:8	HW_RESV_CNT	Buffer Reserved for HW path
		The reserved buffer number is specified on QDMA_RES_THRES.
7:0	SW_RESV_CNT	Buffer Reserved for SW path

Bit(s)	Name	Description
The reserved buffer number is specified on QDMA_RES_THRES.		

15104464 QTX_SCH_6 TX Queue #6, #(16 * n + 6) Schedule 00100010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QTX_SCH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QTX_SCH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
31:0	QTX_SCH	Please refer the description of QTX_SCH_0, the same definition.

15104468 QTX_HEAD_6 TX Queue #6, #(16 * n + 6) Head Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_HEAD															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DES_HEAD															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DES_HEAD	TX descriptor head pointer in Queue #

1510446C QTX_TAIL_6 TX Queue #6, #(16 * n + 6) Tail Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	TX_DES_TAIL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DES_TAIL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DES_TAIL	TX descriptor tail pointer in Queue #

15104470 QTX_CFG_7 TX Queue #7, #(16 * n + 7) Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HW_RESV_CNT								SW_RESV_CNT							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	TX_DES_CNT	TX descriptor count in Queue #
15:8	HW_RESV_CNT	Buffer Reserved for HW path The reserved buffer number is specified on QDMA_RES_THRES.
7:0	SW_RESV_CNT	Buffer Reserved for SW path The reserved buffer number is specified on QDMA_RES_THRES.

15104474 QTX_SCH_7 TX Queue #7, #(16 * n + 7) Schedule 00100010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QTX_SCH															
Type	RW															

Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QTX_SCH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
31:0	QTX_SCH	Please refer the description of QTX_SCH_0, the same definition.

15104478 QTX_HEAD_7 TX Queue #7, #(16 * n + 7) Head Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_HEAD															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DES_HEAD															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DES_HEAD	TX descriptor head pointer in Queue #

1510447C QTX_TAIL_7 TX Queue #7, #(16 * n + 7) Tail Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_TAIL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DES_TAIL															
Type	RO															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DES_TAIL	TX descriptor tail pointer in Queue #

15104480 QTX_CFG_8 TX Queue #8, #(16 * n + 8) Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HW_RESV_CNT								SW_RESV_CNT							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	TX_DES_CNT	TX descriptor count in Queue #
15:8	HW_RESV_CNT	Buffer Reserved for HW path The reserved buffer number is specified on QDMA_RES_THRES.
7:0	SW_RESV_CNT	Buffer Reserved for SW path The reserved buffer number is specified on QDMA_RES_THRES.

15104484 QTX_SCH_8 TX Queue #8, #(16 * n + 8) Schedule 00100010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QTX_SCH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QTX_SCH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
31:0	QTX_SCH	Please refer the description of QTX_SCH_0, the same definition.

15104488 QTX_HEAD_8 TX Queue #8, #(16 * n + 8) Head Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_HEAD															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DES_HEAD															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DES_HEAD	TX descriptor head pointer in Queue #

1510448C QTX_TAIL_8 TX Queue #8, #(16 * n + 8) Tail Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_TAIL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DES_TAIL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DES_TAIL	TX descriptor tail pointer in Queue #

15104490 QTX_CFG_9 TX Queue #9, #(16 * n + 9) Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	TX_DES_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HW_RESV_CNT								SW_RESV_CNT							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	TX_DES_CNT	TX descriptor count in Queue #
15:8	HW_RESV_CNT	Buffer Reserved for HW path The reserved buffer number is specified on QDMA_RES_THRES.
7:0	SW_RESV_CNT	Buffer Reserved for SW path The reserved buffer number is specified on QDMA_RES_THRES.

15104494 QTX_SCH_9 TX Queue #9, #(16 * n + 9) Schedule 00100010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QTX_SCH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QTX_SCH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
31:0	QTX_SCH	Please refer the description of QTX_SCH_0, the same definition.

15104498 QTX_HEAD_9 TX Queue #9, #(16 * n + 9) Head Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_HEAD															
Type	RO															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DES_HEAD															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DES_HEAD	TX descriptor head pointer in Queue #

1510449C QTX_TAIL_9 TX Queue #9, #(16 * n + 9) Tail Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_TAIL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DES_TAIL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DES_TAIL	TX descriptor tail pointer in Queue #

151044A0 QTX_CFG_10 TX Queue #10, #(16 * n + 10) Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HW_RESV_CNT								SW_RESV_CNT							
Type	RW								RW							

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	TX_DES_CNT	TX descriptor count in Queue #
15:8	HW_RESV_CNT	Buffer Reserved for HW path The reserved buffer number is specified on QDMA_RES_THRES.
7:0	SW_RESV_CNT	Buffer Reserved for SW path The reserved buffer number is specified on QDMA_RES_THRES.

151044A4 QTX_SCH_10 TX Queue #10, #(16 * n + 10) Schedule 00100010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QTX_SCH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QTX_SCH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
31:0	QTX_SCH	Please refer the description of QTX_SCH_0, the same definition.

151044A8 QTX_HEAD_10 TX Queue #10, #(16 * n + 10) Head Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_HEAD															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DES_HEAD															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DES_HEAD	TX descriptor head pointer in Queue #

151044AC QTX_TAIL_10 TX Queue #10, #(16 * n + 10) Tail Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_TAIL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DES_TAIL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DES_TAIL	TX descriptor tail pointer in Queue #

151044B0 QTX_CFG_11 TX Queue #11, #(16 * n + 11) Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HW_RESV_CNT								SW_RESV_CNT							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	TX_DES_CNT	TX descriptor count in Queue #
15:8	HW_RESV_CNT	Buffer Reserved for HW path The reserved buffer number is specified on QDMA_RES_THRES.
7:0	SW_RESV_CNT	Buffer Reserved for SW path The reserved buffer number is specified on QDMA_RES_THRES.

151044B4 QTX_SCH_11 TX Queue #11, #(16 * n + 11) Schedule 00100010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QTX_SCH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QTX_SCH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
31:0	QTX_SCH	Please refer the description of QTX_SCH_0, the same definition.

151044B8 QTX_HEAD_11 TX Queue #11, #(16 * n + 11) Head Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_HEAD															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DES_HEAD															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DES_HEAD	TX descriptor head pointer in Queue #

151044BC QTX_TAIL_11 TX Queue #11, #(16 * n + 11) Tail Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_TAIL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DES_TAIL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DES_TAIL	TX descriptor tail pointer in Queue #

151044C0 QTX_CFG_12 TX Queue #12, #(16 * n + 12) Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HW_RESV_CNT								SW_RESV_CNT							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	TX_DES_CNT	TX descriptor count in Queue #
15:8	HW_RESV_CNT	Buffer Reserved for HW path The reserved buffer number is specified on QDMA_RES_THRES.
7:0	SW_RESV_CNT	Buffer Reserved for SW path The reserved buffer number is specified on QDMA_RES_THRES.

151044C4 QTX_SCH_12 TX Queue #12, #(16 * n + 12) Schedule 00100010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QTX_SCH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QTX_SCH															

Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0

Bit(s)	Name	Description
31:0	QTX_SCH	Please refer the description of QTX_SCH_0, the same definition.

151044C8 QTX HEAD 12 TX Queue #12, #(16 * n + 12) Head Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_HEAD															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DES_HEAD															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DES_HEAD	TX descriptor head pointer in Queue #

151044CC QTX TAIL 12 TX Queue #12, #(16 * n + 12) Tail Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_TAIL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DES_TAIL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DES_TAIL	TX descriptor tail pointer in Queue #

151044D0 QTX_CFG_13 TX Queue #13, #(16 * n + 13) Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HW_RESV_CNT								SW_RESV_CNT							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	TX_DES_CNT	TX descriptor count in Queue #
15:8	HW_RESV_CNT	Buffer Reserved for HW path The reserved buffer number is specified on QDMA_RES_THRES.
7:0	SW_RESV_CNT	Buffer Reserved for SW path The reserved buffer number is specified on QDMA_RES_THRES.

151044D4 QTX_SCH_13 TX Queue #13, #(16 * n + 13) Schedule 00100010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QTX_SCH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QTX_SCH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
31:0	QTX_SCH	Please refer the description of QTX_SCH_0, the same definition.

151044D8 QTX_HEAD_13 TX Queue #13, #(16 * n + 13) Head Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	TX_DES_HEAD															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DES_HEAD															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DES_HEAD	TX descriptor head pointer in Queue #

151044DC QTX_TAIL_13 TX Queue #13, #(16 * n + 13) Tail Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_TAIL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DES_TAIL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DES_TAIL	TX descriptor tail pointer in Queue #

151044E0 QTX_CFG_14 TX Queue #14, #(16 * n + 14) Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	HW_RESV_CNT								SW_RESV_CNT							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	TX_DES_CNT	TX descriptor count in Queue #
15:8	HW_RESV_CNT	Buffer Reserved for HW path The reserved buffer number is specified on QDMA_RES_THRES.
7:0	SW_RESV_CNT	Buffer Reserved for SW path The reserved buffer number is specified on QDMA_RES_THRES.

151044E4 QTX_SCH_14 TX Queue #14, #(16 * n + 14) Schedule 00100010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QTX_SCH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QTX_SCH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
31:0	QTX_SCH	Please refer the description of QTX_SCH_0, the same definition.

151044E8 QTX_HEAD_14 TX Queue #14, #(16 * n + 14) Head Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_HEAD															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DES_HEAD															
Type	RO															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DES_HEAD	TX descriptor head pointer in Queue #

151044EC QTX_TAIL_14 TX Queue #14, #(16 * n + 14) Tail Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_TAIL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DES_TAIL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DES_TAIL	TX descriptor tail pointer in Queue #

151044F0 QTX_CFG_15 TX Queue #15, #(16 * n + 15) Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HW_RESV_CNT								SW_RESV_CNT							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	TX_DES_CNT	TX descriptor count in Queue #
15:8	HW_RESV_CNT	Buffer Reserved for HW path
		The reserved buffer number is specified on QDMA_RES_THRES.
7:0	SW_RESV_CNT	Buffer Reserved for SW path

Bit(s)	Name	Description
		The reserved buffer number is specified on QDMA_RES_THRES.

151044F4 QTX_SCH_15 TX Queue #15, #(16 * n + 15) Schedule 00100010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QTX_SCH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QTX_SCH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
31:0	QTX_SCH	Please refer the description of QTX_SCH_0, the same definition.

151044F8 QTX_HEAD_15 TX Queue #15, #(16 * n + 15) Head Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_HEAD															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DES_HEAD															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DES_HEAD	TX descriptor head pointer in Queue #

151044FC QTX_TAIL_15 TX Queue #15, #(16 * n + 15) Tail Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	TX_DES_TAIL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DES_TAIL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DES_TAIL	TX descriptor tail pointer in Queue #

15104500 QRX_BASE_PTR_0 RX Ring #0 Base Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_BASE_PTR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_BASE_PTR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_BASE_PTR	Point to the base address of RX Ring # (4-DW aligned address)

15104504 QRX_MAX_CNT_0 RX Ring #0 Maximum Count 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name					RX_MAX_CNT										
Type					RW										
Reset					0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	RX_MAX_CNT	The maximum number of RXD count in RX Ring #

15104508 QRX_CRX_IDX_0 RX Ring #0 CPU pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RX_CRX_IDX											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	RX_CRX_IDX	Point to the next RXD CPU wants to use

1510450C QRX_DRX_IDX_0 RX Ring #0 DMA pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RX_DRX_IDX											
Type					RO											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	RX_DRX_IDX	Point to the next RXD DMA wants to use

15104510 QRX_BASE_PTR_1 RX Ring #1 Base Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

15104514 QRX_MAX_CNT_1 RX Ring #1 Maximum Count 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

15104518 QRX_CRX_IDX_1 RX Ring #1 CPU pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

1510451C QRX DRX IDX 1 RX Ring #1 DMA pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

15104580 VQTX_TB_BASE_0 TX Virtual Queue Table #0 Base Address 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	VQTX_TB_BASE_0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VQTX_TB_BASE_0															

Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	VQTX_TB_BASE_0	Base address of TX Virtual Queue Table #0 This virtual queue table belongs to virtual queue group #0

15104584 VQTX_TB_BASE_1 TX Virtual Queue Table #1 Base Address 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	VQTX_TB_BASE_1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VQTX_TB_BASE_1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	VQTX_TB_BASE_1	Base address of TX Virtual Queue Table #1 This virtual queue table belongs to virtual queue group #1

15104588 VQTX_TB_BASE_2 TX Virtual Queue Table #2 Base Address 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	VQTX_TB_BASE_2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VQTX_TB_BASE_2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	VQTX_TB_BASE_2	Base address of TX Virtual Queue Table #2 This virtual queue table belongs to virtual queue group #2

1510458C VQTX_TB_BASE_3 TX Virtual Queue Table #3 Base Address 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	VQTX_TB_BASE_3															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VQTX_TB_BASE_3															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	VQTX_TB_BASE_3	Base address of TX Virtual Queue Table #3 This virtual queue table belongs to virtual queue group #3

15104590 VQTX_TB_BASE_4 TX Virtual Queue Table #4 Base Address 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	VQTX_TB_BASE_4															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VQTX_TB_BASE_4															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	VQTX_TB_BASE_4	Base address of TX Virtual Queue Table #4 This virtual queue table belongs to virtual queue group #4

15104594 VQTX_TB_BASE_5 TX Virtual Queue Table #5 Base Address 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	VQTX_TB_BASE_5															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VQTX_TB_BASE_5															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	VQTX_TB_BASE_5	Base address of TX Virtual Queue Table #5 This virtual queue table belongs to virtual queue group #5

15104598 VQTX_TB_BASE_6 TX Virtual Queue Table #6 Base Address 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	VQTX_TB_BASE_6															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VQTX_TB_BASE_6															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	VQTX_TB_BASE_6	Base address of TX Virtual Queue Table #6 This virtual queue table belongs to virtual queue group #6

1510459C VQTX_TB_BASE_7 TX Virtual Queue Table #7 Base Address 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	VQTX_TB_BASE_7															
Type	RW															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VQTX_TB_BASE_7															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	VQTX_TB_BASE_7	Base address of TX Virtual Queue Table #7 This virtual queue table belongs to virtual queue group #7

151045F0 QDMA_PAGE QDMA Configuration Page 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													QTX_CFG_PAGE			
Type													RW			
Reset													0	0	0	0

Bit(s)	Name	Description
3:0	QTX_CFG_PAGE	Switch the page of per physical queue configuration registers This setting will control following registers: QTX_CFG_*/QTX_SCH_*/QTX_HEAD_*/QTX_TAIL_*/RST_TX_IDX*/QDMA_DROP_PREC/FORCE_QUE

15104600 QDMA_INFO QDMA Information 0C010080

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV				INDEX_WIDTH											
Type	RO				RO											
Reset	0	0	0	0	1	1	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	TX_QUE_NUM															
Type	RO															
Reset	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:28	REV	QDMA revision
27:24	INDEX_WIDTH	Ring index width
15:0	TX_QUE_NUM	TX queue number

15104604 QDMA_GLO_CFG QDMA Global Configuration 55404530

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_2B_OFFSET	CSR_CLKGATE_BYP	BYTE_SWAP		PKT_RX_WDONE	DMAD_WR_WDONE										
Type	RW	RW	RW		RW	RW										
Reset	0	1	0		0	1										
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MUTLI_CNT				LEAKY_BK			MUTLI_DMA	BIG_ENDIAN		QDMA_BT_SIZE		RX_DMA_BUSY	RX_DMA_EN	TX_DMA_BUSY	TX_DMA_EN
Type	RW				RW			RW	RW		RW		RO	RW	RO	RW
Reset	0	1	0	0	0			1	0		1	1	0	0	0	0

Bit(s)	Name	Description
31	RX_2B_OFFSET	Prepend 2-Byte to RX-buffer (packet) for aligning IP header to 32-bit boundary. Default MAC header is 14-Byte
30	CSR_CLKGATE_BYP	Clock gated Bypass
29	BYTE_SWAP	Byte Swap
27	PKT_RX_WDONE	Packet Payload Write Done Check
26	DMAD_WR_WDONE	Packet Descriptor Write Done Check
15:12	MUTLI_CNT	Number of TX DMA read outstanding transactions when QDMA_GLO_CFG[8] = 1'b1.
11	LEAKY_BK	Select bucket type for TX queue MAX sharper and MIN sharper
8	MUTLI_DMA	Enable TX DAM AXI read outstanding transaction
7	BIG_ENDIAN	Big-endian
5:4	QDMA_BT_SIZE	The burst size of QDMA
3	RX_DMA_BUSY	
2	RX_DMA_EN	
1	TX_DMA_BUSY	

Bit(s)	Name	Description
0	TX_DMA_EN	

15104608 QDMA_RST_IDX QDMA Reset Index 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				RST_SCH											RST_DRX_IDX1	RST_DRX_IDX0
Type				RW											RW	RW
Reset				0											0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RST_TX_IDX15	RST_TX_IDX14	RST_TX_IDX13	RST_TX_IDX12	RST_TX_IDX11	RST_TX_IDX10	RST_TX_IDX9	RST_TX_IDX8	RST_TX_IDX7	RST_TX_IDX6	RST_TX_IDX5	RST_TX_IDX4	RST_TX_IDX3	RST_TX_IDX2	RST_TX_IDX1	RST_TX_IDX0
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28	RST_SCH	Write 1 to reset all token bucket of scheduler Only valid when QTX_CFG_PAGE = 0
17	RST_DRX_IDX1	Write 1 to reset RX_DMA RX_IDX1 to 0 Only valid when QTX_CFG_PAGE = 0
16	RST_DRX_IDX0	Write 1 to reset RX_DMA RX_IDX0 to 0 Only valid when QTX_CFG_PAGE = 0
15	RST_TX_IDX15	Write 1 to reset TX_DMA TX_IDX (16 * QTX_CFG_PAGE + 15) to 0
14	RST_TX_IDX14	Write 1 to reset TX_DMA TX_IDX (16 * QTX_CFG_PAGE + 14) to 0
13	RST_TX_IDX13	Write 1 to reset TX_DMA TX_IDX (16 * QTX_CFG_PAGE + 13) to 0
12	RST_TX_IDX12	Write 1 to reset TX_DMA TX_IDX (16 * QTX_CFG_PAGE + 12) to 0
11	RST_TX_IDX11	Write 1 to reset TX_DMA TX_IDX (16 * QTX_CFG_PAGE + 11) to 0
10	RST_TX_IDX10	Write 1 to reset TX_DMA TX_IDX (16 * QTX_CFG_PAGE + 10) to 0
9	RST_TX_IDX9	Write 1 to reset TX_DMA TX_IDX (16 * QTX_CFG_PAGE + 9) to 0
8	RST_TX_IDX8	Write 1 to reset TX_DMA TX_IDX (16 * QTX_CFG_PAGE + 8) to 0
7	RST_TX_IDX7	Write 1 to reset TX_DMA TX_IDX (16 * QTX_CFG_PAGE + 7) to 0
6	RST_TX_IDX6	Write 1 to reset TX_DMA TX_IDX (16 * QTX_CFG_PAGE + 6) to 0
5	RST_TX_IDX5	Write 1 to reset TX_DMA TX_IDX (16 * QTX_CFG_PAGE + 5) to 0
4	RST_TX_IDX4	Write 1 to reset TX_DMA TX_IDX (16 * QTX_CFG_PAGE + 4) to 0
3	RST_TX_IDX3	Write 1 to reset TX_DMA TX_IDX (16 * QTX_CFG_PAGE + 3) to 0
2	RST_TX_IDX2	Write 1 to reset TX_DMA TX_IDX (16 * QTX_CFG_PAGE + 2) to 0
1	RST_TX_IDX1	Write 1 to reset TX_DMA TX_IDX (16 * QTX_CFG_PAGE + 1) to 0
0	RST_TX_IDX0	Write 1 to reset TX_DMA TX_IDX (16 * QTX_CFG_PAGE + 0) to 0

1510460C QDMA_DELAY_INT

Delay Interrupt Configuration

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RXDLY_INT_EN	RXMAX_PINT							RXMAX_PTIME							
Type	RW	RW							RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RLS_DINT_EN	RLS_MAX_PINT							RLS_MAX_PTIME							
Type	RW	RW							RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	RXDLY_INT_EN	
30:24	RXMAX_PINT	Specified Max. number of pended interrupts When the number of pended interrupts is equal or greater than the value specified here or interrupt pending time reach the limit (see below), a final RX_DLY_INT is generated. [Note] reset to 0 can disable pending interrupt count check.
23:16	RXMAX_PTIME	Specified Max. pended time When the pending time is equal or greater than RXMAX_PTIME x 20us or the number of pended RX_DONE is equal or greater than RXMAX_PINT (see above), a final RX_DLY_INT is generated. [Note] reset to 0 can disable pending interrupt time check.
15	RLS_DINT_EN	
14:8	RLS_MAX_PINT	Specified Max. number of pended interrupts When the number of pended interrupts is equal or greater than the value specified here or interrupt pending time reach the limit (see below), a final RLS_DLY_INT is generated. [Note] reset to 0 can disable pending interrupt count check.
7:0	RLS_MAX_PTIME	Specified Max. pended time When the pending time is equal or greater than RLS_MAX_PTIME x 20us or the number of pended RX_DONE is equal or greater than RLS_MAX_PINT (see above), a final RLS_DLY_INT is generated. [Note] reset to 0 can disable pending interrupt time check.

15104610	QDMA FC THRES				Flow Control Threshold										90904444	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SW_DROP_FST_VQ_MODE	SW_DROP_MODE		SW_DROP_FST_VQ		SW_DROP_FST_VQ	SW_DROP_FST_VQ	SW_DROP_FST_VQ	HW_DROP_FST_VQ_MODE	HW_DROP_FST_VQ_MODE	HW_DROP_FST_VQ_MODE	HW_DROP_FST_VQ_MODE	HW_DROP_FST_VQ_MODE		HW_DROP_FST_VQ_MODE	HW_DROP_FST_VQ_MODE
Type	RW	RW		RW		RW	RW	RW	RW	RW	RW	RW	RW		RW	RW

Reset	1	0	0	1	0		0	0	1	0	0	1	0		0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SHARE_SW_TH				SHARE_HW_TH				FREE_TH				RING_TH			
Type	RW				RW				RW				RW			
Reset	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0

Bit(s)	Name	Description
31:30	SW_DROP_FSTVQ_MODE	SW drop condition on fullest virtual queue If the corresponding PQ SW occupied queue depth over the SW_RESV_CNT, the en-queuing packet to fullest VQ will be drop depends on the usage of SW free-for-all buffer.
29:28	SW_DROP_MODE	Drop Distribution Mode for SW Drop Different drop probability when SW Free for All buffer usage (>75% / >50% / >25% / >0%) Drop Probability:
27	SW_DROP_FSTVQ	SW drop en-queuing packet on fullest virtual queue, only take effect on the physical queues those binding with virtual queues.
25	SW_DROP_FFA	Flow Control Drop QDMA asserts FC when FFA is equal to 0 and egress queue count is bigger than the reserved queue count. However, the de-assert condition is specified on this control bit.
24	SW_DROP_EN	Enable Flow Control for SW buffer pool QDMA drop packets when FFA is equal to 0 and the egress queue count is bigger than the reserved queue count.
23:22	HW_DROP_FSTVQ_MODE	HW drop condition on fullest virtual queue If the corresponding PQ SW occupied queue depth over the SW_RESV_CNT, the en-queuing packet to fullest VQ will be drop depends on the usage of HW free-for-all buffer.
21:20	HW_REDDROP_MODE	Random Early Drop Distribution Mode for HW Drop Four different drop probability when HW Free-for-All(FFA) buffer usage is (>75% / >50% / >25% / >0%) Drop Probability:
19	HW_DROP_FSTVQ	HW drop en-queuing packet on fullest virtual queue, only take effect on the physical queues those binding with virtual queues.
17	HW_FC_RELEASE	Flow Control Release Condition (not for RED) QDMA asserts FC when FFA is equal to DROP/PFC condition and the egress queue count is bigger than the reserved queue count. However, the de-assert condition is specified on this control bit.
16	HW_DROP_EN	Drop packets when HW flow control is asserted QDMA drop packets when Free-for-all(FFA) is equal to 0 and the egress queue count is bigger than the reserved queue count.
15:12	SHARE_SW_TH	SW Shared buffer threshold QDMA will drop TX packets when the left shared buffer descriptors reach this threshold
11:8	SHARE_HW_TH	HW Shared buffer threshold QDMA will drop TX packets when the left shared buffer descriptors reach this threshold
7:4	FREE_TH	RX free buffer threshold

Bit(s)	Name	Description
3:0	RING_TH	QDMA will pause RXDMA interface when the left free buffer descriptors reach this threshold RX Ring threshold QDMA will pause RXDMA interface when the left RX ring descriptors reach this threshold

15104614 QDMA_FC_MODE QDMA Flow Control Mode 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved												TX_PFC_RELEASE	TX_PFC_ASSERT	TX_PFC_MODE	
Type	RW												RW	RW	RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:4	Reserved	Reserved
3	TX_PFC_RELEASE	PFC Loose Release QDMA TX queue assert PFC signal only if the egress queue count is bigger than the reserved queue count.
2	TX_PFC_ASSERT	PFC Strict Assertion QDMA TX queue assert PFC signal only if the egress queue count is bigger than the reserved queue count.
1:0	TX_PFC_MODE	Priority Flow Control Assertion Mode QDMA TXQ asserts PFC signal to PSE when Free-for-all(FFA) usage reach the value and TXQ is bigger than the reserved queue count. When PFC is asserted, the de-asserted condition is that FFA is less than the value and TXQ drops a half lower than the reserved queue count.

15104618 QDMA_INT_STS Interrupt Status 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_COHERENT	RX_DLY_INT	RLS_COHERENT	RLS_DLY_INT												RX_DONE_INT0
Type	W1C	W1C	W1C	W1C												W1C

Reset	0	0	0	0												0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VQDEP_DEQ_ERR1	VQDEP_DEQ_ERR0	VQDEP_ENQ_ERR1	VQDEP_ENQ_ERR0				FWD_FIFO_OV				QTX_REQ_EMP_VQ				RLS_DONE_INT
Type	W1C	W1C	W1C	W1C				W1C				W1C				W1C
Reset	0	0	0	0				0				0				0

Bit(s)	Name	Description
31	RX_COHERENT	RX_DMA finds data coherent event while checking DDONE bit.
30	RX_DLY_INT	Summary of the whole QDMA RX related interrupts.
29	RLS_COHERENT	TX_DMA finds data coherent event while checking DDONE bit.
28	RLS_DLY_INT	Summary of the whole QDMA TX related interrupts.
16	RX_DONE_INT0	RX ring #0 packet receive interrupt
15	VQDEP_DEQ_ERR1	VQ depth mismatch with the VQHPTR & VQTPTR during de-queuing. A VQ not empty yet after de-queuing, but the remainder VQ_DEPTH >= 1
14	VQDEP_DEQ_ERR0	VQ depth mismatch with the VQHPTR & VQTPTR during de-queuing. A VQ becomes empty after de-queuing but the remainder VQ_DEPTH = 0
13	VQDEP_ENQ_ERR1	VQ depth mismatch with the VQHPTR & VQTPTR during en-queuing. A VQ been en-queued the first packet descriptor, but the VQ_DEPTH already >=1.
12	VQDEP_ENQ_ERR0	VQ depth mismatch with the VQHPTR & VQTPTR during en-queuing. A VQ been en-queued a packet descriptor, but the VQ_DEPTH already full = 16'hffff.
8	FWD_FIFO_OV	Forwarding engine FIFO overflow interrupt
4	QTX_REQ_EMP_VQ	QDMA TX request to transmit an empty VQ
0	RLS_DONE_INT	CPU release transmitted packet interrupt

1510461C QDMA INT MASK Interrupt Mask 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_COHERENT	RX_DLY_INT	RLS_COHERENT	RLS_DLY_INT												RX_DONE_INT0
Type	RW	RW	RW	RW												RW
Reset	0	0	0	0												0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VQDEP_DEQ_ERR1	VQDEP_DEQ_ERR0	VQDEP_ENQ_ERR1	VQDEP_ENQ_ERR0				FWD_FIFO_OV				QTX_REQ_EMP_VQ				RLS_DONE_INT
Type	RW	RW	RW	RW				RW				RW				RW

Reset	0	0	0	0				0				0				0

Bit(s)	Name	Description
31	RX_COHERENT	Interrupt enable for RX_DMA data coherent vent
30	RX_DLY_INT	Summary of the whole QDMA RX related interrupts.
29	RLS_COHERENT	Interrupt enable for TX_DMA data coherent vent
28	RLS_DLY_INT	Summary of the whole QDMA TX related interrupts.
16	RX_DONE_INT0	RX ring #0 packet receive interrupt
15	VQDEP_DEQ_ERR1	VQ depth mismatch with the VQHPTR & VQTPTR during de-queuing. A VQ not empty yet after de-queuing, but the remainder VQ_DEPTH >= 1
14	VQDEP_DEQ_ERR0	VQ depth mismatch with the VQHPTR & VQTPTR during de-queuing. A VQ becomes empty after de-queuing but the remainder VQ_DEPTH = 0
13	VQDEP_ENQ_ERR1	VQ depth mismatch with the VQHPTR & VQTPTR during en-queuing. A VQ been en-queued the first packet descriptor, but the VQ_DEPTH already >= 1.
12	VQDEP_ENQ_ERR0	VQ depth mismatch with the VQHPTR & VQTPTR during en-queuing. A VQ been en-queued a packet descriptor, but the VQ_DEPTH already full = 16'hffff.
8	FWD_FIFO_OV	Forwarding engine FIFO overflow interrupt
4	QTX_REQ_EMP_VQ	QDMA TX request to transmit an empty VQ
0	RLS_DONE_INT	CPU release transmitted packet interrupt

15104620 QDMA_INT_GRP1 QDMA Interrupt Group 1 Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_INT_GRP1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_INT_GRP1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	QDMA_INT_GRP1	Interrupt group 1 assignment. Each bit's definition is same as "QDMA_INT_STS"

15104624 QDMA_INT_GRP2 QDMA Interrupt Group 2 Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_INT_GRP2															

Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_INT_GRP2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	QDMA_INT_GRP2	Interrupt group 2 assignment. Each bit's definition is same as "QDMA_INT_STS"

15104628 **QDMA_DROP_PREC** **QDMA Drop by FFA Percentage Control** 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SW_DROP_PREC															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HW_DROP_PREC															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	SW_DROP_PREC	QDMA SW Drop by FFA Percentage Control QDMA drop packets based on the full percentage of Free-for-All [31:16] = [PQ#(16 * QTX_CFG_PAGE + 15) : PQ#(16 * QTX_CFG_PAGE + 0)]
15:0	HW_DROP_PREC	QDMA HW Drop by FFA Percentage Control QDMA drop packets based on the full percentage of Free-for-All [15:0] = [PQ#(16 * QTX_CFG_PAGE + 15) : PQ#(16 * QTX_CFG_PAGE + 0)]

1510462C **QDMA_DEBUG** **Debug Mode** 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																

Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

15104630 QDMA TEST Test Mode A0000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

15104634 QDMA DMA QDMA DMA FSM 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																

Type																
Reset																

Bit(s)	Name	Description

15104638 QDMA BMU QDMA BMU FSM 00010000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

1510463C QDMA MON QDMA Monitor for Error Interrupt Event 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

15104640 QDMA_HRED1 QDMA HW RED Distribution - I FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FFA_LOW_UTIL															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FFA_MIDDLE_UTIL															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:16	FFA_LOW_UTIL	Low Utilization of FFA on HW path When the utilization of FFA reaches the threshold, RED will start to drop the en-queued packets by 25% probability.
15:0	FFA_MIDDLE_UTIL	Middle Utilization of FFA on HW path When the utilization of FFA reaches the threshold, RED will start to drop the en-queued packets by 50% probability.

15104644 QDMA_HRED2 QDMA HW RED Distribution - II FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REVO															FFA_UTIL_SEL
Type	RW															RW
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FFA_HIGH_UTIL															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:17	REVO	Reserved
16	FFA_UTIL_SEL	Manually Set FFA Utilization When the bit is set, FFA Utilization will be configurable for user.
15:0	FFA_HIGH_UTIL	High Utilization of FFA on HW path When the utilization of FFA reaches the threshold, RED will start to drop the en-queued packets by 75% probability.

Bit(s)	Name	Description

15104648	<u>QDMA_SRED1</u>				QDMA SW RED Distribution - I												FFFFFFFF	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16		
Name	FFA_LOW_UTIL																	
Type	RW																	
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1		
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
Name	FFA_MIDDLE_UTIL																	
Type	RW																	
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1		

Bit(s)	Name	Description
31:16	FFA_LOW_UTIL	Low Utilization of FFA on HW path When the utilization of FFA reaches the threshold, RED will start to drop the en-queued packets by 25% probability.
15:0	FFA_MIDDLE_UTIL	Middle Utilization of FFA on CPU path When the utilization of FFA reaches the threshold, RED will start to drop the en-queued packets by 50% probability.

1510464C	QDMA_SRED2				QDMA SW RED Distribution - II												FFFFFFFF	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16		
Name	REV0															FFA_UTIL_SEL		
Type	RW															RW		
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1		
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
Name	FFA_MIDDLE_UTIL																	
Type	RW																	
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1		

Bit(s)	Name	Description
31:17	REV0	Reserved
16	FFA_UTIL_SEL	Manually Set FFA Utilization

Bit(s)	Name	Description
15:0	FFA_MIDDLE_UTIL	When the bit is set, FFA Utilization will be configurable for user. High Utilization of FFA on CPU path When the utilization of FFA reaches the threshold, RED will start to drop the en-queued packets by 75% probability.

15104650 QTX Q0MIN BK QDMA Queue #0 Min. Bucket 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

15104654 QTX Q1MIN BK QDMA Queue #1 Min. Bucket 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

15104658 QTX Q2MIN BK QDMA Queue #2 Min. Bucket 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

1510465C QTX_Q3MIN_BK QDMA Queue #3 Min. Bucket 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

15104660 QTX_Q0MAX_BK QDMA Queue #0 Max. Bucket 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

15104664 **QTX Q1MAX BK** **QDMA Queue #1 Max. Bucket** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

15104668 **QTX Q2MAX BK** **QDMA Queue #2 Max. Bucket** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

1510466C QTX Q3MAX BK QDMA Queue #3 Max. Bucket 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

15104670 QDMA_INT_STS_G0 QDMA Interrupt Status Group 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_INT_STS_G0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_INT_STS_G0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	QDMA_INT_STS_G0	Interrupt group 0 status, this information already "and" with "QDMA_INT_IMR" Each bit definition is same as "QDMA_INT_STS"

15104674 QDMA_INT_STS_G1 QDMA Interrupt Status Group 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_INT_STS_G1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_INT_STS_G1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	QDMA_INT_STS_G1	Interrupt group 1 status, this information already "and" with "QDMA_INT_IMR" Each bit definition is same as "QDMA_INT_STS"

15104678 QDMA_INT_STS_G2 QDMA Interrupt Status Group 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_INT_STS_G2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_INT_STS_G2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	QDMA_INT_STS_G2	Interrupt group 2 status, this information already "and" with "QDMA_INT_IMR" Each bit definition is same as "QDMA_INT_STS"

15104680 VQTX_GLO TX Virtual Queue Global Configuration 000005EA

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name															VQTB_MIB_EN	
Type															RW	
Reset															0	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VQTX_GQTUM															
Type	RW															
Reset	0	0	0	0	0	1	0	1	1	1	1	0	1	0	1	0

Bit(s)	Name	Description
17	VQTB_MIB_EN	Configuration for the MIB packet/byte counter field of virtual queue table
15:0	VQTX_GQTUM	Amount of bytes a virtual queue is allowed to de-queue before the scheduler moves to the next virtual queue. Defaults to the MTU of the interface. The minimum value is 1.

1510468C VQTX_INVLD_PTR TX Virtual Queue Invalid Pointer DEADBEEF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	VQTX_INVLD_PTR															
Type	RW															
Reset	1	1	0	1	1	1	1	0	1	0	1	0	1	1	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VQTX_INVLD_PTR															
Type	RW															
Reset	1	0	1	1	1	1	1	0	1	1	1	0	1	1	1	1

Bit(s)	Name	Description
31:0	VQTX_INVLD_PTR	The pointer address indicates a invalid virtual queue head/tail pointer. Either "VQHPTR" or "VQTPTR" of VQ table is equal to this invalid pointer VQTX_INVLD_PTR, which means there is no valid packet in this virtual queue.

15104690 VQTX_NUM Number of TX Virtual Queue Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name		VQTX_NUM_7				VQTX_NUM_6				VQTX_NUM_5				VQTX_NUM_4		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		VQTX_NUM_3				VQTX_NUM_2				VQTX_NUM_1				VQTX_NUM_0		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Name	Description
30:28	VQTX_NUM_7	Number of virtual queues in virtual queue group #7
26:24	VQTX_NUM_6	Number of virtual queues in virtual queue group #6
22:20	VQTX_NUM_5	Number of virtual queues in virtual queue group #5
18:16	VQTX_NUM_4	Number of virtual queues in virtual queue group #4
14:12	VQTX_NUM_3	Number of virtual queues in virtual queue group #3
10:8	VQTX_NUM_2	Number of virtual queues in virtual queue group #2
6:4	VQTX_NUM_1	Number of virtual queues in virtual queue group #1
2:0	VQTX_NUM_0	Number of virtual queues in virtual queue group #0

15104698 VQTX_SCH TX Virtual Queue Schedule Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			VQTX_SCH_7				VQTX_SCH_6				VQTX_SCH_5				VQTX_SCH_4	
Type			RW				RW				RW				RW	
Reset			0	0			0	0			0	0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			VQTX_SCH_3				VQTX_SCH_2				VQTX_SCH_1				VQTX_SCH_0	
Type			RW				RW				RW				RW	
Reset			0	0			0	0			0	0			0	0

Bit(s)	Name	Description
29:28	VQTX_SCH_7	Virtual queues scheduling strategy for virtual queue group #7
25:24	VQTX_SCH_6	Virtual queues scheduling strategy for virtual queue group #6
21:20	VQTX_SCH_5	Virtual queues scheduling strategy for virtual queue group #5
17:16	VQTX_SCH_4	Virtual queues scheduling strategy for virtual queue group #4
13:12	VQTX_SCH_3	Virtual queues scheduling strategy for virtual queue group #3
9:8	VQTX_SCH_2	Virtual queues scheduling strategy for virtual queue group #2
5:4	VQTX_SCH_1	Virtual queues scheduling strategy for virtual queue group #1

Bit(s)	Name	Description
1:0	VQTX_SCH_0	Virtual queues scheduling strategy for virtual queue group #0

151046A0 VQTX_HASH_CFG TX Virtual Queue Hash Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					HASH_PT B_MODE EN_3	HASH_PT B_MODE EN_2	HASH_PT B_MODE EN_1	HASH_PT B_MODE EN_0			HASH_ST MODE					HASH_PT B_PRD
Type					RW	RW	RW	RW			RW					RW
Reset					0	0	0	0			0	0				0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HASH_PT B_PRD															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
27	HASH_PT B_MODE EN_3	Enable "Exclusive with CRC32" as a candidate algorithm for perturbed hash changing. This field only valid when HASH_PT B_PRD!=0.
26	HASH_PT B_MODE EN_2	Enable "Exclusive with (B^(A&~C))" as a candidate algorithm for perturbed hash changing. This field only valid when HASH_PT B_PRD!=0.
25	HASH_PT B_MODE EN_1	Enable "Exclusive with (A&B) (~A&C)" as a candidate algorithm for perturbed hash changing. This field only valid when HASH_PT B_PRD!=0.
24	HASH_PT B_MODE EN_0	Enable "Exclusive with HASH_SEED" as a candidate algorithm for perturbed hash changing. This field only valid when HASH_PT B_PRD!=0. (If HASH_PT B_MODE EN_0~3 are all "0", hash will be forced on "Exclusive with HASH_SEED" mode.)
21:20	HASH_ST MODE	Hash scrambled mode selection, for static hash virtual queue index generating.
16:0	HASH_PT B_PRD	This field only valid when HASH_PT B_PRD=0 If HASH_PT B_PRD = 0, means operating in static hash mode, never changing the hash algorithm periodically. Otherwise, operating in perturb hash mode when HASH_PT B_PRD != 0. HASH_PT B_PRD Indicates the period to change the hash algorithm for virtual queue index generating, in 1ms unit.

151046A4 VQTX_HASH_SD TX Virtual Queue Hash Seed 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	HASH_SD															
Type	RW															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HASH_SD															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	HASH_SD	Hash seed for "Exclusive with HASH_SEED" mode.

151046B0 VQTX_VLD_CFG TX Virtual Queue Valid Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	VQTX_VLD_STRG_7				VQTX_VLD_STRG_6				VQTX_VLD_STRG_5				VQTX_VLD_STRG_4			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VQTX_VLD_STRG_3				VQTX_VLD_STRG_2				VQTX_VLD_STRG_1				VQTX_VLD_STRG_0			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:28	VQTX_VLD_STRG_7	Virtual Queue Group #7: Virtual queue valid bit map starting slice number.
27:24	VQTX_VLD_STRG_6	Virtual Queue Group #6: Virtual queue valid bit map starting slice number.
23:20	VQTX_VLD_STRG_5	Virtual Queue Group #5: Virtual queue valid bit map starting slice number.
19:16	VQTX_VLD_STRG_4	Virtual Queue Group #4: Virtual queue valid bit map starting slice number.
15:12	VQTX_VLD_STRG_3	Virtual Queue Group #3: Virtual queue valid bit map starting slice number.
11:8	VQTX_VLD_STRG_2	Virtual Queue Group #2: Virtual queue valid bit map starting slice number.
7:4	VQTX_VLD_STRG_1	Virtual Queue Group #1: Virtual queue valid bit map starting slice number.
3:0	VQTX_VLD_STRG_0	Virtual Queue Group #0: Virtual queue valid bit map starting slice number.
1 VQ valid bit slice comprises 64 bit map.		

Bit(s)	Name	Description
		The amount of VQ valid slices for 1 VQ group depends on the setting of "VQTX_NUM_#", hardware will allocate VQ valid bit slices for each VQ group.

151046BC QTX_MIB_IF TX Queue MIB Interface 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			MIB_RC_DIS	VQTX_MIB_EN				MIB_PQ_SHW_SEP		QTX_MIB_QID						
Type			RW	W1				RW		RW						
Reset			0	0				0		0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							QTX_MIB_VQID									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29	MIB_RC_DIS	Disable the clear action during MIB reading
28	VQTX_MIB_EN	Enable VQTB MIB read procedure
24	MIB_PQ_SHW_SEP	Separate the PQ's HW/SW MIB counter of QTX_MIB_PCNT and QTX_MIB_DPCNT
22:16	QTX_MIB_QID	Physical queue ID for MIB accessing
9:0	QTX_MIB_VQID	Virtual queue ID for MIB accessing

151046C0 VQTX_MIB_PCNT TX Virtual Queue MIB Packet Count 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	VQTX_MIB_PCNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VQTX_MIB_PCNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	VQTX_MIB_PCNT	Packet count of virtual queue table, according to QTX_MIB_QID and QTX_MIB_VQID. Unavailable when VQTB_MIB_EN = 0

151046C4 VQTX_MIB_BCNTL TX Virtual Queue MIB Byte Count Low Bytes 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	VQTX_MIB_BCNTL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VQTX_MIB_BCNTL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	VQTX_MIB_BCNTL	Byte count [31:0] of virtual queue table, according to QTX_MIB_QID and QTX_MIB_VQID. Unavailable when VQTB_MIB_EN = 0

151046C8 VQTX_MIB_BCNTL TX Virtual Queue MIB Byte Count High Bytes 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	VQTX_MIB_BCNTL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VQTX_MIB_BCNTL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	VQTX_MIB_BCNTL	Byte count [63:32] of virtual queue table, according to QTX_MIB_QID and QTX_MIB_VQID.

Bit(s)	Name	Description
		Unavailable when VQTB_MIB_EN = 0

151046CC VQTX_MIB_DPCNT TX Virtual Queue MIB Drop Packet Count 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	VQTX_MIB_DPCNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VQTX_MIB_DPCNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	VQTX_MIB_DPCNT	Dropped packet count of virtual queue table, according to QTX_MIB_QID and QTX_MIB_VQID. Unavailable when VQTB_MIB_EN = 0

151046D0 QTX_MIB_PCNT TX Physical Queue MIB Forward Packet Count 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QTX_MIB_PCNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QTX_MIB_PCNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	QTX_MIB_PCNT	Accumulated forwarded packet count, according to QTX_MIB_QID. If MIB_PQ_SHW_SEP = 1, this counter will be separated into two 16bits counter, [31:16] for software path, [15:0] for hardware path.

151046D4 QTX_MIB_DPCNT TX Physical Queue MIB Dropped Packet Count 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QTX_MIB_DPCNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QTX_MIB_DPCNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	QTX_MIB_DPCNT	Accumulated dropped packet count, according to QTX_MIB_QID. If MIB_PQ_SHW_SEP = 1, this counter will be separated into two 16bits counter, [31:16] for software path, [15:0] for hardware path.

151046D8 QTX_MIB_BCNTL TX Physical Queue MIB Byte Count Low Bytes 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QTX_MIB_BCNTL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QTX_MIB_BCNTL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	QTX_MIB_BCNTL	Accumulated forwarded byte count [31:0] of physical queue #QTX_MIB_QID. Read QTX_MIB_BCNTL will not clear the value of QTX_MIB_BCNTL, QTX_MIB_BCNTL will be cleared by reading QTX_MIB_BCNTH when VQTB_MIB_RC_DIS=0.

151046DC QTX_MIB_BCNTH TX Physical Queue MIB Byte Count High Bytes 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QTX_MIB_BCNTH															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QTX_MIB_BCNTH															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	QTX_MIB_BCNTH	Accumulated forwarded byte count [35:32] of physical queue #QTX_MIB_QID If VQTB_MIB_RC_DIS=0, read QTX_MIB_BCNTH will clear the value of QTX_MIB_BCNTH & QTX_MIB_BCNTL.

15104700 QTX_CTX_PTR TX Forward CPU Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FWD_CTX_PTR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FWD_CTX_PTR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	FWD_CTX_PTR	TX forward chain CPU pointer

15104704 QTX_DTX_PTR TX Forward DMA Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FWD_DTX_PTR															
Type	RW															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FWD_DTX_PTR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	FWD_DTX_PTR	TX forward chain DMA pointer When QDMA TX is disabled, this field can be set to the initial pointer by CPU. After QDMA TX is enabled, this field is read-only.

15104708 QTX_FWD_CNT TX Forward DMA Counter 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ACC_HW_CNT															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ACC_SW_CNT															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	ACC_HW_CNT	Accumulated HW forwarded counter
15:0	ACC_SW_CNT	Accumulated SW forwarded counter

15104710 QTX_CRX_PTR TX Release CPU Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RLS_CRX_PTR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RLS_CRX_PTR															

Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RLS_CRX_PTR	TX release chain CPU pointer

15104714 QTX_DRX_PTR TX Release DMA Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RLS_DRX_PTR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RLS_DRX_PTR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RLS_DRX_PTR	TX release chain DMA pointer When QDMA TX is disabled, this field can be set to the initial pointer by CPU. After QDMA TX is enabled, this field is read-only.

15104718 QTX_RLS_CNT TX Release DMA Counter 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ACC_RLS_CNT															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	ACC_RLS_CNT	Accumulated TX released descriptor count

1510471C QTX_RLS_DBASE TX Release Descriptor Base 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

15104720 QDMA_FQ_HEAD Free Page Head Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FQ_HEAD_PTR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FQ_HEAD_PTR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	FQ_HEAD_PTR	Free buffer head pointer When QDMA TX is disabled, this field can be set to the initial pointer by CPU. After QDMA TX is enabled, this field is read-only.

15104724 QDMA_FQ_TAIL Free Page Tail Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FQ_TAIL_PTR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FQ_TAIL_PTR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	FQ_TAIL_PTR	Free buffer tail pointer When QDMA TX is disabled, this field can be set to the initial pointer by CPU. After QDMA TX is enabled, this field is read-only.

15104728 QDMA_FQ_CNT Free Page Counter 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SWFQ_CNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HWFQ_CNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	SWFQ_CNT	Free buffer on CPU Pool Initial free buffer count on CPU pool when QDMA_GLO_CFG.TX_DMA_EN is de-asserted.
15:0	HWFQ_CNT	Free buffer on HW Pool Initial free buffer count on HW pool when QDMA_GLO_CFG.TX_DMA_EN is de-asserted.

1510472C QDMA_FQ_BLEN Free Page Buffer Length 08000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name			FQ_BUF_BLEN													
Type			RW													
Reset			0	0	1	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description
29:16	FQ_BUF_BLEN	Free buffer byte length Configured free buffer length, QDMA RX will fetch the length info to decide the payload length on one descriptor/buffer.

15104780 QDMA_RATE_EXPO QDMA Scheduler Rate Exponent 0 000F4240

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

15104784 QDMA_RATE_EXP1 QDMA Scheduler Rate Exponent 1 000186A0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

15104788 QDMA_RATE_EXP2 QDMA Scheduler Rate Exponent 2 00002710

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

1510478C QDMA_RATE_EXP3 QDMA Scheduler Rate Exponent 3 000003E8

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

15104790 QDMA_RATE_EXP4 QDMA Scheduler Rate Exponent 4 00000064

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

15104794 QDMA_RATE_EXP5 QDMA Scheduler Rate Exponent 5 0000000A

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

15104798 QDMA_TX_SCH1_SCH2 TX Scheduler1 and Scheduler2 Rate Control 00100010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	SCH2_MAX_WFQ	SCH2_LEAKY_BK	SCH2_BUCKET_DEP	SCH2_RATE_EN	SCH2_RATE_MAN								SCH2_RATE_EXP			
Type	RW	RW	RW	RW	RW								RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SCH1_MAX_WFQ	SCH1_LEAKY_BK	SCH1_BUCKET_DEP	SCH1_RATE_EN	SCH1_RATE_MAN								SCH1_RATE_EXP			
Type	RW	RW	RW	RW	RW								RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
31	SCH2_MAX_WFQ	Physical Queue arbitration mechanism between MIN and MAX rate
30	SCH2_LEAKY_BK	Select bucket type for scheduler output sharper
29:28	SCH2_BUCKET_DEP	Bucket Depth
27	SCH2_RATE_EN	TX SCH2 max. rate control enable
26:20	SCH2_RATE_MAN	Mantissa part of the max. rate control of the TX SCH2 Value range: 0~127
19:16	SCH2_RATE_EXP	Exponent part of the max. rate control of the TX SCH2 value selection
15	SCH1_MAX_WFQ	Physical Queue arbitration mechanism between MIN and MAX rate
14	SCH1_LEAKY_BK	Select bucket type for scheduler output sharper
13:12	SCH1_BUCKET_DEP	Bucket Depth
11	SCH1_RATE_EN	TX SCH1 max. rate control enable
10:4	SCH1_RATE_MAN	Mantissa part of the max. rate control of the TX SCH1 Value range: 0~127
3:0	SCH1_RATE_EXP	Exponent part of the max. rate control of the TX SCH2 value selection

1510479C QDMA TX SCH3 SCH4 TX Scheduler3 and Scheduler4 Rate Control 00100010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SCH4_MAX_WFQ	SCH4_LEAKY_BK	SCH4_BUCKET_DEP	SCH4_RATE_EN	SCH4_RATE_MAN								SCH4_RATE_EXP			
Type	RW	RW	RW	RW	RW								RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SCH3_MAX_WFQ	SCH3_LEAKY_BK	SCH3_BUCKET_DEP	SCH3_RATE_EN	SCH3_RATE_MAN								SCH3_RATE_EXP			

Type	RW	RW	RW		RW	RW							RW				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
31	SCH4_MAX_WFQ	Physical Queue arbitration mechanism between MIN and MAX rate
30	SCH4_LEAKY_BK	Select bucket type for scheduler output sharper
29:28	SCH4_BUCKET_DEP	Bucket Depth
27	SCH4_RATE_EN	TX SCH4 max. rate control enable
26:20	SCH4_RATE_MAN	Mantissa part of the max. rate control of the TX SCH4 Value range: 0~127
19:16	SCH4_RATE_EXP	Exponent part of the max. rate control of the TX SCH4 value selection
15	SCH3_MAX_WFQ	Physical Queue arbitration mechanism between MIN and MAX rate
14	SCH3_LEAKY_BK	Select bucket type for scheduler output sharper
13:12	SCH3_BUCKET_DEP	Bucket Depth
11	SCH3_RATE_EN	TX SCH3 max. rate control enable
10:4	SCH3_RATE_MAN	Mantissa part of the max. rate control of the TX SCH3 Value range: 0~127
3:0	SCH3_RATE_EXP	Exponent part of the max. rate control of the TX SCH3 value selection

151047A0 VQTX_DEP_TH_0_3 QDMA Virtual Queue Group #0~3 Depth Threshold 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

151047A4 VQTX_DEP_TH_4_7 QDMA Virtual Queue Group #4~7 Depth Threshold 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

151047C0 VQTX 0 3 BIND_QID QDMA Virtual Queue Group #0~3 to Physical Queue Binding 03020100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	VQTX_3_BIND_QID									VQTX_2_BIND_QID						
Type	RW									RW						
Reset		0	0	0	0	0	1	1		0	0	0	0	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VQTX_1_BIND_QID									VQTX_0_BIND_QID						
Type	RW									RW						
Reset		0	0	0	0	0	0	1		0	0	0	0	0	0	0

Bit(s)	Name	Description
30:24	VQTX_3_BIND_QID	The Physical Queue Number which binds with Virtual queue group #3
22:16	VQTX_2_BIND_QID	The Physical Queue Number which binds with Virtual queue group #2
14:8	VQTX_1_BIND_QID	The Physical Queue Number which binds with Virtual queue group #1
6:0	VQTX_0_BIND_QID	The Physical Queue Number which binds with Virtual queue group #0

151047C4 VQTX 4 7 BIND_QID QDMA Virtual Queue Group #4~7 to Physical Queue Binding 07060504

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	VQTX_7_BIND_QID									VQTX_6_BIND_QID						

Type		RW								RW						
Reset		0	0	0	0	1	1	1		0	0	0	0	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		VQTX_5_BIND_QID								VQTX_4_BIND_QID						
Type		RW								RW						
Reset		0	0	0	0	1	0	1		0	0	0	0	1	0	0

Bit(s)	Name	Description
30:24	VQTX_7_BIND_QID	The Physical Queue Number which binds with Virtual queue group #7
22:16	VQTX_6_BIND_QID	The Physical Queue Number which binds with Virtual queue group #6
14:8	VQTX_5_BIND_QID	The Physical Queue Number which binds with Virtual queue group #5
6:0	VQTX_4_BIND_QID	The Physical Queue Number which binds with Virtual queue group #4

151047E0 QTX_FC_SW_STS_0_15 TX Queue#0~15 Software Path Flow Control Status 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QTX_FC_SW_STS_0_15															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QTX_FC_SW_STS_0_15															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	QTX_FC_SW_STS_0_15	TX Queue Software Path Flow Control Status Each bit indicates the flow control decision on each physical queue's packet from software path. [0]: PQ#0 [15]: PQ#15

151047EC QDMA_ULTRA_CFG QDMA AXI ULTRA Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	AXI_ULTRA_EN					AXI_ULTRA_THRES										
Type	RW					RW										
Reset	0					0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AXI_PREULTRA_EN					AXI_PREULTRA_THRES										
Type	RW					RW										
Reset	0					0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	AXI_ULTRA_EN	Enable AXI Ultra transaction
26:16	AXI_ULTRA_THRES	AXI Ultra threshold. If CDM TX free FIFO count bigger than AXI_ULTRA_THRES, will trigger AXI Ultra transaction when AXI_ULTRA_EN = 1.
15	AXI_PREULTRA_EN	Enable AXI Pre-ultra transaction
10:0	AXI_PREULTRA_THRES	AXI Pre-ultra threshold. If CDM TX free FIFO count bigger than AXI_PREULTRA_THRES, will trigger AXI Pre-ultra transaction when AXI_PREULTRA_EN = 1.

151047F0 QDMA BUS CFG QDMA AXI BUS Configuration 00030400

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													CCI_EN	CCI_VQTB_EN	CCI_QRXFQ_EN	CCI_FQ_EN
Type													RW	RW	RW	RW
Reset													0	0	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						AXI_CTRL_UPDATED	AXI_RBUSY	AXI_WBUSY		AXI_LOCK_ERROR	AXI_ERMID_SET_RQ	AXI_ERMID_SET_BI_RQ	AXI_OUTSTANDING_EXTEND	AXI_QOS_ON		AXI_CG_DISABLE
Type						RO	RO	RO		RO	RO	RO	RW	RW		RW
Reset						1	0	0		0	0	0	0	0		0

Bit(s)	Name	Description
19	CCI_EN	QDMA CCI global control bit on BMU, QTX and QRX
18	CCI_VQTB_EN	BMU VQTB access the bus through CCI if CCI_EN=1
17	CCI_QRXFQ_EN	QRX FQ_DES access the bus through CCI if CCI_EN=1
16	CCI_FQ_EN	BMU FQ_DES access the bus through CCI if CCI_EN=1
10	AXI_CTRL_UPDATED	Master interface control signal updated status
9	AXI_R_BUSY	Read transaction not completes
8	AXI_W_BUSY	Write transaction not completes
6	AXI_LOCK_ERROR	Detects lock error
5	AXI_ERRMID_SET_RIRQ	Detects error MID from slave in R channel
4	AXI_ERRMID_SET_BIRQ	Detects error MID from slave in B channel
3	AXI_OUTSTANDING_EXTEND	Auto adds extra outstanding for QoS command
2	AXI_QOS_ON	Enable QoS function
0	AXI_CG_DISABLE	Disable auto clock gating of AXI component

151047F4 QDMA_RBUS_CFG QDMA RBUS Configuration 00000002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										R2X_DBG_SEL					R2X_INT_B	R2X_INT_EN
Type										RW					RO	RW
Reset									0	0	0	0			1	0

Bit(s)	Name	Description
7:4	R2X_DBG_SEL	Select debug information from R2X
1	R2X_INT_B	R2X interrupt status R2X wrapper interrupt will set 1'b1 when receive len = 0 cmd from rbus master.
0	R2X_INT_EN	R2X Interrupt Enable Enable R2X wrapper interrupt when receive len = 0 cmd from rbus master.

151047F8 QDMA_RBUS_STAT_0 R2X Status Register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	R2X_INT_STATUS															
Type	RO															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	R2X_INT_STATUS															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	R2X_INT_STATUS	Record the address when receive len = 0 cmd from R2X selected channel according to QDMA_RBUS_CFG[7:4]

151047FC QDMA RBUS STAT 1 R2X Status Register 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	R2X_DBG_INFO															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	R2X_DBG_INFO															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	R2X_DBG_INFO	Record debug information from R2X selected channel according to QDMA_RBUS_CFG[7:4]

15104800 WDMA0 TX BASE PTR 0 TX Ring #0 Base Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_BASE_PTR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_BASE_PTR															

Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_BASE_PTR	Point to the base address of TX Ring #0 (4-DW aligned address)

15104804 **WDMA0 TX MAX CNT 0** TX Ring #0 Maximum Count 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_MAX_CNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TX_MAX_CNT	The maximum number of TXD count in TX Ring #0

15104808 **WDMA0 TX CTX IDX 0** TX Ring #0 CPU pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_CTX_IDX															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TX_CTX_IDX	Point to the next TXD CPU wants to use

Bit(s)	Name	Description

1510480C WDMA0 TX DTX_IDX_0 TX Ring #0 DMA pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DTX_IDX															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TX_DTX_IDX	Point to the next TXD DMA wants to use

15104810 WDMA0 TX BASE_PTR_1 TX Ring #1 Base Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_BASE_PTR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_BASE_PTR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_BASE_PTR	Point to the base address of TX Ring #1 (4-DW aligned address)

15104814 WDMA0 TX MAX_CNT_1 TX Ring #1 Maximum Count 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_MAX_CNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TX_MAX_CNT	The maximum number of TXD count in TX Ring #1

15104818 **WDMA0 TX CTX_IDX_1** TX Ring #1 CPU pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_CTX_IDX															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TX_CTX_IDX	Point to the next TXD CPU wants to use

1510481C **WDMA0 TX DTX_IDX_1** TX Ring #1 DMA pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	TX_DTX_IDX															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TX_DTX_IDX	Point to the next TXD DMA wants to use

15104820 WDMA0_TX_BASE_PTR_2 TX Ring #2 Base Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_BASE_PTR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_BASE_PTR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_BASE_PTR	Point to the base address of TX Ring #2 (4-DW aligned address)

15104824 WDMA0_TX_MAX_CNT_2 TX Ring #2 Maximum Count 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_MAX_CNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TX_MAX_CNT	The maximum number of TXD count in TX Ring #2

15104828 WDMA0 TX CTX_IDX 2 TX Ring #2 CPU pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_CTX_IDX															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TX_CTX_IDX	Point to the next TXD CPU wants to use

1510482C WDMA0 TX DTX_IDX 2 TX Ring #2 DMA pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DTX_IDX															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TX_DTX_IDX	Point to the next TXD DMA wants to use

15104830 WDMA0 TX BASE_PTR 3 TX Ring #3 Base Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_BASE_PTR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_BASE_PTR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_BASE_PTR	Point to the base address of TX Ring #3 (4-DW aligned address)

15104834 **WDMA0_TX_MAX_CNT_3** TX Ring #3 Maximum Count **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_MAX_CNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TX_MAX_CNT	The maximum number of TXD count in TX Ring #3

15104838 **WDMA0_TX_CTX_IDX_3** TX Ring #3 CPU pointer **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_CTX_IDX															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TX_CTX_IDX	Point to the next TXD CPU wants to use

1510483C WDMA0_TX_DTX_IDX_3 TX Ring #3 DMA pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DTX_IDX															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TX_DTX_IDX	Point to the next TXD DMA wants to use

15104900 WDMA0_RX_BASE_PTR_0 RX Ring #0 Base Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_BASE_PTR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_BASE_PTR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_BASE_PTR	Point to the base address of RX Ring #0 (4-DW aligned address)

15104904 WDMA0_RX_MAX_CNT_0 RX Ring #0 Maximum Count 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_MAX_CNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RX_MAX_CNT	The maximum number of RXD count in RX Ring #0

15104908 WDMA0_RX_CRX_IDX_0 RX Ring #0 CPU pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_CRX_IDX															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RX_CRX_IDX	Point to the next RXD CPU wants to use

1510490C WDMA0_RX_DRX_IDX_0 RX Ring #0 DMA pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_DRX_IDX															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RX_DRX_IDX	Point to the next RXD DMA wants to use

15104910 **WDMA0 RX BASE PTR 1** **RX Ring #1 Base Pointer** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_BASE_PTR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_BASE_PTR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_BASE_PTR	Point to the base address of RX Ring #1 (4-DW aligned address)

15104914 **WDMA0 RX MAX CNT 1** **RX Ring #1 Maximum Count** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_MAX_CNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RX_MAX_CNT	The maximum number of RXD count in RX Ring #1

15104918 WDMA0_RX_CRX_IDX_1 RX Ring #1 CPU pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_CRX_IDX															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RX_CRX_IDX	Point to the next RXD CPU wants to use

1510491C WDMA0_RX_DRX_IDX_1 RX Ring #1 DMA pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_DRX_IDX															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RX_DRX_IDX	Point to the next RXD DMA wants to use

15104A00 WDMA0_INFO WDMA Information 40000204

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					INDEX_WIDTH				BASE_PTR_WIDTH							
Type					RO				RO							
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_RING_NUM								TX_RING_NUM							
Type	RO								RO							
Reset	0	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0

Bit(s)	Name	Description
27:24	INDEX_WIDTH	Ring index width 0 means 16bits, 1~15 means 1~15bits
23:16	BASE_PTR_WIDTH	Base pointer width, x Base_addr[31:32-x] is shared with all ring base address. Only ring #0 base address[31:32-x] field is writable. [note]: "0" means no bit of base_address is shared.
15:8	RX_RING_NUM	RX ring number
7:0	TX_RING_NUM	TX ring number

15104A04 WDMA0_GLO_CFG WDMA Global Configuration 50404E70

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_2B_OFFSET	CSR_CLK_GATE_BY	BYTE_SWAP	DEC_WCOMP	PKT_WCOMP	BYTE_SWAP_BIT_SEL	BIG_ENDIAN_BIT_SEL									
Type	RW	RW	RW	RW	RW	RW	RW									
Reset	0	1	0	1	0	0	0									
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MULTI_CNT				MULTI_EN	RX_CH_K_DDO_NE	TX_CH_K_DDO_NE		BIG_ENDIAN	TX_WB_DDO_NE	WDMA_BT_SIZE	RX_DMA_BUS_Y	RX_DMA_A_EN	TX_DMA_A_BUS_Y	TX_DMA_A_EN	

Type	RW				RW	RW	RW		RW	RW	RW		RO	RW	RO	RW
Reset	0	1	0	0	1	1	1		0	1	1	1	0	0	0	0

Bit(s)	Name	Description
31	RX_2B_OFFSET	Prepend 2-Byte to RX-buffer (packet) for aligning IP header to 32-bit boundary. Default MAC header is 14-Byte
30	CSR_CLKGATE_BYP	Clock gated Bypass
29	BYTE_SWAP	Byte Swap
28	DEC_WCOMP	DMA check WDONE or WCOMPLETE when update descriptor into DRAM
27	PKT_WCOMP	RX_DMA check WDONE or WCOMPLETE when write packet into DRAM
26	BYTE_SWAP_BIT_SEL	Bit selection for byte swap function
25	BIG_ENDIAN_BIT_SEL	Bit selection for endian control
15:12	MUTLI_CNT	Number of TX DMA read outstanding transactions when WDMA0_GLO_CFG[11] = 1'b1.
11	MULTI_EN	Enable TX DAM AXI read outstanding transaction
10	RX_CHK_DDONE	Enable RX_DMA check DDONE, if DDONE=1, DMA will into Coherence protection
9	TX_CHK_DDONE	Enable TX_DMA check DDONE, if DDONE=1, DMA will into Coherence protection
7	BIG_ENDIAN	Big endian
6	TX_WB_DDONE	
5:4	WDMA_BT_SIZE	The burst size of WDMA
3	RX_DMA_BUSY	
2	RX_DMA_EN	
1	TX_DMA_BUSY	
0	TX_DMA_EN	

15104A08		WDMA0_RST_IDX				WDMA Reset Index											00000000
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
Name																	RST_D RX_IDX 0
Type																	WO
Reset																	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Name																	RST_DT TX_IDX1 0
Type																	WO
Reset																	0

Bit(s)	Name	Description
16	RST_DRX_IDX0	Write 1 to reset RX_DMA RX_IDX0 to 0
1	RST_DTX_IDX1	Write 1 to reset TX_DMA TX_IDX1 to 0
0	RST_DTX_IDX0	Write 1 to reset TX_DMA TX_IDX0 to 0

15104A10 **WDMA0 FREEQ_THRES** **WDMA Free Queue Threshold** **00000002**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													FREEQ_THRES			
Type													RW			
Reset													0	0	1	0

Bit(s)	Name	Description
3:0	FREEQ_THRES	RX free queue threshold WDMA will stop DMA interface when left RX descriptors reach this threshold

15104A20 **WDMA0 INT STATUS** **WDMA Interrupt Status** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_CO HEREN T	RX_DLY _INT	TX_CO HEREN T	TX_DLY _INT							RX_DO NE_DL Y_INT1	RX_DO NE_DL Y_INT0			RX_DO NE_INT 1	RX_DO NE_INT 0
Type	W1C	W1C	W1C	W1C							W1C	W1C			W1C	W1C
Reset	0	0	0	0							0	0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					TX_DO NE_DL Y_INT3	TX_DO NE_DL Y_INT2	TX_DO NE_DL Y_INT1	TX_DO NE_DL Y_INT0								TX_DO NE_INT 0
Type					W1C	W1C	W1C	W1C								W1C
Reset					0	0	0	0								0

Bit(s)	Name	Description
31	RX_COHERENT	RX_DMA finds data coherent event while checking DDONE bit.
30	RX_DLY_INT	Summary of the whole WDMA RX related interrupts.
29	TX_COHERENT	TX_DMA finds data coherent event while checking DDONE bit.
28	TX_DLY_INT	Summary of the whole WDMA TX related interrupts.
21	RX_DONE_DLY_INT1	RX ring #1 packet receive delay interrupt
20	RX_DONE_DLY_INT0	RX ring #0 packet receive delay interrupt
17	RX_DONE_INT1	RX ring #1 packet receive interrupt
16	RX_DONE_INT0	RX ring #0 packet receive interrupt
11	TX_DONE_DLY_INT3	TX ring #3 packet transmit delay interrupt
10	TX_DONE_DLY_INT2	TX ring #2 packet transmit delay interrupt
9	TX_DONE_DLY_INT1	TX ring #1 packet transmit delay interrupt
8	TX_DONE_DLY_INT0	TX ring #0 packet transmit delay interrupt
0	TX_DONE_INT0	TX ring #0 packet transmit interrupt

15104A28 WDMA0_INT_MASK WDMA Interrupt Mask 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_COHERENT	RX_DLY_INT	TX_COHERENT	TX_DLY_INT							RX_DONE_INT1	RX_DONE_INT0			RX_DONE_INT1	RX_DONE_INT0
Type	RW	RW	RW	RW							RW	RW			RW	RW
Reset	0	0	0	0							0	0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								TX_DONE_INT0								TX_DONE_INT0
Type								RW								RW
Reset								0								0

Bit(s)	Name	Description
31	RX_COHERENT	Interrupt enable for RX_DMA data coherent event
30	RX_DLY_INT	Summary of the whole WDMA RX related interrupts.
29	TX_COHERENT	Interrupt enable for TX_DMA data coherent event
28	TX_DLY_INT	Summary of the whole WDMA TX related interrupts.
21	RX_DONE_DLY_INT1	RX ring #1 packet receive delay interrupt
20	RX_DONE_DLY_INT0	RX ring #0 packet receive delay interrupt
17	RX_DONE_INT1	RX ring #1 packet receive interrupt
16	RX_DONE_INT0	RX ring #0 packet receive interrupt
8	TX_DONE_DLY_INT0	TX ring #0 packet transmit delay interrupt
0	TX_DONE_INT0	TX ring #0 packet transmit interrupt

15104A30 WDMA0_TX_DBG_MONO WDMA TX Debug Monitor 0

00000090

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

15104A34 **WDMA0_TX_DBG_MON1** **WDMA TX Debug Monitor 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

15104A38 **WDMA0_RX_DBG_MON0** **WDMA RX Debug Monitor 0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

15104A3C **WDMA0_RX_DBG_MON1** **WDMA RX Debug Monitor 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

15104A40 **WDMA0_INT_STS_GRP0** **WDMA Interrupt Status Group 0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WDMA_INT_STS_GRP0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WDMA_INT_STS_GRP0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	WDMA_INT_STS_GRP0	Interrupt group 0 status, this information already "and" with " ~WDMA_INT_GRP1 & ~WDMA_INT_GRP2" Each bit definition is same as "WDMA_INT_STATUS"

15104A44 WDMA0 INT_STS_GRP1 WDMA Interrupt Status Group 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WDMA_INT_STS_GRP1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WDMA_INT_STS_GRP1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	WDMA_INT_STS_GRP1	Interrupt group 1 status, this information already "and" with " "WDMA_INT_GRP1" Each bit definition is same as "WDMA_INT_STATUS"

15104A48 WDMA0 INT_STS_GRP2 WDMA Interrupt Status Group 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WDMA_INT_STS_GRP2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WDMA_INT_STS_GRP2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	WDMA_INT_STS_GRP2	Interrupt group 2 status, this information already "and" with " "WDMA_INT_GRP2" Each bit definition is same as "WDMA_INT_STATUS"

Bit(s)	Name	Description

15104A4C **WDMA0_INT_STS_GRP3** **WDMA Interrupt Status Group 3** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WDMA_INT_STS_GRP3															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WDMA_INT_STS_GRP3															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	WDMA_INT_STS_GRP3	Interrupt group 3 status, this information already "and" with "WDMA_INT_GRP3" Each bit definition is same as "WDMA_INT_STATUS"

15104A50 **WDMA0_INT_GRP1** **WDMA Interrupt Group 1 Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WDMA_INT_GRP1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WDMA_INT_GRP1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	WDMA_INT_GRP1	Interrupt group 1 assignment. Each bit's definition is same as "WDMA_INT_STATUS"

15104A54 **WDMA0_INT_GRP2** **WDMA Interrupt Group 2 Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WDMA_INT_GRP2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WDMA_INT_GRP2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	WDMA_INT_GRP2	Interrupt group 2 assignment. Each bit's definition is same as "WDMA_INT_STATUS"

15104A58 **WDMA0_INT_GRP3** **WDMA Interrupt Group 3 Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WDMA_INT_GRP3															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WDMA_INT_GRP3															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	WDMA_INT_GRP3	Interrupt group 3 assignment. Each bit's definition is same as "WDMA_INT_STATUS"

15104A60 **WDMA0_BUS_CFG** **WDMA AXI BUS Configuration** **00000400**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																

Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						AXI_CTRL_UPDATED	AXI_R_BUSY	AXI_W_BUSY		AXI_LOCK_ERROR	AXI_ERRMID_SET_RIRQ	AXI_ERRMID_SET_BIRQ	AXI_OUTSTANDING_EXTEND	AXI_QOS_ON		AXI_CG_DISABLE
Type						RO	RO	RO		RO	RO	RO	RW	RW		RW
Reset						1	0	0		0	0	0	0	0		0

Bit(s)	Name	Description
10	AXI_CTRL_UPDATED	Master interface control signal updated status
9	AXI_R_BUSY	Read transaction not completes
8	AXI_W_BUSY	Write transaction not completes
6	AXI_LOCK_ERROR	Detects lock error
5	AXI_ERRMID_SET_RIRQ	Detects error MID from slave in R channel
4	AXI_ERRMID_SET_BIRQ	Detects error MID from slave in B channel
3	AXI_OUTSTANDING_EXTEND	Auto adds extra outstanding for QoS command
2	AXI_QOS_ON	Enable QoS function
0	AXI_CG_DISABLE	Disable auto clock gating of AXI component

15104A64 WDMA0 ULTRA CFG WDMA AXI ULTRA Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AXI_ULTRA_EN					AXI_ULTRA_THRES										
Type	RW					RW										
Reset	0					0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AXI_PREULTRA_EN					AXI_PREULTRA_THRES										
Type	RW					RW										
Reset	0					0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	AXI_ULTRA_EN	Enable AXI Ultra transaction
26:16	AXI_ULTRA_THRES	AXI Ultra threshold.

Bit(s)	Name	Description
15	AXI_PREULTRA_EN	If CDM TX free FIFO count bigger than AXI_ULTRA_THRES, will trigger AXI Ultra transaction when AXI_ULTRA_EN = 1.
10:0	AXI_PREULTRA_THRES	Enable AXI Pre-ultra transaction AXI Pre-ultra threshold. If CDM TX free FIFO count bigger than AXI_PREULTRA_THRES, will trigger AXI Pre-ultra transaction when AXI_PREULTRA_EN = 1.

15104A68 **WDMA0_PREF_CFG** **WDMA Prefetch Configuration** 00000040

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											PREF_C NT				PREF_B USY	PREF_E N
Type											RW				RO	RW
Reset											0				0	0

Bit(s)	Name	Description
5	PREF_CNT	Maximum Prefetch Count
1	PREF_BUSY	Prefetch Busy
0	PREF_EN	Prefetch Enable

15104A70 **WDMA0_SDL_CFG** **WDMA SDL Configuration** 00000800

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																SDL_E N
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SDL															
Type	RW															
Reset	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	SDL_EN	Enable RX_DMA read SDL from CR
15:0	SDL	RX_DMA read SDL value

15104A74 **WDMA0_IDLE_MASK** **WDMA IDLE MASK** **00000030**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											DMA_IDLE	AXI_IDLE		IDLE_MASK		
Type											RO	RO		RW		
Reset											1	1		0	0	0

Bit(s)	Name	Description
5	DMA_IDLE	DMA idle status
4	AXI_IDLE	AXM idle status
2:0	IDLE_MASK	Idle signal mask

15104A80 **WDMA0_SCH_Q01_CFG** **WDMA Scheduler Configuration for Q0&Q1** **5C004C00**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_BKT_SIZE1	MAX_RATE_ULMT1	MAX_WEIGHT1		MIN_RATE_RATIO1		MAX_RATE1									
Type	RW	RW	RW		RW		RW									
Reset	0	1	0	1	1	1	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_BKT_SIZE0	MAX_RATE_ULMT0	MAX_WEIGHT0		MIN_RATE_RATIO0		MAX_RATE0									
Type	RW	RW	RW		RW		RW									
Reset	0	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MAX_BKT_SIZE1	Maximum bucket size
30	MAX_RATE_ULMT1	Maximum rate limitation
29:28	MAX_WEIGHT1	Define the auto-reload bucket size if MAX_RATE_ULMT is set to 1. It is also served as excess bandwidth allocation ratio for servicing queue
27:26	MIN_RATE_RATIO1	Define the guaranteed Min rate based on MAX_RATE
25:16	MAX_RATE1	Define the limited Max rate for queue if MAX_RATE_ULMT is 0. The value specified represents the amount of 4-byte quota to be added into the queue #1 bucket per 125us. For example: If 512 is programmed, then the max rate limited is : $512 * 4 \text{ bytes}/125\text{us} = 16.384\text{M bytes/sec}$ or 131Mbps
15	MAX_BKT_SIZE0	Maximum bucket size
14	MAX_RATE_ULMT0	Maximum rate limitation
13:12	MAX_WEIGHT0	Define the auto-reload bucket size if MAX_RATE_ULMT is set to 1. It is also served as excess bandwidth allocation ratio for servicing queue
11:10	MIN_RATE_RATIO0	Define the guaranteed Min rate based on MAX_RATE
9:0	MAX_RATE0	Define the limited Max rate for queue if MAX_RATE_ULMT is 0. The value specified represents the amount of 4-byte quota to be added into the queue #1 bucket per 125us. For example: If 512 is programmed, then the max rate limited is : $512 * 4 \text{ bytes}/125\text{us} = 16.384\text{M bytes/sec}$ or 131Mbps

15104A84 WDMA0 SCH_Q23_CFG WDMA Scheduler Configuration for Q2&Q3 7C006C00

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_BKT_SIZE3	MAX_RATE_ULMT3	MAX_WEIGHT3		MIN_RATE_RATIO3		MAX_RATE3									
Type	RW	RW	RW		RW		RW									
Reset	0	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_BKT_SIZE2	MAX_RATE_ULMT2	MAX_WEIGHT2		MIN_RATE_RATIO2		MAX_RATE2									
Type	RW	RW	RW		RW		RW									
Reset	0	1	1	0	1	1	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MAX_BKT_SIZE3	Maximum bucket size
30	MAX_RATE_ULMT3	Maximum rate limitation
29:28	MAX_WEIGHT3	Define the auto-reload bucket size if MAX_RATE_ULMT is set to 1. It is also served as excess bandwidth allocation ratio for servicing queue
27:26	MIN_RATE_RATIO3	Define the guaranteed Min rate based on MAX_RATE
25:16	MAX_RATE3	Define the limited Max rate for queue if MAX_RATE_ULMT is 0. The value specified represents the amount of 4-byte quota to be added into the queue #1 bucket per 125us.

Bit(s)	Name	Description
15	MAX_BKT_SIZE2	For example: If 512 is programmed, then the max rate limited is : 512 * 4 bytes/125us = 16.384M bytes/sec or 131Mbps Maximum bucket size
14	MAX_RATE_ULMT2	Maximum rate limitation
13:12	MAX_WEIGHT2	Define the auto-reload bucket size if MAX_RATE_ULMT is set to 1. It is also served as excess bandwidth allocation ratio for servicing queue
11:10	MIN_RATE_RATIO2	Define the guaranteed Min rate based on MAX_RATE
9:0	MAX_RATE2	Define the limited Max rate for queue if MAX_RATE_ULMT is 0. The value specified represents the amount of 4-byte quota to be added into the queue #1 bucket per 125us. For example: If 512 is programmed, then the max rate limited is : 512 * 4 bytes/125us = 16.384M bytes/sec or 131Mbps

15104A90 WDMA0 INT STATUS 0 WDMA Interrupt Status 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_COHERENT	RX_DLY_INT	TX_COHERENT	TX_DLY_INT							RX_DONE_DLY_INT1	RX_DONE_DLY_INT0			RX_DONE_INT1	RX_DONE_INT0
Type	W1C	W1C	W1C	W1C							W1C	W1C			W1C	W1C
Reset	0	0	0	0							0	0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					TX_DONE_DLY_INT3	TX_DONE_DLY_INT2	TX_DONE_DLY_INT1	TX_DONE_DLY_INT0								TX_DONE_INT0
Type					W1C	W1C	W1C	W1C								W1C
Reset					0	0	0	0								0

Bit(s)	Name	Description
31	RX_COHERENT	RX_DMA finds data coherent event while checking DDONE bit.
30	RX_DLY_INT	Summary of the whole WDMA RX related interrupts.
29	TX_COHERENT	TX_DMA finds data coherent event while checking DDONE bit.
28	TX_DLY_INT	Summary of the whole WDMA TX related interrupts.
21	RX_DONE_DLY_INT1	RX ring #1 packet receive delay interrupt
20	RX_DONE_DLY_INT0	RX ring #0 packet receive delay interrupt
17	RX_DONE_INT1	RX ring #1 packet receive interrupt
16	RX_DONE_INT0	RX ring #0 packet receive interrupt
11	TX_DONE_DLY_INT3	TX ring #3 packet transmit delay interrupt
10	TX_DONE_DLY_INT2	TX ring #2 packet transmit delay interrupt
9	TX_DONE_DLY_INT1	TX ring #1 packet transmit delay interrupt
8	TX_DONE_DLY_INT0	TX ring #0 packet transmit delay interrupt
0	TX_DONE_INT0	TX ring #0 packet transmit interrupt

15104A94 **WDMA0_INT_MASK_0** WDMA Interrupt Mask 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_COHERENT	RX_DLY_INT	TX_COHERENT	TX_DLY_INT							RX_DONE_DLY_INT1	RX_DONE_DLY_INT0			RX_DONE_INT1	RX_DONE_INT0
Type	RW	RW	RW	RW							RW	RW			RW	RW
Reset	0	0	0	0							0	0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								TX_DONE_DLY_INT0								TX_DONE_INT0
Type								RW								RW
Reset								0								0

Bit(s)	Name	Description
31	RX_COHERENT	Interrupt enable for RX_DMA data coherent event
30	RX_DLY_INT	Summary of the whole WDMA RX related interrupts.
29	TX_COHERENT	Interrupt enable for TX_DMA data coherent event
28	TX_DLY_INT	Summary of the whole WDMA TX related interrupts.
21	RX_DONE_DLY_INT1	RX ring #1 packet receive delay interrupt
20	RX_DONE_DLY_INT0	RX ring #0 packet receive delay interrupt
17	RX_DONE_INT1	RX ring #1 packet receive interrupt
16	RX_DONE_INT0	RX ring #0 packet receive interrupt
8	TX_DONE_DLY_INT0	TX ring #0 packet transmit delay interrupt
0	TX_DONE_INT0	TX ring #0 packet transmit interrupt

15104A98 **WDMA0_INT_STATUS_1** WDMA Interrupt Status 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_COHERENT	RX_DLY_INT	TX_COHERENT	TX_DLY_INT							RX_DONE_DLY_INT1	RX_DONE_DLY_INT0			RX_DONE_INT1	RX_DONE_INT0
Type	W1C	W1C	W1C	W1C							W1C	W1C			W1C	W1C
Reset	0	0	0	0							0	0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					TX_DONE_DLY_INT3	TX_DONE_DLY_INT2	TX_DONE_DLY_INT1	TX_DONE_DLY_INT0								TX_DONE_INT0
Type					W1C	W1C	W1C	W1C								W1C

Reset					0	0	0	0								0

Bit(s)	Name	Description
31	RX_COHERENT	RX_DMA finds data coherent event while checking DDONE bit.
30	RX_DLY_INT	Summary of the whole WDMA RX related interrupts.
29	TX_COHERENT	TX_DMA finds data coherent event while checking DDONE bit.
28	TX_DLY_INT	Summary of the whole WDMA TX related interrupts.
21	RX_DONE_DLY_INT1	RX ring #1 packet receive delay interrupt
20	RX_DONE_DLY_INT0	RX ring #0 packet receive delay interrupt
17	RX_DONE_INT1	RX ring #1 packet receive interrupt
16	RX_DONE_INT0	RX ring #0 packet receive interrupt
11	TX_DONE_DLY_INT3	TX ring #3 packet transmit delay interrupt
10	TX_DONE_DLY_INT2	TX ring #2 packet transmit delay interrupt
9	TX_DONE_DLY_INT1	TX ring #1 packet transmit delay interrupt
8	TX_DONE_DLY_INT0	TX ring #0 packet transmit delay interrupt
0	TX_DONE_INT0	TX ring #0 packet transmit interrupt

15104A9C WDMA0 INT MASK 1 WDMA Interrupt Mask 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_COHERENT	RX_DLY_INT	TX_COHERENT	TX_DLY_INT							RX_DONE_DLY_INT1	RX_DONE_DLY_INT0			RX_DONE_INT1	RX_DONE_INT0
Type	RW	RW	RW	RW							RW	RW			RW	RW
Reset	0	0	0	0							0	0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								TX_DONE_DLY_INT0								TX_DONE_INT0
Type								RW								RW
Reset								0								0

Bit(s)	Name	Description
31	RX_COHERENT	Interrupt enable for RX_DMA data coherent event
30	RX_DLY_INT	Summary of the whole WDMA RX related interrupts.
29	TX_COHERENT	Interrupt enable for TX_DMA data coherent event
28	TX_DLY_INT	Summary of the whole WDMA TX related interrupts.
21	RX_DONE_DLY_INT1	RX ring #1 packet receive delay interrupt
20	RX_DONE_DLY_INT0	RX ring #0 packet receive delay interrupt
17	RX_DONE_INT1	RX ring #1 packet receive interrupt
16	RX_DONE_INT0	RX ring #0 packet receive interrupt
8	TX_DONE_DLY_INT0	TX ring #0 packet transmit delay interrupt
0	TX_DONE_INT0	TX ring #0 packet transmit interrupt

Bit(s)	Name	Description

15104AA0 WDMA0 INT STATUS 2 WDMA Interrupt Status 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_COHERENT	RX_DLY_INT	TX_COHERENT	TX_DLY_INT							RX_DONE_DL_Y_INT1	RX_DONE_DL_Y_INT0			RX_DONE_INT1	RX_DONE_INT0
Type	W1C	W1C	W1C	W1C							W1C	W1C			W1C	W1C
Reset	0	0	0	0							0	0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					TX_DONE_DL_Y_INT3	TX_DONE_DL_Y_INT2	TX_DONE_DL_Y_INT1	TX_DONE_DL_Y_INT0								TX_DONE_INT0
Type					W1C	W1C	W1C	W1C								W1C
Reset					0	0	0	0								0

Bit(s)	Name	Description
31	RX_COHERENT	RX_DMA finds data coherent event while checking DDONE bit.
30	RX_DLY_INT	Summary of the whole WDMA RX related interrupts.
29	TX_COHERENT	TX_DMA finds data coherent event while checking DDONE bit.
28	TX_DLY_INT	Summary of the whole WDMA TX related interrupts.
21	RX_DONE_DL_Y_INT1	RX ring #1 packet receive delay interrupt
20	RX_DONE_DL_Y_INT0	RX ring #0 packet receive delay interrupt
17	RX_DONE_INT1	RX ring #1 packet receive interrupt
16	RX_DONE_INT0	RX ring #0 packet receive interrupt
11	TX_DONE_DL_Y_INT3	TX ring #3 packet transmit delay interrupt
10	TX_DONE_DL_Y_INT2	TX ring #2 packet transmit delay interrupt
9	TX_DONE_DL_Y_INT1	TX ring #1 packet transmit delay interrupt
8	TX_DONE_DL_Y_INT0	TX ring #0 packet transmit delay interrupt
0	TX_DONE_INT0	TX ring #0 packet transmit interrupt

15104AA4 WDMA0 INT MASK 2 WDMA Interrupt Mask 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_COHERENT	RX_DLY_INT	TX_COHERENT	TX_DLY_INT							RX_DONE_DL_Y_INT1	RX_DONE_DL_Y_INT0			RX_DONE_INT1	RX_DONE_INT0
Type	RW	RW	RW	RW							RW	RW			RW	RW
Reset	0	0	0	0							0	0			0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								TX_DONE_DL Y_INT0								TX_DONE_INT 0
Type								RW								RW
Reset								0								0

Bit(s)	Name	Description
31	RX_COHERENT	Interrupt enable for RX_DMA data coherent event
30	RX_DLY_INT	Summary of the whole WDMA RX related interrupts.
29	TX_COHERENT	Interrupt enable for TX_DMA data coherent event
28	TX_DLY_INT	Summary of the whole WDMA TX related interrupts.
21	RX_DONE_DLY_INT1	RX ring #1 packet receive delay interrupt
20	RX_DONE_DLY_INT0	RX ring #0 packet receive delay interrupt
17	RX_DONE_INT1	RX ring #1 packet receive interrupt
16	RX_DONE_INT0	RX ring #0 packet receive interrupt
8	TX_DONE_DLY_INT0	TX ring #0 packet transmit delay interrupt
0	TX_DONE_INT0	TX ring #0 packet transmit interrupt

15104AA8 WDMA0_INT_STATUS_3 WDMA Interrupt Status 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_COHERENT	RX_DLY_INT	TX_COHERENT	TX_DLY_INT							RX_DONE_DL Y_INT1	RX_DONE_DL Y_INT0			RX_DONE_INT 1	RX_DONE_INT 0
Type	W1C	W1C	W1C	W1C							W1C	W1C			W1C	W1C
Reset	0	0	0	0							0	0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					TX_DONE_DL Y_INT3	TX_DONE_DL Y_INT2	TX_DONE_DL Y_INT1	TX_DONE_DL Y_INT0								TX_DONE_INT 0
Type					W1C	W1C	W1C	W1C								W1C
Reset					0	0	0	0								0

Bit(s)	Name	Description
31	RX_COHERENT	RX_DMA finds data coherent event while checking DDONE bit.
30	RX_DLY_INT	Summary of the whole WDMA RX related interrupts.
29	TX_COHERENT	TX_DMA finds data coherent event while checking DDONE bit.
28	TX_DLY_INT	Summary of the whole WDMA TX related interrupts.
21	RX_DONE_DLY_INT1	RX ring #1 packet receive delay interrupt
20	RX_DONE_DLY_INT0	RX ring #0 packet receive delay interrupt

Bit(s)	Name	Description
17	RX_DONE_INT1	RX ring #1 packet receive interrupt
16	RX_DONE_INT0	RX ring #0 packet receive interrupt
11	TX_DONE_DLY_INT3	TX ring #3 packet transmit delay interrupt
10	TX_DONE_DLY_INT2	TX ring #2 packet transmit delay interrupt
9	TX_DONE_DLY_INT1	TX ring #1 packet transmit delay interrupt
8	TX_DONE_DLY_INT0	TX ring #0 packet transmit delay interrupt
0	TX_DONE_INT0	TX ring #0 packet transmit interrupt

15104AAC **WDMA0_INT_MASK_3** WDMA Interrupt Mask 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_COHERENT	RX_DLY_INT	TX_COHERENT	TX_DLY_INT							RX_DONE_DLY_INT1	RX_DONE_DLY_INT0			RX_DONE_INT1	RX_DONE_INT0
Type	RW	RW	RW	RW							RW	RW			RW	RW
Reset	0	0	0	0							0	0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								TX_DONE_DLY_INT0								TX_DONE_INT0
Type								RW								RW
Reset								0								0

Bit(s)	Name	Description
31	RX_COHERENT	Interrupt enable for RX_DMA data coherent event
30	RX_DLY_INT	Summary of the whole WDMA RX related interrupts.
29	TX_COHERENT	Interrupt enable for TX_DMA data coherent event
28	TX_DLY_INT	Summary of the whole WDMA TX related interrupts.
21	RX_DONE_DLY_INT1	RX ring #1 packet receive delay interrupt
20	RX_DONE_DLY_INT0	RX ring #0 packet receive delay interrupt
17	RX_DONE_INT1	RX ring #1 packet receive interrupt
16	RX_DONE_INT0	RX ring #0 packet receive interrupt
8	TX_DONE_DLY_INT0	TX ring #0 packet transmit delay interrupt
0	TX_DONE_INT0	TX ring #0 packet transmit interrupt

15104AB0 **WDMA0_TX_DELAY_INT_CFG** WDMA Tx Delay Interrupt Configuration 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																

Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RING0_TXDLY_INT_EN	RING0_TXMAX_PINT							RING0_TXMAX_PTIME							
Type	RW	RW							RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	RING0_TXDLY_INT_EN	Enable delay interrupt mechanism for Tx Ring 0
14:8	RING0_TXMAX_PINT	Specified Max. number of pended interrupts [Note] reset to 0 can disable pending interrupt count check.
7:0	RING0_TXMAX_PTIME	Specified Max. pended time [Note] reset to 0 can disable pending interrupt time check.

15104AB4 WDMA0_TX_DELAY_INT_CFG WDMA Tx Delay Interrupt Configuration 1

00000000

1

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

15104AC0 WDMA0_RX_DELAY_INT_CFG WDMA Rx Delay Interrupt Configuration 0

00000000

0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RING1_RXDLY	RING1_RXMAX_PINT							RING1_RXMAX_PTIME							

	_INT_EN															
Type	RW	RW							RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RING0_RXDLY_INT_EN	RING0_RXMAX_PINT							RING0_RXMAX_PTIME							
Type	RW	RW							RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	RING1_RXDLY_INT_EN	Enable delay interrupt mechanism for Rx Ring 1
30:24	RING1_RXMAX_PINT	Specified Max. number of pended interrupts [Note] reset to 0 can disable pending interrupt count check.
23:16	RING1_RXMAX_PTIME	Specified Max. pended time [Note] reset to 0 can disable pending interrupt time check.
15	RING0_RXDLY_INT_EN	Enable delay interrupt mechanism for Rx Ring 0
14:8	RING0_RXMAX_PINT	Specified Max. number of pended interrupts [Note] reset to 0 can disable pending interrupt count check.
7:0	RING0_RXMAX_PTIME	Specified Max. pended time [Note] reset to 0 can disable pending interrupt time check.

15104AC8 WDMA0_RX_FC_CFG_0 WDMA Rx Flow Control Configuration 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					RING0_FC_DASRT_THRES											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RING0_FC_ASRT_THRES											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
27:16	RING0_FC_DASRT_THRES	Specified PFC deassert threshold. Disable PFC when free DMAD count > threshold.

Bit(s)	Name	Description
11:0	RING0_FC_ASRT_THRES	Specified PFC assert threshold. Enable PFC when free DMAD count < threshold. Threshold = 0 means PFC disabled

15104ACC WDMA0_RX_FC_CFG_1 WDMA Rx Flow Control Configuration 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					RING1_FC_DASRT_THRES											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RING1_FC_ASRT_THRES											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
27:16	RING1_FC_DASRT_THRES	Specified PFC deassert threshold. Disable PFC when free DMAD count > threshold.
11:0	RING1_FC_ASRT_THRES	Specified PFC assert threshold. Enable PFC when free DMAD count < threshold. Threshold = 0 means PFC disabled.

15104C00 WDMA1_TX_BASE_PTR_0 TX Ring #0 Base Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_BASE_PTR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_BASE_PTR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_BASE_PTR	Point to the base address of TX Ring #0 (4-DW aligned address)

Bit(s)	Name	Description

15104C04 WDMA1_TX_MAX_CNT_0 TX Ring #0 Maximum Count 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_MAX_CNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TX_MAX_CNT	The maximum number of TXD count in TX Ring #0

15104C08 WDMA1_TX_CTX_IDX_0 TX Ring #0 CPU pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_CTX_IDX															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TX_CTX_IDX	Point to the next TXD CPU wants to use

15104C0C WDMA1_TX_DTX_IDX_0 TX Ring #0 DMA pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DTX_IDX															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TX_DTX_IDX	Point to the next TXD DMA wants to use

15104C10 WDMA1 TX BASE PTR 1 TX Ring #1 Base Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_BASE_PTR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_BASE_PTR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_BASE_PTR	Point to the base address of TX Ring #1 (4-DW aligned address)

15104C14 WDMA1 TX MAX CNT 1 TX Ring #1 Maximum Count 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	TX_MAX_CNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TX_MAX_CNT	The maximum number of TXD count in TX Ring #1

15104C18 WDMA1 TX CTX_IDX_1 TX Ring #1 CPU pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_CTX_IDX															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TX_CTX_IDX	Point to the next TXD CPU wants to use

15104C1C WDMA1 TX DTX_IDX_1 TX Ring #1 DMA pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DTX_IDX															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TX_DTX_IDX	Point to the next TXD DMA wants to use

15104C20 **WDMA1 TX BASE PTR 2** TX Ring #2 Base Pointer **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_BASE_PTR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_BASE_PTR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_BASE_PTR	Point to the base address of TX Ring #2 (4-DW aligned address)

15104C24 **WDMA1 TX MAX CNT 2** TX Ring #2 Maximum Count **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_MAX_CNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TX_MAX_CNT	The maximum number of TXD count in TX Ring #2

15104C28 **WDMA1 TX CTX IDX 2** TX Ring #2 CPU pointer **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_CTX_IDX															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TX_CTX_IDX	Point to the next TXD CPU wants to use

15104C2C WDMA1 TX DTX_IDX 2 TX Ring #2 DMA pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DTX_IDX															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TX_DTX_IDX	Point to the next TXD DMA wants to use

15104C30 WDMA1 TX BASE_PTR 3 TX Ring #3 Base Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_BASE_PTR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	TX_BASE_PTR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_BASE_PTR	Point to the base address of TX Ring #3 (4-DW aligned address)

15104C34 WDMA1_TX_MAX_CNT_3 TX Ring #3 Maximum Count 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_MAX_CNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TX_MAX_CNT	The maximum number of TXD count in TX Ring #3

15104C38 WDMA1_TX_CTX_IDX_3 TX Ring #3 CPU pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_CTX_IDX															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TX_CTX_IDX	Point to the next TXD CPU wants to use

15104C3C **WDMA1 TX DTX_IDX 3** **TX Ring #3 DMA pointer** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DTX_IDX															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TX_DTX_IDX	Point to the next TXD DMA wants to use

15104D00 **WDMA1 RX_BASE_PTR 0** **RX Ring #0 Base Pointer** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_BASE_PTR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_BASE_PTR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_BASE_PTR	Point to the base address of RX Ring #0 (4-DW aligned address)

15104D04 **WDMA1 RX_MAX_CNT 0** **RX Ring #0 Maximum Count** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_MAX_CNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RX_MAX_CNT	The maximum number of RXD count in RX Ring #0

15104D08 **WDMA1 RX CRX IDX 0** RX Ring #0 CPU pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_CRX_IDX															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RX_CRX_IDX	Point to the next RXD CPU wants to use

15104D0C **WDMA1 RX DRX IDX 0** RX Ring #0 DMA pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	RX_DRX_IDX															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RX_DRX_IDX	Point to the next RXD DMA wants to use

15104D10 WDMA1 RX BASE PTR 1 RX Ring #1 Base Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_BASE_PTR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_BASE_PTR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_BASE_PTR	Point to the base address of RX Ring #1 (4-DW aligned address)

15104D14 WDMA1 RX MAX CNT 1 RX Ring #1 Maximum Count 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_MAX_CNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RX_MAX_CNT	The maximum number of RXD count in RX Ring #1

15104D18 **WDMA1 RX CRX_IDX 1** RX Ring #1 CPU pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_CRX_IDX															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RX_CRX_IDX	Point to the next RXD CPU wants to use

15104D1C **WDMA1 RX DRX_IDX 1** RX Ring #1 DMA pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_DRX_IDX															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RX_DRX_IDX	Point to the next RXD DMA wants to use

15104E00 **WDMA1 INFO**

WDMA Information

40000204

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					INDEX_WIDTH				BASE_PTR_WIDTH							
Type					RO				RO							
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_RING_NUM								TX_RING_NUM							
Type	RO								RO							
Reset	0	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0

Bit(s)	Name	Description
27:24	INDEX_WIDTH	Ring index width 0 means 16bits, 1~15 means 1~15bits
23:16	BASE_PTR_WIDTH	Base pointer width, x Base_addr[31:32-x] is shared with all ring base address. Only ring #0 base address[31:32-x] field is writable. [note]: "0" means no bit of base_address is shared.
15:8	RX_RING_NUM	RX ring number
7:0	TX_RING_NUM	TX ring number

15104E04 WDMA1_GLO_CFG								WDMA Global Configuration								50404E70
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_2B OFFSE T	CSR_CL KGATE _BYP	BYTE_S WAP	DEC_W COMP	PKT_W COMP	BYTE_S WAP_B IT_SEL	BIG_EN DIAN BIT_SE L									
Type	RW	RW	RW	RW	RW	RW	RW									
Reset	0	1	0	1	0	0	0									
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MULTI_CNT				MULTI _EN	RX_CH K_DDO NE	TX_CH K_DDO NE		BIG_EN DIAN	TX_WB DDON E	WDMA_BT_SIZ E	RX_DM A_BUS Y	RX_DM A_EN	TX_DM A_BUS Y	TX_DM A_EN	
Type	RW				RW	RW	RW		RW	RW	RW	RO	RW	RO	RW	
Reset	0	1	0	0	1	1	1		0	1	1	1	0	0	0	0

Bit(s)	Name	Description
31	RX_2B_OFFSET	Prepend 2-Byte to RX-buffer (packet) for aligning IP header to 32-bit boundary. Default MAC header is 14-Byte
30	CSR_CLKGATE_BYP	Clock gated Bypass
29	BYTE_SWAP	Byte Swap
28	DEC_WCOMP	DMA check WDONE or WCOMPLETE when update descriptor into DRAM
27	PKT_WCOMP	RX_DMA check WDONE or WCOMPLETE when write packet into DRAM
26	BYTE_SWAP_BIT_SEL	Bit selection for byte swap function
25	BIG_ENDIAN_BIT_SEL	Bit selection for endian control
15:12	MUTLI_CNT	Number of TX DMA read outstanding transactions when WDMA1_GLO_CFG[11] = 1'b1.
11	MULTI_EN	Enable TX DAM AXI read outstanding transaction
10	RX_CHK_DDONE	Enable RX_DMA check DDONE, if DDONE=1, DMA will into Coherence protection
9	TX_CHK_DDONE	Enable TX_DMA check DDONE, if DDONE=1, DMA will into Coherence protection
7	BIG_ENDIAN	Big endian
6	TX_WB_DDONE	
5:4	WDMA_BT_SIZE	The burst size of WDMA
3	RX_DMA_BUSY	
2	RX_DMA_EN	
1	TX_DMA_BUSY	
0	TX_DMA_EN	

15104E08	WDMA1_RST_IDX				WDMA Reset Index								00000000			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																RST_D RX_IDX 0
Type																WO
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RST_DT X_IDX1	RST_D TX_IDX 0
Type															WO	WO
Reset															0	0

Bit(s)	Name	Description
16	RST_DRX_IDX0	Write 1 to reset RX_DMA RX_IDX0 to 0
1	RST_DTX_IDX1	Write 1 to reset TX_DMA TX_IDX1 to 0
0	RST_DTX_IDX0	Write 1 to reset TX_DMA TX_IDX0 to 0

Bit(s)	Name	Description

15104E10 WDMA1 FREEQ_THRES WDMA Free Queue Threshold 00000002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													FREEQ_THRES			
Type													RW			
Reset													0	0	1	0

Bit(s)	Name	Description
3:0	FREEQ_THRES	RX free queue threshold WDMA will stop DMA interface when left RX descriptors reach this threshold

15104E20 WDMA1 INT_STATUS WDMA Interrupt Status 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_COHERENT	RX_DLY_INT	TX_COHERENT	TX_DLY_INT							RX_DONE_DL_Y_INT1	RX_DONE_DL_Y_INT0			RX_DONE_INT1	RX_DONE_INT0
Type	W1C	W1C	W1C	W1C							W1C	W1C			W1C	W1C
Reset	0	0	0	0							0	0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								TX_DONE_DL_Y_INT0								TX_DONE_INT0
Type								W1C								W1C
Reset								0								0

Bit(s)	Name	Description
31	RX_COHERENT	RX_DMA finds data coherent event while checking DDONE bit.
30	RX_DLY_INT	Summary of the whole WDMA RX related interrupts.

Bit(s)	Name	Description
29	TX_COHERENT	TX_DMA finds data coherent event while checking DDONE bit.
28	TX_DLY_INT	Summary of the whole WDMA TX related interrupts.
21	RX_DONE_DLY_INT1	RX ring #1 packet receive delay interrupt
20	RX_DONE_DLY_INT0	RX ring #0 packet receive delay interrupt
17	RX_DONE_INT1	RX ring #1 packet receive interrupt
16	RX_DONE_INT0	RX ring #0 packet receive interrupt
8	TX_DONE_DLY_INT0	TX ring #0 packet transmit delay interrupt
0	TX_DONE_INT0	TX ring #0 packet transmit interrupt

15104E28 WDMA1_INT_MASK WDMA Interrupt Mask 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_COHERENT	RX_DLY_INT	TX_COHERENT	TX_DLY_INT							RX_DONE_INT1	RX_DONE_INT0			RX_DONE_INT1	RX_DONE_INT0
Type	RW	RW	RW	RW							RW	RW			RW	RW
Reset	0	0	0	0							0	0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								TX_DONE_INT0								TX_DONE_INT0
Type								RW								RW
Reset								0								0

Bit(s)	Name	Description
31	RX_COHERENT	Interrupt enable for RX_DMA data coherent event
30	RX_DLY_INT	Summary of the whole WDMA RX related interrupts.
29	TX_COHERENT	Interrupt enable for TX_DMA data coherent event
28	TX_DLY_INT	Summary of the whole WDMA TX related interrupts.
21	RX_DONE_DLY_INT1	RX ring #1 packet receive delay interrupt
20	RX_DONE_DLY_INT0	RX ring #0 packet receive delay interrupt
17	RX_DONE_INT1	RX ring #1 packet receive interrupt
16	RX_DONE_INT0	RX ring #0 packet receive interrupt
8	TX_DONE_DLY_INT0	TX ring #0 packet transmit delay interrupt
0	TX_DONE_INT0	TX ring #0 packet transmit interrupt

15104E30 WDMA1_TX_DBG_MON0 WDMA TX Debug Monitor 0 00000090

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																

Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

15104E34 **WDMA1_TX_DBG_MON1** **WDMA TX Debug Monitor 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

15104E38 **WDMA1_RX_DBG_MON0** **WDMA RX Debug Monitor 0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																

Type																
Reset																

Bit(s)	Name	Description

15104E3C **WDMA1_RX_DBG_MON1** **WDMA RX Debug Monitor 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

15104E40 **WDMA1_INT_STS_GRP0** **WDMA Interrupt Status Group 0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WDMA_INT_STS_GRP0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WDMA_INT_STS_GRP0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	WDMA_INT_STS_GRP0	Interrupt group 0 status, this information already "and" with "~WDMA_INT_GRP1 & ~WDMA_INT_GRP2" Each bit definition is same as "WDMA_INT_STATUS"

Bit(s)	Name	Description

15104E44 WDMA1 INT_STS_GRP1 WDMA Interrupt Status Group 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WDMA_INT_STS_GRP1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WDMA_INT_STS_GRP1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	WDMA_INT_STS_GRP1	Interrupt group 1 status, this information already "and" with "WDMA_INT_GRP1" Each bit definition is same as "WDMA_INT_STATUS"

15104E48 WDMA1 INT_STS_GRP2 WDMA Interrupt Status Group 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WDMA_INT_STS_GRP2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WDMA_INT_STS_GRP2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	WDMA_INT_STS_GRP2	Interrupt group 2 status, this information already "and" with "WDMA_INT_GRP2" Each bit definition is same as "WDMA_INT_STATUS"

15104E4C WDMA1_INT_STS_GRP3 WDMA Interrupt Status Group 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WDMA_INT_STS_GRP3															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WDMA_INT_STS_GRP3															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	WDMA_INT_STS_GRP3	Interrupt group 3 status, this information already "and" with "WDMA_INT_GRP3" Each bit definition is same as "WDMA_INT_STATUS"

15104E50 WDMA1_INT_GRP1 WDMA Interrupt Group 1 Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WDMA_INT_GRP1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WDMA_INT_GRP1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	WDMA_INT_GRP1	Interrupt group 1 assignment. Each bit's definition is same as "WDMA_INT_STATUS"

15104E54 WDMA1_INT_GRP2 WDMA Interrupt Group 2 Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WDMA_INT_GRP2															

Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WDMA_INT_GRP2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	WDMA_INT_GRP2	Interrupt group 2 assignment. Each bit's definition is same as "WDMA_INT_STATUS"

15104E58 **WDMA1 INT_GRP3** **WDMA Interrupt Group 3 Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WDMA_INT_GRP3															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WDMA_INT_GRP3															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	WDMA_INT_GRP3	Interrupt group 3 assignment. Each bit's definition is same as "WDMA_INT_STATUS"

15104E60 **WDMA1 BUS_CFG** **WDMA AXI BUS Configuration** **00000400**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name						AXI_CTRL_UPDATED	AXI_R_BUSY	AXI_W_BUSY		AXI_LOCK_ERROR	AXI_ERRMID_SET_RIRQ	AXI_ERRMID_SET_BIRQ	AXI_OUTSTANDING_EXTEND	AXI_QOS_ON		AXI_CG_DISABLE
Type						RO	RO	RO		RO	RO	RO	RW	RW		RW
Reset						1	0	0		0	0	0	0	0		0

Bit(s)	Name	Description
10	AXI_CTRL_UPDATED	Master interface control signal updated status
9	AXI_R_BUSY	Read transaction not completes
8	AXI_W_BUSY	Write transaction not completes
6	AXI_LOCK_ERROR	Detects lock error
5	AXI_ERRMID_SET_RIRQ	Detects error MID from slave in R channel
4	AXI_ERRMID_SET_BIRQ	Detects error MID from slave in B channel
3	AXI_OUTSTANDING_EXTEND	Auto adds extra outstanding for QoS command
2	AXI_QOS_ON	Enable QoS function
0	AXI_CG_DISABLE	Disable auto clock gating of AXI component

15104E64 WDMA1_ULTRA_CFG WDMA AXI ULTRA Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AXI_ULTRA_EN					AXI_ULTRA_THRES										
Type	RW					RW										
Reset	0					0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AXI_PREULTRA_EN					AXI_PREULTRA_THRES										
Type	RW					RW										
Reset	0					0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	AXI_ULTRA_EN	Enable AXI Ultra transaction
26:16	AXI_ULTRA_THRES	AXI Ultra threshold. If CDM TX free FIFO count bigger than AXI_ULTRA_THRES, will trigger AXI Ultra transaction when AXI_ULTRA_EN = 1.
15	AXI_PREULTRA_EN	Enable AXI Pre-ultra transaction
10:0	AXI_PREULTRA_THRES	AXI Pre-ultra threshold.

Bit(s)	Name	Description
		If CDM TX free FIFO count bigger than AXI_PREULTRA_THRES, will trigger AXI Pre-ultra transaction when AXI_PREULTRA_EN = 1.

15104E68 WDMA1_PREF_CFG WDMA Prefetch Configuration 00000040

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											PREF_CNT				PREF_BUSY	PREF_EN
Type											RW				RO	RW
Reset											0				0	0

Bit(s)	Name	Description
5	PREF_CNT	Maximum Prefetch Count
1	PREF_BUSY	Prefetch Busy
0	PREF_EN	Prefetch Enable

15104E70 WDMA1_SDL_CFG WDMA SDL Configuration 00000800

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																SDL_EN
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SDL															
Type	RW															
Reset	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	SDL_EN	Enable RX_DMA read SDL from CR
15:0	SDL	RX_DMA read SDL value

Bit(s)	Name	Description

15104E74 WDMA1_IDLE_MASK WDMA IDLE MASK 00000030

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											DMA_IDLE	AXI_IDLE		IDLE_MASK		
Type											RO	RO		RW		
Reset											1	1		0	0	0

Bit(s)	Name	Description
5	DMA_IDLE	DMA idle status
4	AXI_IDLE	AXM idle status
2:0	IDLE_MASK	Idle signal mask

15104E80 WDMA1_SCH_Q01_CFG WDMA Scheduler Configuration for Q0&Q1 5C004C00

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_BKT_SIZE1	MAX_RATE_ULMT1	MAX_WEIGHT1		MIN_RATE_RATIO1		MAX_RATE1									
Type	RW	RW	RW		RW		RW									
Reset	0	1	0	1	1	1	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_BKT_SIZE0	MAX_RATE_ULMT0	MAX_WEIGHT0		MIN_RATE_RATIO0		MAX_RATE0									
Type	RW	RW	RW		RW		RW									
Reset	0	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MAX_BKT_SIZE1	Maximum bucket size

Bit(s)	Name	Description
30	MAX_RATE_ULMT1	Maximum rate limitation
29:28	MAX_WEIGHT1	Define the auto-reload bucket size if MAX_RATE_ULMT is set to 1. It is also served as excess bandwidth allocation ratio for servicing queue
27:26	MIN_RATE_RATIO1	Define the guaranteed Min rate based on MAX_RATE
25:16	MAX_RATE1	Define the limited Max rate for queue if MAX_RATE_ULMT is 0. The value specified represents the amount of 4-byte quota to be added into the queue #1 bucket per 125us. For example: If 512 is programmed, then the max rate limited is : $512 * 4 \text{ bytes}/125\text{us} = 16.384\text{M bytes/sec}$ or 131Mbps
15	MAX_BKT_SIZE0	Maximum bucket size
14	MAX_RATE_ULMT0	Maximum rate limitation
13:12	MAX_WEIGHT0	Define the auto-reload bucket size if MAX_RATE_ULMT is set to 1. It is also served as excess bandwidth allocation ratio for servicing queue
11:10	MIN_RATE_RATIO0	Define the guaranteed Min rate based on MAX_RATE
9:0	MAX_RATE0	Define the limited Max rate for queue if MAX_RATE_ULMT is 0. The value specified represents the amount of 4-byte quota to be added into the queue #1 bucket per 125us. For example: If 512 is programmed, then the max rate limited is : $512 * 4 \text{ bytes}/125\text{us} = 16.384\text{M bytes/sec}$ or 131Mbps

15104E84		WDMA1 SCH_Q23_CFG				WDMA Scheduler Configuration for Q2&Q3										7C006C00	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
Name	MAX_BKT_SIZE3	MAX_RATE_ULMT3	MAX_WEIGHT3		MIN_RATE_RATIO3		MAX_RATE3										
Type	RW	RW	RW		RW		RW										
Reset	0	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Name	MAX_BKT_SIZE2	MAX_RATE_ULMT2	MAX_WEIGHT2		MIN_RATE_RATIO2		MAX_RATE2										
Type	RW	RW	RW		RW		RW										
Reset	0	1	1	0	1	1	0	0	0	0	0	0	0	0	0	0	

Bit(s)	Name	Description
31	MAX_BKT_SIZE3	Maximum bucket size
30	MAX_RATE_ULMT3	Maximum rate limitation
29:28	MAX_WEIGHT3	Define the auto-reload bucket size if MAX_RATE_ULMT is set to 1. It is also served as excess bandwidth allocation ratio for servicing queue
27:26	MIN_RATE_RATIO3	Define the guaranteed Min rate based on MAX_RATE
25:16	MAX_RATE3	Define the limited Max rate for queue if MAX_RATE_ULMT is 0. The value specified represents the amount of 4-byte quota to be added into the queue #1 bucket per 125us. For example: If 512 is programmed, then the max rate limited is :

Bit(s)	Name	Description
15	MAX_BKT_SIZE2	512 * 4 bytes/125us = 16.384M bytes/sec or 131Mbps Maximum bucket size
14	MAX_RATE_ULMT2	Maximum rate limitation
13:12	MAX_WEIGHT2	Define the auto-reload bucket size if MAX_RATE_ULMT is set to 1. It is also served as excess bandwidth allocation ratio for servicing queue
11:10	MIN_RATE_RATIO2	Define the guaranteed Min rate based on MAX_RATE
9:0	MAX_RATE2	Define the limited Max rate for queue if MAX_RATE_ULMT is 0. The value specified represents the amount of 4-byte quota to be added into the queue #1 bucket per 125us. For example: If 512 is programmed, then the max rate limited is : 512 * 4 bytes/125us = 16.384M bytes/sec or 131Mbps

15104E90 **WDMA1_INT_STATUS_0** **WDMA Interrupt Status 0** 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_COHERENT	RX_DLY_INT	TX_COHERENT	TX_DLY_INT							RX_DONE_DLY_INT1	RX_DONE_DLY_INT0			RX_DONE_INT1	RX_DONE_INT0
Type	W1C	W1C	W1C	W1C							W1C	W1C			W1C	W1C
Reset	0	0	0	0							0	0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								TX_DONE_DLY_INT0								TX_DONE_INT0
Type								W1C								W1C
Reset								0								0

Bit(s)	Name	Description
31	RX_COHERENT	RX_DMA finds data coherent event while checking DDONE bit.
30	RX_DLY_INT	Summary of the whole WDMA RX related interrupts.
29	TX_COHERENT	TX_DMA finds data coherent event while checking DDONE bit.
28	TX_DLY_INT	Summary of the whole WDMA TX related interrupts.
21	RX_DONE_DLY_INT1	RX ring #1 packet receive delay interrupt
20	RX_DONE_DLY_INT0	RX ring #0 packet receive delay interrupt
17	RX_DONE_INT1	RX ring #1 packet receive interrupt
16	RX_DONE_INT0	RX ring #0 packet receive interrupt
8	TX_DONE_DLY_INT0	TX ring #0 packet transmit delay interrupt
0	TX_DONE_INT0	TX ring #0 packet transmit interrupt

15104E94 **WDMA1_INT_MASK_0** **WDMA Interrupt Mask 0** 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	RX_CO HEREN T	RX_DLY _INT	TX_CO HEREN T	TX_DLY _INT							RX_DO NE_DL Y_INT1	RX_DO NE_DL Y_INT0			RX_DO NE_INT 1	RX_DO NE_INT 0
Type	RW	RW	RW	RW							RW	RW			RW	RW
Reset	0	0	0	0							0	0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								TX_DO NE_DL Y_INT0								TX_DO NE_INT 0
Type								RW								RW
Reset								0								0

Bit(s)	Name	Description
31	RX_COHERENT	Interrupt enable for RX_DMA data coherent event
30	RX_DLY_INT	Summary of the whole WDMA RX related interrupts.
29	TX_COHERENT	Interrupt enable for TX_DMA data coherent event
28	TX_DLY_INT	Summary of the whole WDMA TX related interrupts.
21	RX_DONE_DLY_INT1	RX ring #1 packet receive delay interrupt
20	RX_DONE_DLY_INT0	RX ring #0 packet receive delay interrupt
17	RX_DONE_INT1	RX ring #1 packet receive interrupt
16	RX_DONE_INT0	RX ring #0 packet receive interrupt
8	TX_DONE_DLY_INT0	TX ring #0 packet transmit delay interrupt
0	TX_DONE_INT0	TX ring #0 packet transmit interrupt

15104E98 WDMA1 INT STATUS 1 WDMA Interrupt Status 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_CO HEREN T	RX_DLY _INT	TX_CO HEREN T	TX_DLY _INT							RX_DO NE_DL Y_INT1	RX_DO NE_DL Y_INT0			RX_DO NE_INT 1	RX_DO NE_INT 0
Type	W1C	W1C	W1C	W1C							W1C	W1C			W1C	W1C
Reset	0	0	0	0							0	0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								TX_DO NE_DL Y_INT0								TX_DO NE_INT 0
Type								W1C								W1C
Reset								0								0

Bit(s)	Name	Description
31	RX_COHERENT	RX_DMA finds data coherent event while checking DDONE bit.
30	RX_DLY_INT	Summary of the whole WDMA RX related interrupts.
29	TX_COHERENT	TX_DMA finds data coherent event while checking DDONE bit.
28	TX_DLY_INT	Summary of the whole WDMA TX related interrupts.
21	RX_DONE_DLY_INT1	RX ring #1 packet receive delay interrupt
20	RX_DONE_DLY_INT0	RX ring #0 packet receive delay interrupt
17	RX_DONE_INT1	RX ring #1 packet receive interrupt
16	RX_DONE_INT0	RX ring #0 packet receive interrupt
8	TX_DONE_DLY_INT0	TX ring #0 packet transmit delay interrupt
0	TX_DONE_INT0	TX ring #0 packet transmit interrupt

15104E9C WDMA1 INT MASK 1 WDMA Interrupt Mask 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_COHERENT	RX_DLY_INT	TX_COHERENT	TX_DLY_INT							RX_DONE_INT1	RX_DONE_INT0			RX_DONE_INT1	RX_DONE_INT0
Type	RW	RW	RW	RW							RW	RW			RW	RW
Reset	0	0	0	0							0	0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								TX_DONE_INT0								TX_DONE_INT0
Type								RW								RW
Reset								0								0

Bit(s)	Name	Description
31	RX_COHERENT	Interrupt enable for RX_DMA data coherent event
30	RX_DLY_INT	Summary of the whole WDMA RX related interrupts.
29	TX_COHERENT	Interrupt enable for TX_DMA data coherent event
28	TX_DLY_INT	Summary of the whole WDMA TX related interrupts.
21	RX_DONE_DLY_INT1	RX ring #1 packet receive delay interrupt
20	RX_DONE_DLY_INT0	RX ring #0 packet receive delay interrupt
17	RX_DONE_INT1	RX ring #1 packet receive interrupt
16	RX_DONE_INT0	RX ring #0 packet receive interrupt
8	TX_DONE_DLY_INT0	TX ring #0 packet transmit delay interrupt
0	TX_DONE_INT0	TX ring #0 packet transmit interrupt

15104EA0 WDMA1 INT STATUS 2 WDMA Interrupt Status 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	RX_CO HEREN T	RX_DLY _INT	TX_CO HEREN T	TX_DLY _INT							RX_DO NE_DL Y_INT1	RX_DO NE_DL Y_INT0			RX_DO NE_INT 1	RX_DO NE_INT 0
Type	W1C	W1C	W1C	W1C							W1C	W1C			W1C	W1C
Reset	0	0	0	0							0	0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								TX_DO NE_DL Y_INT0								TX_DO NE_INT 0
Type								W1C								W1C
Reset								0								0

Bit(s)	Name	Description
31	RX_COHERENT	RX_DMA finds data coherent event while checking DDONE bit.
30	RX_DLY_INT	Summary of the whole WDMA RX related interrupts.
29	TX_COHERENT	TX_DMA finds data coherent event while checking DDONE bit.
28	TX_DLY_INT	Summary of the whole WDMA TX related interrupts.
21	RX_DONE_DLY_INT1	RX ring #1 packet receive delay interrupt
20	RX_DONE_DLY_INT0	RX ring #0 packet receive delay interrupt
17	RX_DONE_INT1	RX ring #1 packet receive interrupt
16	RX_DONE_INT0	RX ring #0 packet receive interrupt
8	TX_DONE_DLY_INT0	TX ring #0 packet transmit delay interrupt
0	TX_DONE_INT0	TX ring #0 packet transmit interrupt

15104EA4 WDMA1 INT MASK 2 WDMA Interrupt Mask 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_CO HEREN T	RX_DLY _INT	TX_CO HEREN T	TX_DLY _INT							RX_DO NE_DL Y_INT1	RX_DO NE_DL Y_INT0			RX_DO NE_INT 1	RX_DO NE_INT 0
Type	RW	RW	RW	RW							RW	RW			RW	RW
Reset	0	0	0	0							0	0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								TX_DO NE_DL Y_INT0								TX_DO NE_INT 0
Type								RW								RW
Reset								0								0

Bit(s)	Name	Description
31	RX_COHERENT	Interrupt enable for RX_DMA data coherent event
30	RX_DLY_INT	Summary of the whole WDMA RX related interrupts.
29	TX_COHERENT	Interrupt enable for TX_DMA data coherent event
28	TX_DLY_INT	Summary of the whole WDMA TX related interrupts.
21	RX_DONE_DLY_INT1	RX ring #1 packet receive delay interrupt
20	RX_DONE_DLY_INT0	RX ring #0 packet receive delay interrupt
17	RX_DONE_INT1	RX ring #1 packet receive interrupt
16	RX_DONE_INT0	RX ring #0 packet receive interrupt
8	TX_DONE_DLY_INT0	TX ring #0 packet transmit delay interrupt
0	TX_DONE_INT0	TX ring #0 packet transmit interrupt

15104EA8 WDMA1 INT STATUS 3 WDMA Interrupt Status 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_COHERENT	RX_DLY_INT	TX_COHERENT	TX_DLY_INT							RX_DONE_INT1	RX_DONE_INT0			RX_DONE_INT1	RX_DONE_INT0
Type	W1C	W1C	W1C	W1C							W1C	W1C			W1C	W1C
Reset	0	0	0	0							0	0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								TX_DONE_INT0								TX_DONE_INT0
Type								W1C								W1C
Reset								0								0

Bit(s)	Name	Description
31	RX_COHERENT	RX_DMA finds data coherent event while checking DDONE bit.
30	RX_DLY_INT	Summary of the whole WDMA RX related interrupts.
29	TX_COHERENT	TX_DMA finds data coherent event while checking DDONE bit.
28	TX_DLY_INT	Summary of the whole WDMA TX related interrupts.
21	RX_DONE_DLY_INT1	RX ring #1 packet receive delay interrupt
20	RX_DONE_DLY_INT0	RX ring #0 packet receive delay interrupt
17	RX_DONE_INT1	RX ring #1 packet receive interrupt
16	RX_DONE_INT0	RX ring #0 packet receive interrupt
8	TX_DONE_DLY_INT0	TX ring #0 packet transmit delay interrupt
0	TX_DONE_INT0	TX ring #0 packet transmit interrupt

15104EAC WDMA1 INT MASK 3 WDMA Interrupt Mask 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	RX_COHERENT	RX_DLY_INT	TX_COHERENT	TX_DLY_INT							RX_DONE_DLY_INT1	RX_DONE_DLY_INT0			RX_DONE_INT1	RX_DONE_INT0
Type	RW	RW	RW	RW							RW	RW			RW	RW
Reset	0	0	0	0							0	0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								TX_DONE_DLY_INT0								TX_DONE_INT0
Type								RW								RW
Reset								0								0

Bit(s)	Name	Description
31	RX_COHERENT	Interrupt enable for RX_DMA data coherent event
30	RX_DLY_INT	Summary of the whole WDMA RX related interrupts.
29	TX_COHERENT	Interrupt enable for TX_DMA data coherent event
28	TX_DLY_INT	Summary of the whole WDMA TX related interrupts.
21	RX_DONE_DLY_INT1	RX ring #1 packet receive delay interrupt
20	RX_DONE_DLY_INT0	RX ring #0 packet receive delay interrupt
17	RX_DONE_INT1	RX ring #1 packet receive interrupt
16	RX_DONE_INT0	RX ring #0 packet receive interrupt
8	TX_DONE_DLY_INT0	TX ring #0 packet transmit delay interrupt
0	TX_DONE_INT0	TX ring #0 packet transmit interrupt

15104EB0 WDMA1 TX DELAY INT_CFG WDMA Tx Delay Interrupt Configuration 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RING0_TXDLY_INT_EN	RING0_TXMAX_PINT							RING0_TXMAX_PTIME							
Type	RW	RW							RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	RING0_TXDLY_INT_EN	Enable delay interrupt mechanism for Tx Ring 0
14:8	RING0_TXMAX_PINT	Specified Max. number of pended interrupts [Note] reset to 0 can disable pending interrupt count check.
7:0	RING0_TXMAX_PTIME	Specified Max. pended time [Note] reset to 0 can disable pending interrupt time check.

15104EB4 WDMA1_TX_DELAY_INT_CFG WDMA Tx Delay Interrupt Configuration 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

15104EC0 WDMA1_RX_DELAY_INT_CFG WDMA Rx Delay Interrupt Configuration 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RING1_RXDLY_INT_EN	RING1_RXMAX_PINT							RING1_RXMAX_PTIME							
Type	RW	RW							RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RING0_RXDLY_INT_EN	RING0_RXMAX_PINT							RING0_RXMAX_PTIME							
Type	RW	RW							RW							

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	RING1_RXDLY_INT_EN	Enable delay interrupt mechanism for Rx Ring 1
30:24	RING1_RXMAX_PINT	Specified Max. number of pended interrupts [Note] reset to 0 can disable pending interrupt count check.
23:16	RING1_RXMAX_PTIME	Specified Max. pended time [Note] reset to 0 can disable pending interrupt time check.
15	RING0_RXDLY_INT_EN	Enable delay interrupt mechanism for Rx Ring 0
14:8	RING0_RXMAX_PINT	Specified Max. number of pended interrupts [Note] reset to 0 can disable pending interrupt count check.
7:0	RING0_RXMAX_PTIME	Specified Max. pended time [Note] reset to 0 can disable pending interrupt time check.

15104EC8	WDMA1_RX_FC_CFG_0				WDMA Rx Flow Control Configuration 0												00000000	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16		
Name					RING0_FC_DASRT_THRES													
Type					RW													
Reset					0	0	0	0	0	0	0	0	0	0	0	0		
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
Name					RING0_FC_ASRT_THRES													
Type					RW													
Reset					0	0	0	0	0	0	0	0	0	0	0	0		

Bit(s)	Name	Description
27:16	RING0_FC_DASRT_THRES	Specified PFC deassert threshold. Disable PFC when free DMAD count > threshold.
11:0	RING0_FC_ASRT_THRES	Specified PFC assert threshold. Enable PFC when free DMAD count < threshold. Threshold = 0 means PFC disabled

15104ECC	WDMA1_RX_FC_CFG_1				WDMA Rx Flow Control Configuration 1												00000000	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16		
Name					RING1_FC_DASRT_THRES													
Type					RW													
Reset					0	0	0	0	0	0	0	0	0	0	0	0		

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RING1_FC_ASRT_THRES											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
27:16	RING1_FC_DASRT_THRES	Specified PFC deassert threshold. Disable PFC when free DMAD count > threshold.
11:0	RING1_FC_ASRT_THRES	Specified PFC assert threshold. Enable PFC when free DMAD count < threshold. Threshold = 0 means PFC disabled.

15106000 ADMA TX BASE PTR 0 TX Ring #0 Base Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_BASE_PTR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_BASE_PTR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_BASE_PTR	Point to the base address of TX Ring #0 (4-DW aligned address)

15106004 ADMA TX MAX CNT 0 TX Ring #0 Maximum Count 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					TX_MAX_CNT											

Type					RW										
Reset					0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	TX_MAX_CNT	The maximum number of TXD count in TX Ring #0

15106008 ADMA TX CTX_IDX_0 TX Ring #0 CPU pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					TX_CTX_IDX											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	TX_CTX_IDX	Point to the next TXD CPU wants to use

1510600C ADMA TX DTX_IDX_0 TX Ring #0 DMA pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					TX_DTX_IDX											
Type					RO											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	TX_DTX_IDX	Point to the next TXD DMA wants to use

15106010 ADMA TX BASE_PTR_1 TX Ring #1 Base Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_BASE_PTR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_BASE_PTR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_BASE_PTR	Point to the base address of TX Ring #1 (4-DW aligned address)

15106014 ADMA TX MAX_CNT_1 TX Ring #1 Maximum Count 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					TX_MAX_CNT											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	TX_MAX_CNT	The maximum number of TXD count in TX Ring #1

15106018 ADMA TX CTX_IDX_1 TX Ring #1 CPU pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					TX_CTX_IDX											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	TX_CTX_IDX	Point to the next TXD CPU wants to use

1510601C ADMA_TX_DTX_IDX_1 TX Ring #1 DMA pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					TX_DTX_IDX											
Type					RO											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	TX_DTX_IDX	Point to the next TXD DMA wants to use

15106020 ADMA_TX_BASE_PTR_2 TX Ring #2 Base Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_BASE_PTR															
Type	RW															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_BASE_PTR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_BASE_PTR	Point to the base address of TX Ring #2 (4-DW aligned address)

15106024 ADMA TX MAX CNT 2 TX Ring #2 Maximum Count 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	TX_MAX_CNT	The maximum number of TXD count in TX Ring #2

15106028 ADMA TX CTX_IDX 2 TX Ring #2 CPU pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																

Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	TX_CTX_IDX	Point to the next TXD CPU wants to use

1510602C ADMA_TX_DTX_IDX_2 TX Ring #2 DMA pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					TX_DTX_IDX											
Type					RO											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	TX_DTX_IDX	Point to the next TXD DMA wants to use

15106030 ADMA_TX_BASE_PTR_3 TX Ring #3 Base Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_BASE_PTR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_BASE_PTR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_BASE_PTR	Point to the base address of TX Ring #3 (4-DW aligned address)

15106034 **ADMA TX MAX CNT 3** TX Ring #3 Maximum Count 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					TX_MAX_CNT											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	TX_MAX_CNT	The maximum number of TXD count in TX Ring #3

15106038 **ADMA TX CTX IDX 3** TX Ring #3 CPU pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					TX_CTX_IDX											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	TX_CTX_IDX	Point to the next TXD CPU wants to use

1510603C **ADMA TX DTX IDX 3** TX Ring #3 DMA pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																

Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					TX_DTX_IDX											
Type					RO											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	TX_DTX_IDX	Point to the next TXD DMA wants to use

15106100 ADMA RX BASE PTR 0 RX Ring #0 Base Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_BASE_PTR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_BASE_PTR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_BASE_PTR	Point to the base address of RX Ring #0 (4-DW aligned address)

15106104 ADMA RX MAX CNT 0 RX Ring #0 Maximum Count 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RX_MAX_CNT											
Type					RW											

Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	RX_MAX_CNT	The maximum number of RXD count in RX Ring #0

15106108 ADMA_RX_CRX_IDX_0 RX Ring #0 CPU pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RX_CRX_IDX											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	RX_CRX_IDX	Point to the next RXD CPU wants to use

1510610C ADMA_RX_DRX_IDX_0 RX Ring #0 DMA pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RX_DRX_IDX											
Type					RO											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	RX_DRX_IDX	Point to the next RXD DMA wants to use

15106110 ADMA_RX_BASE_PTR_1 RX Ring #1 Base Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_BASE_PTR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_BASE_PTR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_BASE_PTR	Point to the base address of RX Ring #1 (4-DW aligned address)

15106114 ADMA_RX_MAX_CNT_1 RX Ring #1 Maximum Count 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	RX_MAX_CNT	The maximum number of RXD count in RX Ring #1

15106118 ADMA_RX_CRX_IDX_1 RX Ring #1 CPU pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																

Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_CRX_IDX															
Type	RW															
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	RX_CRX_IDX	Point to the next RXD CPU wants to use

1510611C ADMA RX DRX_IDX 1 RX Ring #1 DMA pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_DRX_IDX															
Type	RO															
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	RX_DRX_IDX	Point to the next RXD DMA wants to use

15106120 ADMA RX_BASE_PTR 2 RX Ring #2 Base Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_BASE_PTR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_BASE_PTR															

Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_BASE_PTR	Point to the base address of RX Ring #2 (4-DW aligned address)

15106124 **ADMA_RX_MAX_CNT_2** RX Ring #2 Maximum Count 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RX_MAX_CNT											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	RX_MAX_CNT	The maximum number of RXD count in RX Ring #2

15106128 **ADMA_RX_CRX_IDX_2** RX Ring #2 CPU pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RX_CRX_IDX											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	RX_CRX_IDX	Point to the next RXD CPU wants to use

Bit(s)	Name	Description

1510612C ADMA RX DRX_IDX 2 RX Ring #2 DMA pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RX_DRX_IDX											
Type					RO											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	RX_DRX_IDX	Point to the next RXD DMA wants to use

15106130 ADMA RX_BASE_PTR 3 RX Ring #3 Base Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_BASE_PTR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_BASE_PTR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_BASE_PTR	Point to the base address of RX Ring #3 (4-DW aligned address)

15106134 ADMA RX_MAX_CNT 3 RX Ring #3 Maximum Count 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RX_MAX_CNT											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	RX_MAX_CNT	The maximum number of RXD count in RX Ring #3

15106138 ADMA_RX_CRX_IDX_3 RX Ring #3 CPU pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RX_CRX_IDX											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	RX_CRX_IDX	Point to the next RXD CPU wants to use

1510613C ADMA_RX_DRX_IDX_3 RX Ring #3 DMA pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RX_DRX_IDX											
Type					RO											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	RX_DRX_IDX	Point to the next RXD DMA wants to use

15106140 ADMA RX_BASE_PTR_4 RX Ring #4 Base Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_BASE_PTR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_BASE_PTR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_BASE_PTR	Point to the base address of RX Ring #4 (4-DW aligned address)

15106144 ADMA RX_MAX_CNT_4 RX Ring #4 Maximum Count 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RX_MAX_CNT											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	RX_MAX_CNT	The maximum number of RXD count in RX Ring #4

15106148 ADMA RX CRX IDX 4 RX Ring #4 CPU pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RX_CRX_IDX											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	RX_CRX_IDX	Point to the next RXD CPU wants to use

1510614C ADMA RX DRX IDX 4 RX Ring #4 DMA pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RX_DRX_IDX											
Type					RO											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	RX_DRX_IDX	Point to the next RXD DMA wants to use

15106150 ADMA RX BASE PTR 5 RX Ring #5 Base Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_BASE_PTR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_BASE_PTR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_BASE_PTR	Point to the base address of RX Ring #5 (4-DW aligned address)

15106154 ADMA_RX_MAX_CNT_5 RX Ring #5 Maximum Count 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RX_MAX_CNT											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	RX_MAX_CNT	The maximum number of RXD count in RX Ring #5

15106158 ADMA_RX_CRX_IDX_5 RX Ring #5 CPU pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RX_CRX_IDX											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	RX_CRX_IDX	Point to the next RXD CPU wants to use

1510615C ADMA RX DRX_IDX_5 RX Ring #5 DMA pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RX_DRX_IDX											
Type					RO											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	RX_DRX_IDX	Point to the next RXD DMA wants to use

15106160 ADMA RX_BASE_PTR_6 RX Ring #6 Base Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_BASE_PTR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_BASE_PTR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_BASE_PTR	Point to the base address of RX Ring #6 (4-DW aligned address)

15106164 ADMA RX MAX CNT 6 RX Ring #6 Maximum Count 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RX_MAX_CNT											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	RX_MAX_CNT	The maximum number of RXD count in RX Ring #6

15106168 ADMA RX CRX IDX 6 RX Ring #6 CPU pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RX_CRX_IDX											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	RX_CRX_IDX	Point to the next RXD CPU wants to use

1510616C ADMA RX DRX IDX 6 RX Ring #6 DMA pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RX_DRX_IDX											
Type					RO											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	RX_DRX_IDX	Point to the next RXD DMA wants to use

15106170 ADMA_RX_BASE_PTR_7 RX Ring #7 Base Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_BASE_PTR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_BASE_PTR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_BASE_PTR	Point to the base address of RX Ring #7 (4-DW aligned address)

15106174 ADMA_RX_MAX_CNT_7 RX Ring #7 Maximum Count 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RX_MAX_CNT											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	RX_MAX_CNT	The maximum number of RXD count in RX Ring #7

15106178 ADMA_RX_CRX_IDX_7 RX Ring #7 CPU pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RX_CRX_IDX											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	RX_CRX_IDX	Point to the next RXD CPU wants to use

1510617C ADMA_RX_DRX_IDX_7 RX Ring #7 DMA pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RX_DRX_IDX											
Type					RO											

Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	RX_DRX_IDX	Point to the next RXD DMA wants to use

15106200 ADMA_INFO ADMA Information 4C000804

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					INDEX_WIDTH				BASE_PTR_WIDTH							
Type					RO				RO							
Reset					1	1	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_RING_NUM								TX_RING_NUM							
Type	RO								RO							
Reset	0	0	0	0	1	0	0	0	0	0	0	0	0	1	0	0

Bit(s)	Name	Description
27:24	INDEX_WIDTH	Ring index width
23:16	BASE_PTR_WIDTH	Base pointer width, x Base_addr[31:32-x] is shared with all ring base address. Only ring #0 base address[31:32-x] field is writable. [note]: "0" means no bit of base_address is shared.
15:8	RX_RING_NUM	RX ring number
7:0	TX_RING_NUM	TX ring number

15106204 ADMA_GLO_CFG ADMA Global Configuration 50404C70

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_2B_OFFSET	CSR_CLK_GATE_BYP	BYTE_SWAP	DEC_WCOMP	PKT_WCOMP	BYTE_SWAP_BIT_SEL	BIG_ENDIAN_BIT_SEL									
Type	RW	RW	RW	RW	RW	RW	RW									
Reset	0	1	0	1	0	0	0									
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	MUTLI_CNT				MULTI_EN	CHK_D DONE		RX_DMA_LRO_EN	BIG_ENDIAN	TX_WB_DDONE	DMA_BT_SIZE		RX_DMA_BUSY	RX_DMA_EN	TX_DMA_BUSY	TX_DMA_EN
Type	RW				RW	RW		RW	RW	RW	RW		RO	RW	RO	RW
Reset	0	1	0	0	1	1		0	0	1	1	1	0	0	0	0

Bit(s)	Name	Description
31	RX_2B_OFFSET	Prepend 2-Byte to RX-buffer (packet) for aligning IP header to 32-bit boundary. Default MAC header is 14-Byte
30	CSR_CLKGATE_BYP	Clock gated Bypass
29	BYTE_SWAP	Byte Swap
28	DEC_WCOMP	DMA check WDONE or WCOMPLETE when update descriptor into DRAM
27	PKT_WCOMP	RX_DMA check WDONE or WCOMPLETE when write packet into DRAM
26	BYTE_SWAP_BIT_SEL	Bit selection for byte swap function
25	BIG_ENDIAN_BIT_SEL	Bit selection for endian control
15:12	MUTLI_CNT	Number of TX DMA read outstanding transactions when ADMA_GLO_CFG[11] = 1'b1.
11	MULTI_EN	Enable TX DAM AXI read outstanding transaction
10	CHK_DDONE	Enable DMA check DDONE, if DDONE=1, DMA will into Coherence protection
8	RX_DMA_LRO_EN	ADMA RX DMA LRO Enable
7	BIG_ENDIAN	Big endian
6	TX_WB_DDONE	
5:4	DMA_BT_SIZE	The burst size of ADMA
3	RX_DMA_BUSY	
2	RX_DMA_EN	
1	TX_DMA_BUSY	
0	TX_DMA_EN	

15106208 **ADMA_RST_IDX** ADMA Reset Index 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									RST_D RX_IDX 7	RST_D RX_IDX 6	RST_D RX_IDX 5	RST_D RX_IDX 4	RST_D RX_IDX 3	RST_D RX_IDX 2	RST_D RX_IDX 1	RST_D RX_IDX 0
Type									WO	WO	WO	WO	WO	WO	WO	WO
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													RST_DT X_IDX3	RST_DT X_IDX2	RST_DT X_IDX1	RST_D TX_IDX 0
Type													WO	WO	WO	WO

Reset													0	0	0	0

Bit(s)	Name	Description
23	RST_DRX_IDX7	Write 1 to reset RX_DMA RX_IDX7 to 0
22	RST_DRX_IDX6	Write 1 to reset RX_DMA RX_IDX6 to 0
21	RST_DRX_IDX5	Write 1 to reset RX_DMA RX_IDX5 to 0
20	RST_DRX_IDX4	Write 1 to reset RX_DMA RX_IDX4 to 0
19	RST_DRX_IDX3	Write 1 to reset RX_DMA RX_IDX3 to 0
18	RST_DRX_IDX2	Write 1 to reset RX_DMA RX_IDX2 to 0
17	RST_DRX_IDX1	Write 1 to reset RX_DMA RX_IDX1 to 0
16	RST_DRX_IDX0	Write 1 to reset RX_DMA RX_IDX0 to 0
3	RST_DTX_IDX3	Write 1 to reset TX_DMA TX_IDX3 to 0
2	RST_DTX_IDX2	Write 1 to reset TX_DMA TX_IDX2 to 0
1	RST_DTX_IDX1	Write 1 to reset TX_DMA TX_IDX1 to 0
0	RST_DTX_IDX0	Write 1 to reset TX_DMA TX_IDX0 to 0

15106210 ADMA_RX_CFG ADMA Rx DMA Configuration 00000002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	LRO_SDL															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													FREEQ_THRES			
Type													RW			
Reset													0	0	1	0

Bit(s)	Name	Description
31:16	LRO_SDL	ADMA LRO Free Buffer SDL
3:0	FREEQ_THRES	RX free queue threshold ADMA will stop DMA interface when left RX descriptors reach this threshold

15106220 ADMA_INT_STATUS ADMA Interrupt Status 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_DO NE_DL Y_INT7	RX_DO NE_DL Y_INT6	RX_DO NE_DL Y_INT5	RX_DO NE_DL Y_INT4	RX_DO NE_DL Y_INT3	RX_DO NE_DL Y_INT2	RX_DO NE_DL Y_INT1	RX_DO NE_DL Y_INT0	RX_DO NE_INT 7	RX_DO NE_INT 6	RX_DO NE_INT 5	RX_DO NE_INT 4	RX_DO NE_INT 3	RX_DO NE_INT 2	RX_DO NE_INT 1	RX_DO NE_INT 0
Type	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_CO HEREN T	RX_DLY _INT	TX_CO HEREN T	TX_DLY _INT					TX_DO NE_DL Y_INT3	TX_DO NE_DL Y_INT2	TX_DO NE_DL Y_INT1	TX_DO NE_DL Y_INT0	TX_DO NE_INT 3	TX_DO NE_INT 2	TX_DO NE_INT 1	TX_DO NE_INT 0
Type	W1C	W1C	W1C	W1C					W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C
Reset	0	0	0	0					0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	RX_DONE_DLY_INT7	RX ring #7 packet receive delay interrupt
30	RX_DONE_DLY_INT6	RX ring #6 packet receive delay interrupt
29	RX_DONE_DLY_INT5	RX ring #5 packet receive delay interrupt
28	RX_DONE_DLY_INT4	RX ring #4 packet receive delay interrupt
27	RX_DONE_DLY_INT3	RX ring #3 packet receive delay interrupt
26	RX_DONE_DLY_INT2	RX ring #2 packet receive delay interrupt
25	RX_DONE_DLY_INT1	RX ring #1 packet receive delay interrupt
24	RX_DONE_DLY_INT0	RX ring #0 packet receive delay interrupt
23	RX_DONE_INT7	RX ring #7 packet receive interrupt
22	RX_DONE_INT6	RX ring #6 packet receive interrupt
21	RX_DONE_INT5	RX ring #5 packet receive interrupt
20	RX_DONE_INT4	RX ring #4 packet receive interrupt
19	RX_DONE_INT3	RX ring #3 packet receive interrupt
18	RX_DONE_INT2	RX ring #2 packet receive interrupt
17	RX_DONE_INT1	RX ring #1 packet receive interrupt
16	RX_DONE_INT0	RX ring #0 packet receive interrupt
15	RX_COHERENT	RX_DMA finds data coherent event while checking DDONE bit.
14	RX_DLY_INT	Summary of the whole ADMA RX related interrupts.
13	TX_COHERENT	TX_DMA finds data coherent event while checking DDONE bit.
12	TX_DLY_INT	Summary of the whole ADMA TX related interrupts.
7	TX_DONE_DLY_INT3	TX ring #3 packet transmit delay interrupt
6	TX_DONE_DLY_INT2	TX ring #2 packet transmit delay interrupt
5	TX_DONE_DLY_INT1	TX ring #1 packet transmit delay interrupt
4	TX_DONE_DLY_INT0	TX ring #0 packet transmit delay interrupt
3	TX_DONE_INT3	TX ring #3 packet transmit interrupt
2	TX_DONE_INT2	TX ring #2 packet transmit interrupt
1	TX_DONE_INT1	TX ring #1 packet transmit interrupt
0	TX_DONE_INT0	TX ring #0 packet transmit interrupt

15106228	ADMA_INT_MASK				ADMA Interrupt Mask												00000000	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16		
Name	RX_DO NE_DL Y_INT7	RX_DO NE_DL Y_INT6	RX_DO NE_DL Y_INT5	RX_DO NE_DL Y_INT4	RX_DO NE_DL Y_INT3	RX_DO NE_DL Y_INT2	RX_DO NE_DL Y_INT1	RX_DO NE_DL Y_INT0	RX_DO NE_INT 7	RX_DO NE_INT 6	RX_DO NE_INT 5	RX_DO NE_INT 4	RX_DO NE_INT 3	RX_DO NE_INT 2	RX_DO NE_INT 1	RX_DO NE_INT 0		
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW		

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_CO HEREN T	RX_DLY _INT	TX_CO HEREN T	TX_DLY _INT					TX_DO NE_DL Y_INT3	TX_DO NE_DL Y_INT2	TX_DO NE_DL Y_INT1	TX_DO NE_DL Y_INT0	TX_DO NE_INT 3	TX_DO NE_INT 2	TX_DO NE_INT 1	TX_DO NE_INT 0
Type	RW	RW	RW	RW					RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0					0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	RX_DONE_DLY_INT7	RX ring #7 packet receive delay interrupt
30	RX_DONE_DLY_INT6	RX ring #6 packet receive delay interrupt
29	RX_DONE_DLY_INT5	RX ring #5 packet receive delay interrupt
28	RX_DONE_DLY_INT4	RX ring #4 packet receive delay interrupt
27	RX_DONE_DLY_INT3	RX ring #3 packet receive delay interrupt
26	RX_DONE_DLY_INT2	RX ring #2 packet receive delay interrupt
25	RX_DONE_DLY_INT1	RX ring #1 packet receive delay interrupt
24	RX_DONE_DLY_INT0	RX ring #0 packet receive delay interrupt
23	RX_DONE_INT7	RX ring #7 packet receive interrupt
22	RX_DONE_INT6	RX ring #6 packet receive interrupt
21	RX_DONE_INT5	RX ring #5 packet receive interrupt
20	RX_DONE_INT4	RX ring #4 packet receive interrupt
19	RX_DONE_INT3	RX ring #3 packet receive interrupt
18	RX_DONE_INT2	RX ring #2 packet receive interrupt
17	RX_DONE_INT1	RX ring #1 packet receive interrupt
16	RX_DONE_INT0	RX ring #0 packet receive interrupt
15	RX_COHERENT	RX_DMA finds data coherent event while checking DDONE bit.
14	RX_DLY_INT	Summary of the whole ADMA RX related interrupts.
13	TX_COHERENT	TX_DMA finds data coherent event while checking DDONE bit.
12	TX_DLY_INT	Summary of the whole ADMA TX related interrupts.
7	TX_DONE_DLY_INT3	TX ring #3 packet transmit delay interrupt
6	TX_DONE_DLY_INT2	TX ring #2 packet transmit delay interrupt
5	TX_DONE_DLY_INT1	TX ring #1 packet transmit delay interrupt
4	TX_DONE_DLY_INT0	TX ring #0 packet transmit delay interrupt
3	TX_DONE_INT3	TX ring #3 packet transmit interrupt
2	TX_DONE_INT2	TX ring #2 packet transmit interrupt
1	TX_DONE_INT1	TX ring #1 packet transmit interrupt
0	TX_DONE_INT0	TX ring #0 packet transmit interrupt

15106230 ADMA TX DBG MONO ADMA TX Debug Monitor 0 00000090

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

15106234 **ADMA TX DBG MON1** **ADMA TX Debug Monitor 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

15106238 **ADMA RX DBG MON0** **ADMA RX Debug Monitor 0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

1510623C ADMA_RX_DBG_MON1 ADMA RX Debug Monitor 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

15106240 ADMA_INT_STS_GRP0 ADMA Interrupt Status Group 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ADMA_INT_STS_GRP0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ADMA_INT_STS_GRP0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	ADMA_INT_STS_GRP0	Interrupt group 0 status, this information already "and" with "~ADMA_INT_GRP1 & ~ADMA_INT_GRP2" Each bit definition is same as "ADMA_INT_STATUS"

15106244 ADMA_INT_STS_GRP1 ADMA Interrupt Status Group 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ADMA_INT_STS_GRP1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ADMA_INT_STS_GRP1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	ADMA_INT_STS_GRP1	Interrupt group 1 status, this information already "and" with "ADMA_INT_GRP1" Each bit definition is same as "ADMA_INT_STATUS"

15106248 ADMA_INT_STS_GRP2 ADMA Interrupt Status Group 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ADMA_INT_STS_GRP2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ADMA_INT_STS_GRP2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	ADMA_INT_STS_GRP2	Interrupt group 2 status, this information already "and" with "ADMA_INT_GRP2" Each bit definition is same as "ADMA_INT_STATUS"

1510624C ADMA_INT_STS_GRP3 ADMA Interrupt Status Group 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ADMA_INT_STS_GRP3															

Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ADMA_INT_STS_GRP3															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	ADMA_INT_STS_GRP3	Interrupt group 3 status, this information already "and" with "ADMA_INT_GRP3" Each bit definition is same as "ADMA_INT_STATUS"

15106250 ADMA_INT_GRP1 ADMA Interrupt Group 1 Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ADMA_INT_GRP1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ADMA_INT_GRP1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	ADMA_INT_GRP1	Interrupt group 1 assignment. Each bit's definition is same as "ADMA_INT_STATUS"

15106254 ADMA_INT_GRP2 ADMA Interrupt Group 2 Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ADMA_INT_GRP2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	ADMA_INT_GRP2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	ADMA_INT_GRP2	Interrupt group 2 assignment. Each bit's definition is same as "ADMA_INT_STATUS"

15106258 ADMA_INT_GRP3 ADMA Interrupt Group 3 Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ADMA_INT_GRP3															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ADMA_INT_GRP3															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	ADMA_INT_GRP3	Interrupt group 3 assignment. Each bit's definition is same as "ADMA_INT_STATUS"

15106260 ADMA_BUS_CFG ADMA AXI BUS Configuration 00000400

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						AXI_CTL_UPDATED	AXI_R_BUSY	AXI_W_BUSY		AXI_LOCK_ERROR	AXI_ERR_RMID_SET_RQ	AXI_ERR_RMID_SET_BI_RQ	AXI Outstanding_EXTEND	AXI_QOS_ON		AXI_CFG_DISABLE

Type						RO	RO	RO		RO	RO	RO	RW	RW		RW
Reset						1	0	0		0	0	0	0	0		0

Bit(s)	Name	Description
10	AXI_CTRL_UPDATED	Master interface control signal updated status
9	AXI_R_BUSY	Read transaction not completes
8	AXI_W_BUSY	Write transaction not completes
6	AXI_LOCK_ERROR	Detects lock error
5	AXI_ERRMID_SET_RIRQ	Detects error MID from slave in R channel
4	AXI_ERRMID_SET_BIRQ	Detects error MID from slave in B channel
3	AXI_OUTSTANDING_EXTEND	Auto adds extra outstanding for QoS command
2	AXI_QOS_ON	Enable QoS function
0	AXI_CG_DISABLE	Disable auto clock gating of AXI component

15106264 ADMA_ULTRA_CFG ADMA AXI ULTRA Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AXI_ULTRA_EN					AXI_ULTRA_THRES										
Type	RW					RW										
Reset	0					0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AXI_PREULTRA_EN					AXI_PREULTRA_THRES										
Type	RW					RW										
Reset	0					0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	AXI_ULTRA_EN	Enable AXI Ultra transaction
26:16	AXI_ULTRA_THRES	AXI Ultra threshold. If CDM TX free FIFO count bigger than AXI_ULTRA_THRES, will trigger AXI Ultra transaction when AXI_ULTRA_EN = 1.
15	AXI_PREULTRA_EN	Enable AXI Pre-ultra transaction
10:0	AXI_PREULTRA_THRES	AXI Pre-ultra threshold. If CDM TX free FIFO count bigger than AXI_PREULTRA_THRES, will trigger AXI Pre-ultra transaction when AXI_PREULTRA_EN = 1.

15106280 ADMA_SCH_Q01_CFG ADMA Scheduler Configuration for Q0&Q1 5C004C00

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_BKT_SIZE1	MAX_RATE_ULMT1	MAX_WEIGHT1		MIN_RATE_RATIO1		MAX_RATE1									
Type	RW	RW	RW		RW		RW									
Reset	0	1	0	1	1	1	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_BKT_SIZE0	MAX_RATE_ULMT0	MAX_WEIGHT0		MIN_RATE_RATIO0		MAX_RATE0									
Type	RW	RW	RW		RW		RW									
Reset	0	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MAX_BKT_SIZE1	Maximum bucket size
30	MAX_RATE_ULMT1	Maximum rate limitation
29:28	MAX_WEIGHT1	Define the auto-reload bucket size if MAX_RATE_ULMT is set to 1. It is also served as excess bandwidth allocation ratio for servicing queue
27:26	MIN_RATE_RATIO1	Define the guaranteed Min rate based on MAX_RATE
25:16	MAX_RATE1	Define the limited Max rate for queue if MAX_RATE_ULMT is 0. The value specified represents the amount of 4-byte quota to be added into the queue #1 bucket per 125us. For example: If 512 is programmed, then the max rate limited is : $512 * 4 \text{ bytes}/125\text{us} = 16.384\text{M bytes/sec}$ or 131Mbps
15	MAX_BKT_SIZE0	Maximum bucket size
14	MAX_RATE_ULMT0	Maximum rate limitation
13:12	MAX_WEIGHT0	Define the auto-reload bucket size if MAX_RATE_ULMT is set to 1. It is also served as excess bandwidth allocation ratio for servicing queue
11:10	MIN_RATE_RATIO0	Define the guaranteed Min rate based on MAX_RATE
9:0	MAX_RATE0	Define the limited Max rate for queue if MAX_RATE_ULMT is 0. The value specified represents the amount of 4-byte quota to be added into the queue #1 bucket per 125us. For example: If 512 is programmed, then the max rate limited is : $512 * 4 \text{ bytes}/125\text{us} = 16.384\text{M bytes/sec}$ or 131Mbps

15106284 ADMA SCH Q23 CFG ADMA Scheduler Configuration for Q2&Q3 7C006C00

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_BKT_SIZE3	MAX_RATE_ULMT3	MAX_WEIGHT3		MIN_RATE_RATIO3		MAX_RATE3									
Type	RW	RW	RW		RW		RW									
Reset	0	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_BKT_SIZE3	MAX_RATE_ULMT3	MAX_WEIGHT3		MIN_RATE_RATIO3		MAX_RATE2									
Type	RW	RW	RW		RW		RW									
Reset	0	1	1	0	1	1	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MAX_BKT_SIZE3	Maximum bucket size
30	MAX_RATE_ULMT3	Maximum rate limitation
29:28	MAX_WEIGHT3	Define the auto-reload bucket size if MAX_RATE_ULMT is set to 1. It is also served as excess bandwidth allocation ratio for servicing queue
27:26	MIN_RATE_RATIO3	Define the guaranteed Min rate based on MAX_RATE
25:16	MAX_RATE3	Define the limited Max rate for queue if MAX_RATE_ULMT is 0. The value specified represents the amount of 4-byte quota to be added into the queue #1 bucket per 125us. For example: If 512 is programmed, then the max rate limited is : $512 * 4 \text{ bytes}/125\text{us} = 16.384\text{M bytes/sec}$ or 131Mbps
15	MAX_BKT_SIZE2	Maximum bucket size
14	MAX_RATE_ULMT2	Maximum rate limitation
13:12	MAX_WEIGHT2	Define the auto-reload bucket size if MAX_RATE_ULMT is set to 1. It is also served as excess bandwidth allocation ratio for servicing queue
11:10	MIN_RATE_RATIO2	Define the guaranteed Min rate based on MAX_RATE
9:0	MAX_RATE2	Define the limited Max rate for queue if MAX_RATE_ULMT is 0. The value specified represents the amount of 4-byte quota to be added into the queue #1 bucket per 125us. For example: If 512 is programmed, then the max rate limited is : $512 * 4 \text{ bytes}/125\text{us} = 16.384\text{M bytes/sec}$ or 131Mbps

15106290 ADMA_INT_STATUS_0 ADMA Interrupt Status 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	INT_STATUS															
Type	W1C															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	INT_STATUS															
Type	W1C															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	INT_STATUS	Interrupt Status

Bit(s)	Name	Description
		Bitmap same as ADMA_INT_STATUS

15106294 ADMA_INT_MASK_0 ADMA Interrupt Mask 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	INT_MASK															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	INT_MASK															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	INT_MASK	Interrupt Mask Bitmap same as ADMA_INT_MASK

15106298 ADMA_INT_STATUS_1 ADMA Interrupt Status 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	INT_STATUS															
Type	W1C															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	INT_STATUS															
Type	W1C															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	INT_STATUS	Interrupt Status Bitmap same as ADMA_INT_STATUS

1510629C ADMA_INT_MASK_1 ADMA Interrupt Mask 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	INT_MASK															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	INT_MASK															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	INT_MASK	Interrupt Mask Bitmap same as ADMA_INT_MASK

151062A0 ADMA_INT_STATUS_2 ADMA Interrupt Status 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	INT_STATUS															
Type	W1C															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	INT_STATUS															
Type	W1C															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	INT_STATUS	Interrupt Status Bitmap same as ADMA_INT_STATUS

151062A4 ADMA_INT_MASK_2 ADMA Interrupt Mask 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	INT_MASK															
Type	RW															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	INT_MASK															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	INT_MASK	Interrupt Mask Bitmap same as ADMA_INT_MASK

151062A8 ADMA_INT_STATUS_3 ADMA Interrupt Status 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	INT_STATUS															
Type	W1C															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	INT_STATUS															
Type	W1C															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	INT_STATUS	Interrupt Status Bitmap same as ADMA_INT_STATUS

151062AC ADMA_INT_MASK_3 ADMA Interrupt Mask 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	INT_MASK															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	INT_MASK															

Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	INT_MASK	Interrupt Mask Bitmap same as ADMA_INT_MASK

151062B0 ADMA_TX_DELAY_INT_CFG_0ADMA Tx Delay Interrupt Configuration 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RING1_TXDLY_INT_EN	RING1_TXMAX_PINT								RING1_TXMAX_PTIME						
Type	RW	RW								RW						
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RING0_TXDLY_INT_EN	RING0_TXMAX_PINT								RING0_TXMAX_PTIME						
Type	RW	RW								RW						
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	RING1_TXDLY_INT_EN	Enable delay interrupt mechanism for Tx Ring 1
30:24	RING1_TXMAX_PINT	Specified Max. number of pended interrupts [Note] reset to 0 can disable pending interrupt count check.
23:16	RING1_TXMAX_PTIME	Specified Max. pended time [Note] reset to 0 can disable pending interrupt time check.
15	RING0_TXDLY_INT_EN	Enable delay interrupt mechanism for Tx Ring 0
14:8	RING0_TXMAX_PINT	Specified Max. number of pended interrupts [Note] reset to 0 can disable pending interrupt count check.
7:0	RING0_TXMAX_PTIME	Specified Max. pended time [Note] reset to 0 can disable pending interrupt time check.

151062B4 ADMA_TX_DELAY_INT_CFG_1ADMA Tx Delay Interrupt Configuration 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RING3_TXDLY_INT_EN	RING3_TXMAX_PINT								RING3_TXMAX_PTIME						

Type	RW	RW							RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RING2_TXDLY_INT_EN	RING2_TXMAX_PINT							RING2_TXMAX_PTIME							
Type	RW	RW							RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	RING3_TXDLY_INT_EN	Enable delay interrupt mechanism for Tx Ring 3
30:24	RING3_TXMAX_PINT	Specified Max. number of pended interrupts [Note] reset to 0 can disable pending interrupt count check.
23:16	RING3_TXMAX_PTIME	Specified Max. pended time [Note] reset to 0 can disable pending interrupt time check.
15	RING2_TXDLY_INT_EN	Enable delay interrupt mechanism for Tx Ring 2
14:8	RING2_TXMAX_PINT	Specified Max. number of pended interrupts [Note] reset to 0 can disable pending interrupt count check.
7:0	RING2_TXMAX_PTIME	Specified Max. pended time [Note] reset to 0 can disable pending interrupt time check.

151062C0 ADMA_RX_DELAY_INT_CFG ADMA Rx Delay Interrupt Configuration 0 00000000
0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RING_4_7_RXDLY_INT_EN	RING_4_7_RXMAX_PINT							RING_4_7_RXMAX_PTIME							
Type	RW	RW							RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RING_0_3_RXDLY_INT_EN	RING_0_3_RXMAX_PINT							RING_0_3_RXMAX_PTIME							
Type	RW	RW							RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	RING_4_7_RXDLY_INT_EN	Enable delay interrupt mechanism for Rx Ring 4~7
30:24	RING_4_7_RXMAX_PINT	Specified Max. number of pended interrupts for Rx Ring 4~7 [Note] Reset to 0 can disable pending interrupt count check.
23:16	RING_4_7_RXMAX_PTIME	Specified Max. pended time for Rx Ring 4~7 [Note] Reset to 0 can disable pending interrupt time check.
15	RING_0_3_RXDLY_INT_EN	Enable delay interrupt mechanism for Rx Ring 0~3
14:8	RING_0_3_RXMAX_PINT	Specified Max. number of pended interrupts for Rx Ring 0~3 [Note] Reset to 0 can disable pending interrupt count check.
7:0	RING_0_3_RXMAX_PTIME	Specified Max. pended time for Rx Ring 0~3 [Note] Reset to 0 can disable pending interrupt time check.

151062C8 ADMA_RX_FC_CFG_0 ADMA Rx Flow Control Configuration 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

151062CC ADMA_RX_FC_CFG_1 ADMA Rx Flow Control Configuration 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

15106400 LRO2_ALT_TIMER Reserved 000FFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

15106408 LRO2_CTRL_DW0 Control CRs F0884000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RING_RELINGUISH_DONE				RING_RELINGUISH_REQ				cr_l4_c trl_psh _en	lro_crs n_bnw	cr_alt score_ mode	first_in eligible _pkt_r edirect _en	L3_CKS _UPD_ EN	SDL		
Type	RO				RW				RW	RW	RW	RW	RW	RW		
Reset	1	1	1	1	0	0	0	0	1	0	0	0	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SDL												MULTI PLE_N ON_RI NG_EN	IPv6_E N	EN	
Type	RW													RW	RW	RW
Reset	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:28	RING_RELINGUISH_DONE	it represent has relinquished rings
27:24	RING_RELINGUISH_REQ	FW request to flush aggregated packets by writing 1, then 0

Bit(s)	Name	Description
23	cr_l4_ctrl_psh_en	lro_crsn_bnw In order to save one LRO RXD with large sdl0(64KB), it is better to redirect ineligible packet into Normal ring when the hit LRO ring is clean and empty without existed aggregated packets.
22	lro_crsn_bnw	
21	cr_alt_score_mode	
20	first_ineligible_pkt_redirect_en	
19	L3_CKS_UPD_EN	ipv4 checksum update enable
18:3	SDL	max aggregated packet length
2	MULTIPLE_NON_RING_EN	To enable multiple non-LRO Rx rings
1	IPv6_EN	enable bit for IPv6 packet LRO
0	EN	enable bit to activate RX LRO feature

1510640C LRO2_CTRL_DW1 Control CRs 1F1E1F1E

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CPU_REASON															
Type	RW															
Reset	0	0	0	1	1	1	1	1	0	0	0	1	1	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CPU_REASON															
Type	RW															
Reset	0	0	0	1	1	1	1	1	0	0	0	1	1	1	1	0

Bit(s)	Name	Description
31:0	CPU_REASON	

15106410 LRO2_CTRL_DW2 Control CRs 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AUTO_LEARN_ELIGIBLE_THRESHOLD															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUTO_LEARN_ELIGIBLE_THRESHOLD															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	AUTO_LEARN_ELIGIBLE_THRESHOLD	min threshold to become a candidate for LRO aggregation

15106414 LRO2_CTRL_DW3 Control CRs 05F20F00

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_RXD_SDL0															
Type	RW															
Reset	0	0	0	0	0	1	0	1	1	1	1	1	0	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CAND_WGT_IDX		VLAN_VID_CMP_DEPTH		VLAN_EN				REV							
Type	RW		RW		RW				RW							
Reset	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	MIN_RXD_SDL0	The least remaining room of SDL0 in RXD for LRO aggregation. It should be greater than the maximum size of packet which RX MAC can accept without dropping. That is, MIN_RXD_SDL0 MUST be equal or greater than MAX_RX_JUMBO/MAC_RX_PKT_LEN fields in CR MAC_P*_MCR(address : 1B11_0100)
15:14	CAND_WGT_IDX	Candidate weight index the estimated candidate weight value = throughput >> {CAND_WGT_IDX,1'b0}
13:12	VLAN_VID_CMP_DEPTH	determine how many depth of VLAN ID need to be compared
11:8	VLAN_EN	support max 4-depth VLAN for LRO
7:0	REV	

15106418 LRO2_CTRL_DW4 Control CRs 00008100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV															SPC_TAG_EN
Type	RW															RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EXT_TPID															

Type	RW															
Reset	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:17	REV	
16	SPC_TAG_EN	special tag enable
15:0	EXT_TPID	user extended TPID

1510641C LRO2 ALT SCORE DELTA 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ALT_SCORE_DELTA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ALT_SCORE_DELTA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	ALT_SCORE_DELTA	To add a delta before determine whether replace or not!

15106420 LRO2 TIMEOUT FLAG 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REVO															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REVO							AGE_TIMEOUT				AGG_TIMEOUT				BUSY
Type	RO							RC				RC				RC
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:9	REV0	
8:5	AGE_TIMEOUT	If the ring time out, the related bit will be on. After CR reading, the bit will be cleared.
4:1	AGG_TIMEOUT	If the ring time out, the related bit will be on. After CR reading, the bit will be cleared.
0	BUSY	LRO busy

15106430 LRO2_RING1_STS LRO2 Ring1 Status 00000100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV							AGG_CNT_ZERO	AGG_CNT							
Type	RO							RO	RO							
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:9	REV	
8	AGG_CNT_ZERO	
7:0	AGG_CNT	

15106434 LRO2_RING2_STS LRO2 Ring2 Status 00000100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV							AGG_CNT_ZERO	AGG_CNT							
Type	RO							RO	RO							

Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:9	REV	
8	AGG_CNT_ZERO	
7:0	AGG_CNT	

15106438 LRO2_RING3_STS LRO2 Ring3 Status 00000100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV							AGG_CNT_ZERO	AGG_CNT							
Type	RO							RO	RO							
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:9	REV	
8	AGG_CNT_ZERO	
7:0	AGG_CNT	current aggregated packet count number

1510643C LRO2_RING4_STS LRO2 Ring4 Status 00000100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV							AGG_CNT_ZERO	AGG_CNT							
Type	RO							RO	RO							

Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:9	REV	
8	AGG_CNT_ZERO	
7:0	AGG_CNT	current aggregated packet count number

15106440 **LRO2_ALT_DBG** **LRO2 ALT debug** **00000100**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

15106444 **LRO2_ALT_DBG_DATA** **LRO2 ALT debug data** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

15106450 LRO2_RING1_STP_DTP_DW Source TCP port number 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	STP															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DTP															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	STP	Source TCP port number
15:0	DTP	Destination TCP port number

15106454 LRO2_RING1_DIP_DW0 Destination IP address[31:0] 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DATA	Destination IP address[31:0]

15106458 LRO2_RING1_DIP_DW1 Destination IP address[63:32] 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DATA															

Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DATA	Destination IP address[63:32]

1510645C LRO2_RING1_DIP_DW2 Destination IP address[95:64] 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DATA	Destination IP address[95:64]

15106460 LRO2_RING1_DIP_DW3 Destination IP address[127:96] 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA															

Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DATA	Destination IP address[127:96]

15106464 LRO2_RING1_SIP_DW0 Source IP address[31:0] 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DATA	Source IP address[31:0]

15106468 LRO2_RING1_SIP_DW1 Source IP address[63:32] 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DATA	Source IP address[63:32]

1510646C LRO2_RING1_SIP_DW2 Source IP address[95:64] 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DATA	Source IP address[95:64]

15106470 LRO2_RING1_SIP_DW3 Source IP address[127:96] 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DATA	Source IP address[127:96]

15106474 LRO2_RING1_CTRL_DW0 l2_vlan_vid_l2_l 00000002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	VLAN_VID_L2_L								VLAN_VID_L1							
Type	RW								RW							

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VLAN_VID_L1		VLAN_VID_L0												FRCP_I PV4_E N	FRCP_I PV6_E N
Type	RW		RW												RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bit(s)	Name	Description
31:26	VLAN_VID_L2_L	VLAN VID of four forced port LRO rings
25:14	VLAN_VID_L1	To validate IPv4 flow of forced port LRO ring
13:2	VLAN_VID_L0	To validate IPv4 flow of forced port LRO ring
1	FRCP_IPV4_EN	To validate IPv4 flow of forced port LRO ring
0	FRCP_IPV6_EN	To validate IPv6 flow of forced port LRO ring

15106478 LRO2_RING1_CTRL_DW1 RX ring age time[9:0] FFC00000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AGE_TIME_L										VLAN_VLD_L3	VLAN_VLD_L2	VLAN_VLD_L1	VLAN_VLD_L0	VLAN_VID_L3	
Type	RW										RW	RW	RW	RW	RW	
Reset	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VLAN_VID_L3										VLAN_VID_L2_H					
Type	RW										RW					
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:22	AGE_TIME_L	age time to flush LRO ring
21	VLAN_VLD_L3	valid bit of VLAN VID for four forced port LRO ring
20	VLAN_VLD_L2	valid bit of VLAN VID for four forced port LRO ring
19	VLAN_VLD_L1	valid bit of VLAN VID for four forced port LRO ring
18	VLAN_VLD_L0	valid bit of VLAN VID for four forced port LRO ring
17:6	VLAN_VID_L3	VLAN VID of four forced port LRO rings
5:0	VLAN_VID_L2_H	VLAN VID of four forced port LRO rings

1510647C LRO2_RING1_CTRL_DW2 LRO2_MAX_AGGREGATED_CNT_L 03FFFCBF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	MAX_AGGREGATED_CNT_L						MAX_AGG_TIME									
Type	RW						RW									
Reset	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_AGG_TIME						MYIP_VLD	VLD	OP_MODE		AGE_TIME_H					
Type	RW						RW	RW	RW		RW					
Reset	1	1	1	1	1	1	0	0	1	0	1	1	1	1	1	1

Bit(s)	Name	Description
31:26	MAX_AGGREGATED_CNT_L	to limit max aggregated packets
25:10	MAX_AGG_TIME	Maximum aggregation time to flush, = 0 to disable flush
9	MYIP_VLD	To validate programmed DIP information
8	VLD	To validate programmed flow information
7:6	OP_MODE	00 : normal, 01 : PSE, 10 : forced_port, 11 : auto_learn
5:0	AGE_TIME_H	Age time to flush LRO ring, = 0 to disable flush

15106480 LRO2_RING1_CTRL_DW3 Reserved 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV															MAX_AGGREGATED_CNT_H
Type	RO															RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
31:2	REV	to limit max aggregated packets
1:0	MAX_AGGREGATED_CNT_H	to limit max aggregated packets

15106490 LRO2_RING2_STP_DTP_DW Source TCP port number 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	STP															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DTP															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	STP	Source TCP port number
15:0	DTP	Destination TCP port number

15106494 LRO2_RING2_DIP_DW0 Destination IP address[31:0] 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DATA	Destination IP address[31:0]

15106498 LRO2_RING2_DIP_DW1 Destination IP address[63:32] 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DATA	Destination IP address[63:32]

1510649C LRO2_RING2_DIP_DW2 Destination IP address[95:64] 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DATA	Destination IP address[95:64]

151064A0 LRO2_RING2_DIP_DW3 Destination IP address[127:96] 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DATA	Destination IP address[127:96]

151064A4 LRO2_RING2_SIP_DW0 Source IP address[31:0] 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DATA	Source IP address[31:0]

151064A8 LRO2_RING2_SIP_DW1 Source IP address[63:32] 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DATA	Source IP address[63:32]

151064AC LRO2_RING2_SIP_DW2 Source IP address[95:64] 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DATA	Source IP address[95:64]

151064B0 LRO2_RING2_SIP_DW3 Source IP address[127:96] 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DATA	Source IP address[127:96]

151064B4 LRO2_RING2_CTRL_DW0 l2_vlan_vid_l2_l 00000002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	VLAN_VID_L2_L								VLAN_VID_L1							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	VLAN_VID_L1		VLAN_VID_L0												FRCP_I PV4_E N	FRCP_I PV6_E N
Type	RW		RW												RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bit(s)	Name	Description
31:26	VLAN_VID_L2_L	VLAN VID of four forced port LRO rings
25:14	VLAN_VID_L1	To validate IPv4 flow of forced port LRO ring
13:2	VLAN_VID_L0	To validate IPv4 flow of forced port LRO ring
1	FRCP_IPV4_EN	To validate IPv4 flow of forced port LRO ring
0	FRCP_IPV6_EN	To validate IPv6 flow of forced port LRO ring

151064B8 LRO2_RING2_CTRL_DW1 RX ring age time[9:0] FFC00000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AGE_TIME_L										VLAN_VLD_L3	VLAN_VLD_L2	VLAN_VLD_L1	VLAN_VLD_L0	VLAN_VID_L3	
Type	RW										RW	RW	RW	RW	RW	
Reset	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VLAN_VID_L3										VLAN_VID_L2_H					
Type	RW										RW					
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:22	AGE_TIME_L	age time to flush LRO ring
21	VLAN_VLD_L3	valid bit of VLAN VID for four forced port LRO ring
20	VLAN_VLD_L2	valid bit of VLAN VID for four forced port LRO ring
19	VLAN_VLD_L1	valid bit of VLAN VID for four forced port LRO ring
18	VLAN_VLD_L0	valid bit of VLAN VID for four forced port LRO ring
17:6	VLAN_VID_L3	VLAN VID of four forced port LRO rings
5:0	VLAN_VID_L2_H	VLAN VID of four forced port LRO rings

151064BC LRO2_RING2_CTRL_DW2 LRO2_MAX_AGGREGATED_CNT_L 03FFFCBF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_AGGREGATED_CNT_L										MAX_AGG_TIME					
Type	RW										RW					

Reset	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_AGG_TIME						MYIP_VLD	VLD	OP_MODE		AGE_TIME_H					
Type	RW						RW	RW	RW		RW					
Reset	1	1	1	1	1	1	0	0	1	0	1	1	1	1	1	1

Bit(s)	Name	Description
31:26	MAX_AGGREGATED_CNT_L	to limit max aggregated packets
25:10	MAX_AGG_TIME	Maximum aggregation time to flush, =0 to disable flush
9	MYIP_VLD	To validate programmed DIP information
8	VLD	To validate programmed flow information
7:6	OP_MODE	00 : normal, 01 : PSE, 10 : forced_port, 11 : auto_learn
5:0	AGE_TIME_H	Age time to flush LRO ring, = 0 to disable flush

151064C0 LRO2_RING2_CTRL_DW3 Reserved 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV														MAX_AGGREGATED_CNT_H	
Type	RO														RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
31:2	REV	to limit max aggregated packets
1:0	MAX_AGGREGATED_CNT_H	to limit max aggregated packets

151064D0 LRO2_RING3_STP_DTP_DW Source TCP port number 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	STP															
Type	RW															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DTP															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	STP	Source TCP port number
15:0	DTP	Destination TCP port number

151064D4 LRO2_RING3_DIP_DW0 Destination IP address[31:0] 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DATA	Destination IP address[31:0]

151064D8 LRO2_RING3_DIP_DW1 Destination IP address[63:32] 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA															
Type	RW															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DATA	Destination IP address[63:32]

151064DC LRO2_RING3_DIP_DW2 Destination IP address[95:64] 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DATA	Destination IP address[95:64]

151064E0 LRO2_RING3_DIP_DW3 Destination IP address[127:96] 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DATA	Destination IP address[127:96]

151064E4 LRO2_RING3 SIP DW0 Source IP address[31:0] 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DATA	Source IP address[31:0]

151064E8 LRO2_RING3 SIP DW1 Source IP address[63:32] 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DATA	Source IP address[63:32]

151064EC LRO2_RING3 SIP DW2 Source IP address[95:64] 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DATA	Source IP address[95:64]

151064F0 LRO2_RING3_SIP_DW3 Source IP address[127:96] 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DATA	Source IP address[127:96]

151064F4 LRO2_RING3_CTRL_DW0 l2_vlan_vid_l2_l 00000002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	VLAN_VID_L2_L								VLAN_VID_L1							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VLAN_VID_L1		VLAN_VID_L0												FRCP_I PV4_E N	FRCP_I PV6_E N
Type	RW		RW												RW	RW

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bit(s)	Name	Description
31:26	VLAN_VID_L2_L	VLAN VID of four forced port LRO rings
25:14	VLAN_VID_L1	To validate IPv4 flow of forced port LRO ring
13:2	VLAN_VID_L0	To validate IPv4 flow of forced port LRO ring
1	FRCP_IPV4_EN	To validate IPv4 flow of forced port LRO ring
0	FRCP_IPV6_EN	To validate IPv6 flow of forced port LRO ring

151064F8 LRO2_RING3_CTRL_DW1 RX ring age time[9:0] FFC00000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AGE_TIME_L										VLAN_VLD_L3	VLAN_VLD_L2	VLAN_VLD_L1	VLAN_VLD_L0	VLAN_VID_L3	
Type	RW										RW	RW	RW	RW	RW	
Reset	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VLAN_VID_L3										VLAN_VID_L2_H					
Type	RW										RW					
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:22	AGE_TIME_L	age time to flush LRO ring
21	VLAN_VLD_L3	valid bit of VLAN VID for four forced port LRO ring
20	VLAN_VLD_L2	valid bit of VLAN VID for four forced port LRO ring
19	VLAN_VLD_L1	valid bit of VLAN VID for four forced port LRO ring
18	VLAN_VLD_L0	valid bit of VLAN VID for four forced port LRO ring
17:6	VLAN_VID_L3	VLAN VID of four forced port LRO rings
5:0	VLAN_VID_L2_H	VLAN VID of four forced port LRO rings

151064FC LRO2_RING3_CTRL_DW2 LRO2_MAX_AGGREGATED_CNT_L 03FFFCBF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_AGGREGATED_CNT_L										MAX_AGG_TIME					
Type	RW										RW					
Reset	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	MAX_AGG_TIME						MYIP_VLD	VLD	OP_MODE		AGE_TIME_H					
Type	RW						RW	RW	RW		RW					
Reset	1	1	1	1	1	1	0	0	1	0	1	1	1	1	1	1

Bit(s)	Name	Description
31:26	MAX_AGGREGATED_CNT_L	to limit max aggregated packets
25:10	MAX_AGG_TIME	Maximum aggregation time to flush, = 0 to disable flush
9	MYIP_VLD	To validate programmed DIP information
8	VLD	To validate programmed flow information
7:6	OP_MODE	00 : normal, 01 : PSE, 10 : forced_port, 11 : auto_learn
5:0	AGE_TIME_H	Age time to flush LRO ring, = 0 to disable flush

15106500 LRO2_RING3_CTRL_DW3 Reserved 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV														MAX_AGGREGATED_CNT_H	
Type	RO														RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
31:2	REV	to limit max aggregated packets
1:0	MAX_AGGREGATED_CNT_H	to limit max aggregated packets

15106510 LRO2_RING4_STP_DTP_DW Source TCP port number 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	STP															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	DTP															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	STP	Source TCP port number
15:0	DTP	Destination TCP port number

15106514 LRO2_RING4_DIP_DW0 Destination IP address[31:0] 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DATA	Destination IP address[31:0]

15106518 LRO2_RING4_DIP_DW1 Destination IP address[63:32] 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DATA	Destination IP address[63:32]

1510651C LRO2 RING4 DIP DW2 Destination IP address[95:64] 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DATA	Destination IP address[95:64]

15106520 LRO2 RING4 DIP DW3 Destination IP address[127:96] 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DATA	Destination IP address[127:96]

15106524 LRO2 RING4 SIP DW0 Source IP address[31:0] 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DATA	Source IP address[31:0]

15106528 LRO2_RING4_SIP_DW1 Source IP address[63:32] 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DATA	Source IP address[63:32]

1510652C LRO2_RING4_SIP_DW2 Source IP address[95:64] 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DATA	Source IP address[95:64]

15106530 LRO2_RING4 SIP DW3 Source IP address[127:96] 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DATA	Source IP address[127:96]

15106534 LRO2_RING4 CTRL DW0 l2_vlan_vid_l2_l 00000002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	VLAN_VID_L2_L								VLAN_VID_L1							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VLAN_VID_L1														FRCP_I PV4_E N	FRCP_I PV6_E N
Type	RW														RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bit(s)	Name	Description
31:26	VLAN_VID_L2_L	VLAN VID of four forced port LRO rings
25:14	VLAN_VID_L1	To validate IPv4 flow of forced port LRO ring
13:2	VLAN_VID_L0	To validate IPv4 flow of forced port LRO ring
1	FRCP_IPV4_EN	To validate IPv4 flow of forced port LRO ring
0	FRCP_IPV6_EN	To validate IPv6 flow of forced port LRO ring

15106538 LRO2_RING4_CTRL_DW1 RX ring age time[9:0] FFC00000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AGE_TIME_L										VLAN_VLD_L3	VLAN_VLD_L2	VLAN_VLD_L1	VLAN_VLD_L0	VLAN_VID_L3	
Type	RW										RW	RW	RW	RW	RW	
Reset	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VLAN_VID_L3										VLAN_VID_L2_H					
Type	RW										RW					
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:22	AGE_TIME_L	age time to flush LRO ring
21	VLAN_VLD_L3	valid bit of VLAN VID for four forced port LRO ring
20	VLAN_VLD_L2	valid bit of VLAN VID for four forced port LRO ring
19	VLAN_VLD_L1	valid bit of VLAN VID for four forced port LRO ring
18	VLAN_VLD_L0	valid bit of VLAN VID for four forced port LRO ring
17:6	VLAN_VID_L3	VLAN VID of four forced port LRO rings
5:0	VLAN_VID_L2_H	VLAN VID of four forced port LRO rings

1510653C LRO2_RING4_CTRL_DW2 LRO2_MAX_AGGREGATED_CNT_L 03FFFCBF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_AGGREGATED_CNT_L										MAX_AGG_TIME					
Type	RW										RW					
Reset	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_AGG_TIME										MYIP_VLD	VLD	OP_MODE	AGE_TIME_H		
Type	RW										RW	RW	RW	RW		

Reset	1	1	1	1	1	1	0	0	1	0	1	1	1	1	1	1

Bit(s)	Name	Description
31:26	MAX_AGGREGATED_CNT_L	to limit max aggregated packets
25:10	MAX_AGG_TIME	Maximum aggregation time to flush, = 0 to disable flush
9	MYIP_VLD	To validate programmed DIP information
8	VLD	To validate programmed flow information
7:6	OP_MODE	00 : normal, 01 : PSE, 10 : forced_port, 11 : auto_learn
5:0	AGE_TIME_H	Age time to flush LRO ring, = 0 to disable flush

15106540 LRO2_RING4_CTRL_DW3 Reserved 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV														MAX_AGGREGATED_CNT_H	
Type	RO														RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
31:2	REV	to limit max aggregated packets
1:0	MAX_AGGREGATED_CNT_H	to limit max aggregated packets

15106800 RSS2_GLO_CFG RSS Global Configuration 1F1F3370

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	IPV4_TUPLE_EN								IPV6_TUPLE_EN							
Type	RW								RW							
Reset	1								1							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IPV4_TYPE				IPV6_TYPE				INDR_TBL_SIZE				RSS_CFG_RDY	RSS_CFG_REQ	RSS_BUSY	RSS_ENABLE
Type	RW				RW				RW				RO	RW	RO	RW

Reset		0	1	1		0	1	1		1	1	1	0	0	0	0

Bit(s)	Name	Description
28:24	IPV4_TUPLE_EN	IPv4 Hash Tuple Global Enable This field controls which hash tuple is valid for IPv4 hash calculation. The invalid(disabled) tuple can be seem as 0x0 when calculating HASH. For example, when SIP is disabled, 2-tuple and 4-tuple hash will not consider SIP. Another example, when DPORT is disabled, 4-tuple hash will not consider DPORT. Bit Maps: {DPROT,SPORT,DIP,SIP,Reserved} Set the bits to 1 to enable corresponding hash tuple for hash calculation. Set the bits to 0 to disable corresponding hash tuple for hash calculation.
20:16	IPV6_TUPLE_EN	IPv6 Hash Tuple Global Enable This field controls which hash tuple is valid for IPv6 hash calculation. See description of IPV4_TUPLE_EN for more detail. Bit Maps: {DPROT,SPORT,DIP,SIP,Reserved} Set the bits to 1 to enable corresponding hash tuple for hash calculation. Set the bits to 0 to disable corresponding hash tuple for hash calculation.
14:12	IPV4_TYPE	IPv4 Hash Type Selection Flag This field controls the selection of hash 2-tuple and 4-tuple for different kinds of IPv4 packet. Bit Maps: {UDP 4-tuple,TCP4-tuple,IP 2-tuple} RSS performs the hash calculations as specified for the enabled case. For example, IPV4_TYPE=3'b011, RSS will use 4-tuple hash for IPv4 TCP packets and 2-tuple hash for IPv4 non-TCP packets (such as IPv4 fragment packet).
10:8	IPV6_TYPE	IPv6 Hash Type Selection Flag This field controls the selection of hash 2-tuple and 4-tuple for different kinds of IPv6 packet. Bit Maps: {UDP 4-tuple,TCP4-tuple,IP 2-tuple} See description of IPV4_TYPE for more detail.
6:4	INDR_TBL_SIZE	Change the size of indirection table. This register field affects how many bits of hash result will be used as the entry of indirection table. For example, INDR_TBL_SIZE=6 means RSS use only 6 bits of hash result as indirection table entry, which also means that indirection table has $2^6=64$ entries.
3	RSS_CFG_RDY	RSS is ready to accept new register configuration. This register will be asserted after RSS accepted the request from RSS_CFG_REQ. See description of RSS_CFG_REQ for more detail.
2	RSS_CFG_REQ	Request to change RSS register configuration. When Request asserted, RSS will be paused after the process of current packet has finished. It is worth to notice that assert RSS_CFG_REQ is required before enable RSS or changing other register setting(such as indirection table). Must wait RSS_CFG_RDY=1 before changing RSS register value(including RSS_ENABLE).
1	RSS_BUSY	RSS is working or not
0	RSS_ENABLE	Enable/Disable RSS

Bit(s)	Name	Description

15106804 RSS2_GLO_CFG2 RSS Global Configuration2 C000001A

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

15106808 RSS2_GLO_CFG3 RSS Global Configuration3 00008100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV															SPC_TAG_EN
Type	RW															RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EXT_TPID															
Type	RW															
Reset	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:17	REV	Reserved
16	SPC_TAG_EN	special tag enable
15:0	EXT_TPID	user extended TPID

1510680C RSS2_LFB_TIMER Low Flow Balance Timer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

15106818 RSS2_DBG_PROBE RSS DEBUG PROBE 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

15106820 RSS2_HASH_KEY_DW0 RSS hash Key DW0 BEAC01FA

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DATA															
Type	RW															
Reset	1	0	1	1	1	1	1	0	1	0	1	0	1	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0

Bit(s)	Name	Description
31:0	DATA	Hash Key bit 31~0

15106824 RSS2 HASH KEY DW1 RSS hash Key DW1 6A42B73B

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DATA															
Type	RW															
Reset	0	1	1	0	1	0	1	0	0	1	0	0	0	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA															
Type	RW															
Reset	1	0	1	1	0	1	1	1	0	0	1	1	1	0	1	1

Bit(s)	Name	Description
31:0	DATA	Hash Key bit 63~32

15106828 RSS2 HASH KEY DW2 RSS hash Key DW2 8030F20C

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DATA															
Type	RW															
Reset	1	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA															
Type	RW															
Reset	1	1	1	1	0	0	1	0	0	0	0	0	1	1	0	0

Bit(s)	Name	Description
31:0	DATA	Hash Key bit 95~64

1510682C RSS2_HASH_KEY_DW3 RSS hash Key DW3 77CB2DA3

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DATA															
Type	RW															
Reset	0	1	1	1	0	1	1	1	1	1	0	0	1	0	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA															
Type	RW															
Reset	0	0	1	0	1	1	0	1	1	0	1	0	0	0	1	1

Bit(s)	Name	Description
31:0	DATA	Hash Key bit 127~96

15106830 RSS2_HASH_KEY_DW4 RSS hash Key DW4 AE7B30B4

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DATA															
Type	RW															
Reset	1	0	1	0	1	1	1	0	0	1	1	1	1	0	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA															
Type	RW															
Reset	0	0	1	1	0	0	0	0	1	0	1	1	0	1	0	0

Bit(s)	Name	Description
31:0	DATA	Hash Key bit 159~128

15106834 RSS2_HASH_KEY_DW5 RSS hash Key DW5 D0CA2BCB

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	DATA															
Type	RW															
Reset	1	1	0	1	0	0	0	0	1	1	0	0	1	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA															
Type	RW															
Reset	0	0	1	0	1	0	1	1	1	1	0	0	1	0	1	1

Bit(s)	Name	Description
31:0	DATA	Hash Key bit 191~160

15106838 RSS2 HASH KEY DW6 RSS hash Key DW6 43A38FB0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DATA															
Type	RW															
Reset	0	1	0	0	0	0	1	1	1	0	1	0	0	0	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA															
Type	RW															
Reset	1	0	0	0	1	1	1	1	1	0	1	1	0	0	0	0

Bit(s)	Name	Description
31:0	DATA	Hash Key bit 223~192

1510683C RSS2 HASH KEY DW7 RSS hash Key DW7 4167253D

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DATA															
Type	RW															
Reset	0	1	0	0	0	0	0	1	0	1	1	0	0	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	DATA															
Type	RW															
Reset	0	0	1	0	0	1	0	1	0	0	1	1	1	1	0	1

Bit(s)	Name	Description
31:0	DATA	Hash Key bit 255~224

15106840 RSS2 HASH KEY DW8 RSS hash Key DW8 255B0EC2

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DATA															
Type	RW															
Reset	0	0	1	0	0	1	0	1	0	1	0	1	1	0	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA															
Type	RW															
Reset	0	0	0	0	1	1	1	0	1	1	0	0	0	0	1	0

Bit(s)	Name	Description
31:0	DATA	Hash Key bit 287~256

15106844 RSS2 HASH KEY DW9 RSS hash Key DW9 6D5A56DA

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DATA															
Type	RW															
Reset	0	1	1	0	1	1	0	1	0	1	0	1	1	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA															
Type	RW															
Reset	0	1	0	1	0	1	1	0	1	1	0	1	1	0	1	0

Bit(s)	Name	Description
31:0	DATA	Hash Key bit 319~288

15106850 **RSS2_INDR_TABLE_DW0** **RSS Indirection table DW0** **DEADBEEF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DATA															
Type	RW															
Reset	1	1	0	1	1	1	1	0	1	0	1	0	1	1	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA															
Type	RW															
Reset	1	0	1	1	1	1	1	0	1	1	1	0	1	1	1	1

Bit(s)	Name	Description
31:0	DATA	Indirection Table Entry 15~0 Each entry has 2bits

15106854 **RSS2_INDR_TABLE_DW1** **RSS Indirection table DW1** **DEADBEEF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DATA															
Type	RW															
Reset	1	1	0	1	1	1	1	0	1	0	1	0	1	1	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA															
Type	RW															
Reset	1	0	1	1	1	1	1	0	1	1	1	0	1	1	1	1

Bit(s)	Name	Description
31:0	DATA	Indirection Table Entry 31~16 Each entry has 2bits

15106858 **RSS2_INDR_TABLE_DW2** **RSS Indirection table DW2** **DEADBEEF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DATA															
Type	RW															
Reset	1	1	0	1	1	1	1	0	1	0	1	0	1	1	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA															
Type	RW															
Reset	1	0	1	1	1	1	1	0	1	1	1	0	1	1	1	1

Bit(s)	Name	Description
31:0	DATA	Indirection Table Entry 47~32 Each entry has 2bits

1510685C RSS2 INDR TABLE DW3 RSS Indirection table DW3 DEADBEEF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DATA															
Type	RW															
Reset	1	1	0	1	1	1	1	0	1	0	1	0	1	1	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA															
Type	RW															
Reset	1	0	1	1	1	1	1	0	1	1	1	0	1	1	1	1

Bit(s)	Name	Description
31:0	DATA	Indirection Table Entry 63~48 Each entry has 2bits

15106860 RSS2 INDR TABLE DW4 RSS Indirection table DW4 DEADBEEF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DATA															
Type	RW															

Reset	1	1	0	1	1	1	1	0	1	0	1	0	1	1	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA															
Type	RW															
Reset	1	0	1	1	1	1	1	0	1	1	1	0	1	1	1	1

Bit(s)	Name	Description
31:0	DATA	Indirection Table Entry 79~64 Each entry has 2bits

15106864 RSS2_INDR_TABLE_DW5 RSS Indirection table DW5 DEADBEEF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DATA															
Type	RW															
Reset	1	1	0	1	1	1	1	0	1	0	1	0	1	1	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA															
Type	RW															
Reset	1	0	1	1	1	1	1	0	1	1	1	0	1	1	1	1

Bit(s)	Name	Description
31:0	DATA	Indirection Table Entry 95~80 Each entry has 2bits

15106868 RSS2_INDR_TABLE_DW6 RSS Indirection table DW6 DEADBEEF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DATA															
Type	RW															
Reset	1	1	0	1	1	1	1	0	1	0	1	0	1	1	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA															

Type	RW															
Reset	1	0	1	1	1	1	1	0	1	1	1	0	1	1	1	1

Bit(s)	Name	Description
31:0	DATA	Indirection Table Entry 111~96 Each entry has 2bits

1510686C RSS2 INDR TABLE DW7 RSS Indirection table DW7 DEADBEEF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DATA															
Type	RW															
Reset	1	1	0	1	1	1	1	0	1	0	1	0	1	1	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA															
Type	RW															
Reset	1	0	1	1	1	1	1	0	1	1	1	0	1	1	1	1

Bit(s)	Name	Description
31:0	DATA	Indirection Table Entry 127~112 Each entry has 2bits

15110000 MAC PPSC PHY Polling and SMI Master Control 45000504

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PHY_A P_EN	PHY_P RE_EN	PHY_MDC_CFG						RESV0			MDC_T URBO	RESV1		EE_AN_EN	
Type	RW	RW	RW						RW			RW	RW		RW	
Reset	0	1	0	0	0	1	0	1	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESV2			PHY_END_ADDR					RESV3			PHY_START_ADDR				
Type	RW			RW					RW			RW				
Reset	0	0	0	0	0	1	0	1	0	0	0	0	0	1	0	0

Bit(s)	Name	Description
31	PHY_AP_EN	PHY auto polling enable Indicate all PHY's status will be updated to PHY's status registers by PHY polling process.
30	PHY_PRE_EN	PHY preamble enable Indicates SMI master will send preamble bits (32-bits) at each MDIO read/write transaction. [note] This bit will affect both PHY polling mode and PHY indirect access mode.
29:24	PHY_MDC_CFG	PHY MDC clock configuration Used to configure the divider N for MDC clock frequency. MDC clock is sourced from 12.5MHz system clock and divided by N. [note] MDC clock is gated or disabled when PHY_MDC_CFG is set to 0.
23:21	RESV0	Reserved
20	MDC_TURBO	MDC clock Turbo mode When this bit is set, MDC clock is sourced from 25MHz system clock and divided by PHY_MDC_CFG.
19:18	RESV1	Reserved
17:16	EE_AN_EN	PHY EEE auto-polling enable
15:13	RESV2	Reserved
12:8	PHY_END_ADDR	PHY polling end address Indicate the end of PHY address of PHY auto-polling process. [note] The difference between start and end must be 1.
7:5	RESV3	Reserved
4:0	PHY_START_ADDR	PHY polling start address Indicate the start of PHY address of PHY auto-polling process.

15110004		MAC PIAC			PHY Indirect Access Control										00090000		
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
Name	PHY_ACS_ST	RESV0	MDIO_REG_ADDR					MDIO_PHY_ADDR					MDIO_CMD		NMDIO_ST		
Type	W1C	RW	RW					RW					RW		RW		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Name	MDIO_RW_DATA																
Type	RW																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Bit(s)	Name	Description
31	PHY_ACS_ST	PHY access start Start to indirect access PHY's register. While PHY's register access is complete, this bit will be self-cleared to 0.
30	RESV0	Reserved
29:25	MDIO_REG_ADDR	Register Address (Clause 22) or Device Address (Clause 45)
24:20	MDIO_PHY_ADDR	PHY Address (Clause 22) or Port Address (Clause 45)

Bit(s)	Name	Description
19:18	MDIO_CMD	MDIO command
17:16	NMDIO_ST	MDIO Start Field
15:0	MDIO_RW_DATA	MDIO Read/Write data This is used as MDIO data field for read/write data access. When MDIO write command is activated, this is used as MDIO write data field. When MDIO read command is activated, this is used as MDIO read data field for read access only.

15110008	MAC_GPC				GIGA MAC Port Control								400C400C			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					RESV0				P2_RMII_CKRX	P2_RMII_CKIN	P2_TMII_FREQ	P2_TMII_MODE	P2_TX_CLK_MODE	P2_RX_CLK_MODE	P2_RX_SKEW	
Type					RW				RW	RW	RW	RW	RW	RW	RW	
Reset					0	0	0		0	0	0	0	1	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RESV2		P1_TMII_FREQ	P1_TMII_MODE	P1_TX_CLK_MODE	P1_RX_CLK_MODE	P1_RX_SKEW	
Type									RW		RW	RW	RW	RW	RW	
Reset									0	0	0	0	1	1	0	0

Bit(s)	Name	Description
27:25	RESV0	Reserved
23	P2_RMII_CKRX	RMII Reference Clock Pin Selection
22	P2_RMII_CKIN	RMII Reference Clock Direction
21	P2_TMII_FREQ	
20	P2_TMII_MODE	TMII mode Switch to Turbot MII mode
19	P2_TX_CLK_MODE	P2 TX clock control
18	P2_RX_CLK_MODE	P2 RX clock control
17:16	P2_RX_SKEW	P2 RX clock skew control
7:6	RESV2	Reserved
5	P1_TMII_FREQ	
4	P1_TMII_MODE	TMII mode Switch to Turbot MII mode
3	P1_TX_CLK_MODE	P1 TX clock control
2	P1_RX_CLK_MODE	P1 RX clock control
1:0	P1_RX_SKEW	P1 RX clock skew control

1511000C MAC_MISC

MAC MISC register

80000006

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AUTO_POLLING_1G	RESV														
Type	RW	RW														
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESV												CNTR_WRAP	CNTR_RC	ESW_MUX_SEL	
Type	RW												RW	RW	RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0

Bit(s)	Name	Description
31	AUTO_POLLING_1G	
30:3	RESV	Reserved
2	CNTR_WRAP	counter wrap control
1	CNTR_RC	counter read clear control
0	ESW_MUX_SEL	

15110100 MAC P1 MCR Port 1 MAC Control 20006300

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_RX_JUMBO				RESV0		MAC_RX_PKT_LEN		MTCC_LMT				IPG_CFG		RESV1	DIFF_RX_FIFO_WCLR
Type	RW				RW		RW		RW				RW		RW	RW
Reset	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FORCE_MODE	MAC_TX_EN	MAC_RX_EN	DEL_RX_FIFO_CLR	GMAC_RDMA_HANG_ECO_ROLLBACK	PRMBL_LMT_EN	BKOFF_EN	BACKPR_EN	FORCE_EEE1G	FORCE_EEE10G	FORCE_RX_FC	FORCE_TX_FC	FORCE_SPD		FORCE_DPX	FORCE_LINK
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW		RW	RW
Reset	0	1	1	0	0	0	1	1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:28	MAX_RX_JUMBO	Maximum received jumbo packet length
27:26	RESV0	
25:24	MAC_RX_PKT_LEN	Maximum received packet length
		Sets the maximum length of ingress packets including CRC that can be received by MAC.
23:20	MTCC_LMT	MTCC limit
		Maximum transmit collision count limitation.
19:18	IPG_CFG	Inter-Frame Gap Shrink
17	RESV1	Reserved
16	DIFF_RXFIFO_WCLR	Change RX FIFO wclear function
15	FORCE_MODE	Force MAC Mode
14	MAC_TX_EN	TX MAC Enable
13	MAC_RX_EN	RX MAC Enable
12	DEL_RXFIFO_CLR	Disable RX FIFO clear function
11	GMAC_RDMA_HANG_ECO_ROLLBACK	Rollback ECO for GMAC RDMA hang issue
10	PRMBL_LMT_EN	Preamble Limit Enable
9	BKOFF_EN	Back-off Enable
8	BACKPR_EN	Back-Pressure enable
7	FORCE_EEE1G	Force LPI mode for 1000m link speed
		When (FORCE_MODE= 1), these bits are used to control MAC EEE mode
6	FORCE_EEE100	Force LPI mode for 100m link speed
		When (FORCE_MODE= 1), these bits are used to control MAC EEE mode
5	FORCE_RX_FC	Force RX flow control
		When (FORCE_MODE= 1), these bits are used to control MAC RX flow control
4	FORCE_TX_FC	Force TX flow control
		When (FORCE_MODE= 1), these bits are used to control MAC TX flow control
3:2	FORCE_SPD	Force link speed
		When (FORCE_MODE= 1), these bits are used to control MAC link speed
1	FORCE_DPX	Force duplex
		When (FORCE_MODE= 1), these bits are used to control MAC link duplex
0	FORCE_LINK	Force link state
		When (FORCE_MODE= 1), these bits are used to control MAC link state

15110104	MAC_P1_EEE				Port 1 EEE Control												00000002
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
Name	WAKEUP_TIME_1000								WAKEUP_TIME_100								
Type	RW								RW								
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Name	LPI_TXIDLE_THD								RESV0				CKG_T XIDLE	CKG_R XLPI		LPI_M ODE	
Type	RW								RW				RW	RW		RW	

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	WAKEUP_TIME_1000	Wake up time for 1000mbps LPI mode The minimum allowed time needed to wait for PHY to be fully functional and TXMAC can transmit packet after wake-up Time unit: 1us
23:16	WAKEUP_TIME_100	Wake up time for 100mbps LPI mode The minimum allowed time needed to wait for PHY to be fully functional and TXMAC can transmit packet after wake-up Time unit: 1us
15:8	LPI_TXIDLE_THD	TX IDLE timer to enter LPI mode When there is no packet to be transmitted and exceeds time period specified by LPI_TXIDLE_THD, the TXMAC will automatically enter LPI (Low Power Idle) mode and send EEE LPI signal to link partner Time unit: 1ms
7:4	RESV0	Reserved
3	CKG_TXIDLE	TX Clock Power Down
2	CKG_RXLPI	RX Clock Power Down
0	LPI_MODE	LPI mode activated

15110108 **MAC P1_SR** Port 1 MAC Status 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RESV0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESV0								EEE1G_STATUS	EEE100_STATUS	RX_FC_STATUS	TX_FC_STATUS	SPD_STATUS		DPX_STATUS	LINK_STATUS
Type	RO								RO	RO	RO	RO	RO		RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:8	RESV0	Reserved
7	EEE1G_STATUS	LPI mode for 1000m link speed
6	EEE100_STATUS	LPI mode for 100m link speed
5	RX_FC_STATUS	RX flow control status
4	TX_FC_STATUS	TX flow control status
3:2	SPD_STATUS	Link speed status
1	DPX_STATUS	Duplex status
0	LINK_STATUS	Link state

1511010C MAC P1 FSM Port 1 FSM 01010000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

15110110 MAC P1 WOL Port 1 WOL 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WOL_DBG														WOL_I NT_STS	WOL_S TS
Type	RO														W1C	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESV0												SNP_P KT	CRC_DI S	WOL_I NT_EN	WOL_E N
Type	RW												RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:18	WOL_DBG	GMAC1 Wake-up On Lan Debug Signals
17	WOL_INT_STS	GMAC1 Wake-up On Lan Interrupt Status
16	WOL_STS	GMAC1 Wake-up On Lan Status If enable WOL_EN, this bit will change from 0 to 1 when GMAC RX state machine enter IDLE state. It indicates GMAC will drop all packets and detect magic packet.
15:4	RESV0	
3	SNP_PKT	GMAC1 Wake-up On Lan with snoopy packet
2	CRC_DIS	GMAC1 Wake-up On Lan with CRC Check Disable
1	WOL_INT_EN	GMAC1 Wake-up On Lan Interrupt Enable

Bit(s)	Name	Description
0	WOL_EN	GMAC1 Wake-up On Lan Function Enable

15110114 MAC_P1_SGMII Port 1 SGMII 050B0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	LOADPSTMR_EXTEND_TIME								SYNCDONE_TIME							
Type	RW								RW							
Reset	0	0	0	0	0	1	0	1	0	0	0	0	1	0	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																DIS_TXCLK_ENA
Type																RW
Reset																1

Bit(s)	Name	Description
31:24	LOADPSTMR_EXTEND_TIME	rx_loadpstmr extend time in SGMII mode
23:16	SYNCDONE_TIME	Sync done time for RX flow control in SGMII mode
0	DIS_TXCLK_ENA	Disable txclk_ena in SGMII mode

15110118 MAC_P1_PFC_CTRL Port 1 PFC Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RESV															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESV												PFC_AUTO_SYNC_DLY	PFC_SYNC_EN	PFC_EN	
Type	RW												RW	RW	RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:4	RESV	
3:2	PFC_AUTO_SYNC_DLY	Select the delay of sending PFC auto sync packet

Bit(s)	Name	Description
1	PFC_SYNC_EN	Enable the PFC auto-sync ability
0	PFC_EN	Enable the PFC ability

1511011C MAC P1 PFC STS Port 1 PFC Status 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RESV															PFC_A UTO_E N
Type	RO															RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_PFC_STS								RX_PFC_STS							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:17	RESV	
16	PFC_AUTO_EN	PFC auto enable status
15:8	TX_PFC_STS	
7:0	RX_PFC_STS	

15110120 MAC P1 PFC RX_PSON_CNT Port 1 RX PFC pause on counter for low priority 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Q3_RX_PSON_CNT								Q2_RX_PSON_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Q1_RX_PSON_CNT								Q0_RX_PSON_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	Q3_RX_PSON_CNT	PFC RX pause on count for port 1 priority 3
23:16	Q2_RX_PSON_CNT	PFC RX pause on count for port 1 priority 2
15:8	Q1_RX_PSON_CNT	PFC RX pause on count for port 1 priority 1
7:0	Q0_RX_PSON_CNT	PFC RX pause on count for port 1 priority 0

15110124 **MAC_P1_PFC_RX_PSON_CNT** Port 1 RX PFC pause on counter for high priority 00000000

H

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Q7_RX_PSON_CNT								Q6_RX_PSON_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Q5_RX_PSON_CNT								Q4_RX_PSON_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	Q7_RX_PSON_CNT	PFC RX pause on count for port 1 priority 7
23:16	Q6_RX_PSON_CNT	PFC RX pause on count for port 1 priority 6
15:8	Q5_RX_PSON_CNT	PFC RX pause on count for port 1 priority 5
7:0	Q4_RX_PSON_CNT	PFC RX pause on count for port 1 priority 4

15110128 **MAC_P1_PFC_RX_PSOFF_CNT** Port 1 RX PFC pause off counter for low priority 00000000

L

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Q3_RX_PSOFF_CNT								Q2_RX_PSOFF_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Q1_RX_PSOFF_CNT								Q0_RX_PSOFF_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	Q3_RX_PSOFF_CNT	PFC RX pause off count for port 1 priority 3
23:16	Q2_RX_PSOFF_CNT	PFC RX pause off count for port 1 priority 2
15:8	Q1_RX_PSOFF_CNT	PFC RX pause off count for port 1 priority 1
7:0	Q0_RX_PSOFF_CNT	PFC RX pause off count for port 1 priority 0

1511012C **MAC_P1_PFC_RX_PSOFF_CNT** Port 1 RX PFC pause off counter for high priority 00000000

H

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Q7_RX_PSOFF_CNT								Q6_RX_PSOFF_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Q5_RX_PSOFF_CNT								Q4_RX_PSOFF_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	Q7_RX_PSOFF_CNT	PFC RX pause off count for port 1 priority 7
23:16	Q6_RX_PSOFF_CNT	PFC RX pause off count for port 1 priority 6
15:8	Q5_RX_PSOFF_CNT	PFC RX pause off count for port 1 priority 5
7:0	Q4_RX_PSOFF_CNT	PFC RX pause off count for port 1 priority 4

15110130 **MAC_P1_PFC_TX_PSON_CNT** Port 1 TX PFC pause on counter for low priority 00000000

L

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Q3_TX_PSON_CNT								Q2_TX_PSON_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Q1_TX_PSON_CNT								Q0_TX_PSON_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	Q3_TX_PSON_CNT	PFC TX pause on count for port 1 priority 3
23:16	Q2_TX_PSON_CNT	PFC TX pause on count for port 1 priority 2
15:8	Q1_TX_PSON_CNT	PFC TX pause on count for port 1 priority 1
7:0	Q0_TX_PSON_CNT	PFC TX pause on count for port 1 priority 0

15110134 **MAC_P1_PFC_TX_PSON_CNT** Port 1 TX PFC pause on counter for high priority 00000000

H

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Q7_TX_PSON_CNT								Q6_TX_PSON_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Q5_TX_PSON_CNT								Q4_TX_PSON_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	Q7_TX_PSON_CNT	PFC TX pause on count for port 1 priority 7
23:16	Q6_TX_PSON_CNT	PFC TX pause on count for port 1 priority 6
15:8	Q5_TX_PSON_CNT	PFC TX pause on count for port 1 priority 5
7:0	Q4_TX_PSON_CNT	PFC TX pause on count for port 1 priority 4

15110138 **MAC_P1_PFC_TX_PSOFF_CNT** Port 1 TX PFC pause off counter for low priority 00000000

L

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Q3_TX_PSOFF_CNT								Q2_TX_PSOFF_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Q1_TX_PSOFF_CNT								Q0_TX_PSOFF_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	Q3_TX_PSOFF_CNT	PFC TX pause off count for port 1 priority 3
23:16	Q2_TX_PSOFF_CNT	PFC TX pause off count for port 1 priority 2
15:8	Q1_TX_PSOFF_CNT	PFC TX pause off count for port 1 priority 1
7:0	Q0_TX_PSOFF_CNT	PFC TX pause off count for port 1 priority 0

1511013C **MAC P1 PFC TX PSOFF CNT** Port 1 TX PFC pause off counter for high priority 00000000

H

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Q7_TX_PSOFF_CNT								Q6_TX_PSOFF_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Q5_TX_PSOFF_CNT								Q4_TX_PSOFF_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	Q7_TX_PSOFF_CNT	PFC TX pause off count for port 1 priority 7
23:16	Q6_TX_PSOFF_CNT	PFC TX pause off count for port 1 priority 6
15:8	Q5_TX_PSOFF_CNT	PFC TX pause off count for port 1 priority 5
7:0	Q4_TX_PSOFF_CNT	PFC TX pause off count for port 1 priority 4

15110200 **MAC P2 MCR** Port 2 MAC Control 20006300

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_RX_JUMBO				RESV0		MAC_RX_PKT_LEN		MTCC_LMT				IPG_CFG		RESV1	DIFF_RX_FIFO_WCLR
Type	RW				RW		RW		RW				RW		RW	RW
Reset	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FORCE_MOD_E	MAC_TX_EN	MAC_RX_EN	DEL_RX_FIFO_CLR	GMAC_RDMA_HANG_ECO_ROLLBACK	PRMBL_LMT_EN	BKOFF_EN	BACKPR_EN	FORCE_EEE1G	FORCE_EEE10G	FORCE_RX_FC	FORCE_TX_FC	FORCE_SPD		FORCE_DPX	FORCE_LINK

Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	1	1	0	0	0	1	1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:28	MAX_RX_JUMBO	Maximum received jumbo packet length
27:26	RESV0	
25:24	MAC_RX_PKT_LEN	Maximum received packet length Sets the maximum length of ingress packets including CRC that can be received by MAC.
23:20	MTCC_LMT	MTCC limit Maximum transmit collision count limitation.
19:18	IPG_CFG	Inter-Frame Gap Shrink
17	RESV1	Reserved
16	DIFF_RXFIFO_WCLR	Change RX FIFO wclear function
15	FORCE_MODE	Force MAC Mode
14	MAC_TX_EN	TX MAC Enable
13	MAC_RX_EN	RX MAC Enable
12	DEL_RXFIFO_CLR	Disable RX FIFO clear function
11	GMAC_RDMA_HANG_ECO_ROLLBACK	Rollback ECO for GMAC RDMA hang issue
10	PRMBL_LMT_EN	Preamble Limit Enable
9	BKOFF_EN	Back-off Enable
8	BACKPR_EN	Back-Pressure enable
7	FORCE_EEE1G	Force LPI mode for 1000m link speed
6	FORCE_EEE100	When (FORCE_MODE= 1), these bits are used to control MAC EEE mode Force LPI mode for 100m link speed
5	FORCE_RX_FC	When (FORCE_MODE= 1), these bits are used to control MAC EEE mode Force RX flow control
4	FORCE_TX_FC	When (FORCE_MODE= 1), these bits are used to control MAC RX flow control Force TX flow control
3:2	FORCE_SPD	Force link speed When (FORCE_MODE= 1), these bits are used to control MAC link speed
1	FORCE_DPX	Force duplex When (FORCE_MODE= 1), these bits are used to control MAC link duplex
0	FORCE_LINK	Force link state When (FORCE_MODE= 1), these bits are used to control MAC link state

15110204		MAC_P2_EEE				Port 2 EEE Control										00000002	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
Name	WAKEUP_TIME_1000								WAKEUP_TIME_100								
Type	RW								RW								
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	

Name	LPI_TXIDLE_THD								RESV0				CKG_T XIDLE	CKG_R XLPI		LPI_M ODE
Type	RW								RW				RW	RW		RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0		0

Bit(s)	Name	Description
31:24	WAKEUP_TIME_1000	Wake up time for 1000mbps LPI mode The minimum allowed time needed to wait for PHY to be fully functional and TXMAC can transmit packet after wake-up Time unit: 1us
23:16	WAKEUP_TIME_100	Wake up time for 100mbps LPI mode The minimum allowed time needed to wait for PHY to be fully functional and TXMAC can transmit packet after wake-up Time unit: 1us
15:8	LPI_TXIDLE_THD	TX IDLE timer to enter LPI mode When there is no packet to be transmitted and exceeds time period specified by LPI_TXIDLE_THD, the TXMAC will automatically enter LPI (Low Power Idle) mode and send EEE LPI signal to link partner Time unit: 1ms
7:4	RESV0	Reserved
3	CKG_TXIDLE	TX Clock Power Down
2	CKG_RXLPI	RX Clock Power Down
0	LPI_MODE	LPI mode activated

15110208 MAC_P2_SR Port 2 MAC Status 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RESV0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESV0								EEE1G_STATUS	EEE100_STATUS	RX_FC_STATUS	TX_FC_STATUS	SPD_STATUS		DPX_STATUS	LINK_STATUS
Type	RO								RO	RO	RO	RO	RO		RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:8	RESV0	Reserved
7	EEE1G_STATUS	LPI mode for 1000m link speed
6	EEE100_STATUS	LPI mode for 100m link speed
5	RX_FC_STATUS	RX flow control status

Bit(s)	Name	Description
4	TX_FC_STATUS	TX flow control status
3:2	SPD_STATUS	Link speed status
1	DPX_STATUS	Duplex status
0	LINK_STATUS	Link state

1511020C MAC P2 FSM Port 2 FSM 01010000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

15110210 MAC P2 WOL Port 2 WOL 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WOL_DBG														WOL_I NT_STS	WOL_S TS
Type	RO														W1C	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESV0												SNP_P KT	CRC_DI S	WOL_I NT_EN	WOL_E N
Type	RW												RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:18	WOL_DBG	GMAC2 Wake-up On Lan Debug Signals
17	WOL_INT_STS	GMAC2 Wake-up On Lan Interrupt Status
16	WOL_STS	GMAC2 Wake-up On Lan Status

Bit(s)	Name	Description
		If enable WOL_EN, this bit will change from 0 to 1 when GMAC RX state machine enter IDLE state. It indicates GMAC will drop all packets and detect magic packet.
15:4	RESVO	
3	SNP_PKT	GMAC2 Wake-up On Lan with snoopy packet
2	CRC_DIS	GMAC2 Wake-up On Lan with CRC Check Disable
1	WOL_INT_EN	GMAC2 Wake-up On Lan Interrupt Enable
0	WOL_EN	GMAC2 Wake-up On Lan Function Enable

15110214 MAC P2 SGMII Port 2 SGMII 05080001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	LOADPSTMR_EXTEND_TIME								SYNCDONE_TIME							
Type	RW								RW							
Reset	0	0	0	0	0	1	0	1	0	0	0	0	1	0	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																DIS_TXCLK_ENA
Type																RW
Reset																1

Bit(s)	Name	Description
31:24	LOADPSTMR_EXTEND_TIME	rx_loadpstmr extend time in SGMII mode
23:16	SYNCDONE_TIME	Sync done time for RX flow control in SGMII mode
0	DIS_TXCLK_ENA	Disable txclk_ena in SGMII mode

15110218 MAC P2 PFC CTRL Port 2 PFC Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RESV															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESV												PFC_AUTO_SYNC_DLY	PFC_SYNC_EN	PFC_EN	
Type	RW												RW	RW	RW	

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:4	RESV	
3:2	PFC_AUTO_SYNC_DLY	Select the delay of sending PFC auto sync packet
1	PFC_SYNC_EN	Enable the PFC auto-sync ability
0	PFC_EN	Enable the PFC ability

1511021C MAC P2 PFC STS Port 2 PFC Status 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RESV															PFC_A UTO_E N
Type	RO															RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_PFC_STS								RX_PFC_STS							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:17	RESV	
16	PFC_AUTO_EN	PFC auto enable status
15:8	TX_PFC_STS	
7:0	RX_PFC_STS	

15110220 MAC P2 PFC RX PSON CNT Port 2 RX PFC pause on counter for low priority 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Q3_RX_PSON_CNT								Q2_RX_PSON_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Q1_RX_PSON_CNT								Q0_RX_PSON_CNT							
Type	RC								RC							

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	Q3_RX_PSON_CNT	PFC RX pause on count for port 2 priority 3
23:16	Q2_RX_PSON_CNT	PFC RX pause on count for port 2 priority 2
15:8	Q1_RX_PSON_CNT	PFC RX pause on count for port 2 priority 1
7:0	Q0_RX_PSON_CNT	PFC RX pause on count for port 2 priority 0

15110224 **MAC P2 PFC RX PSON_CNT** Port 2 RX PFC pause on counter for high priority 00000000
H

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Q7_RX_PSON_CNT								Q6_RX_PSON_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Q5_RX_PSON_CNT								Q4_RX_PSON_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	Q7_RX_PSON_CNT	PFC RX pause on count for port 2 priority 7
23:16	Q6_RX_PSON_CNT	PFC RX pause on count for port 2 priority 6
15:8	Q5_RX_PSON_CNT	PFC RX pause on count for port 2 priority 5
7:0	Q4_RX_PSON_CNT	PFC RX pause on count for port 2 priority 4

15110228 **MAC P2 PFC RX PSOFF_CNT** Port 2 RX PFC pause off counter for low priority 00000000
L

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Q3_RX_PSOFF_CNT								Q2_RX_PSOFF_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Q1_RX_PSOFF_CNT								Q0_RX_PSOFF_CNT							
Type	RC								RC							

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	Q3_RX_PSOFF_CNT	PFC RX pause off count for port 2 priority 3
23:16	Q2_RX_PSOFF_CNT	PFC RX pause off count for port 2 priority 2
15:8	Q1_RX_PSOFF_CNT	PFC RX pause off count for port 2 priority 1
7:0	Q0_RX_PSOFF_CNT	PFC RX pause off count for port 2 priority 0

1511022C **MAC P2 PFC RX PSOFF CNT** Port 2 RX PFC pause off counter for high priority 00000000
H

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Q7_RX_PSOFF_CNT								Q6_RX_PSOFF_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Q5_RX_PSOFF_CNT								Q4_RX_PSOFF_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	Q7_RX_PSOFF_CNT	PFC RX pause off count for port 2 priority 7
23:16	Q6_RX_PSOFF_CNT	PFC RX pause off count for port 2 priority 6
15:8	Q5_RX_PSOFF_CNT	PFC RX pause off count for port 2 priority 5
7:0	Q4_RX_PSOFF_CNT	PFC RX pause off count for port 2 priority 4

15110230 **MAC P2 PFC TX PSON CNT** Port 2 TX PFC pause on counter for low priority 00000000
L

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Q3_TX_PSON_CNT								Q2_TX_PSON_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Q1_TX_PSON_CNT								Q0_TX_PSON_CNT							
Type	RC								RC							

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	Q3_TX_PSON_CNT	PFC TX pause on count for port 2 priority 3
23:16	Q2_TX_PSON_CNT	PFC TX pause on count for port 2 priority 2
15:8	Q1_TX_PSON_CNT	PFC TX pause on count for port 2 priority 1
7:0	Q0_TX_PSON_CNT	PFC TX pause on count for port 2 priority 0

15110234 **MAC P2 PFC TX PSON_CNT** Port 2 TX PFC pause on counter for high priority 00000000
H

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Q7_TX_PSON_CNT								Q6_TX_PSON_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Q5_TX_PSON_CNT								Q4_TX_PSON_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	Q7_TX_PSON_CNT	PFC TX pause on count for port 2 priority 7
23:16	Q6_TX_PSON_CNT	PFC TX pause on count for port 2 priority 6
15:8	Q5_TX_PSON_CNT	PFC TX pause on count for port 2 priority 5
7:0	Q4_TX_PSON_CNT	PFC TX pause on count for port 2 priority 4

15110238 **MAC P2 PFC TX PSOFF_CNT** Port 2 TX PFC pause off counter for low priority 00000000
L

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Q3_TX_PSOFF_CNT								Q2_TX_PSOFF_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Q1_TX_PSOFF_CNT								Q0_TX_PSOFF_CNT							
Type	RC								RC							

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	Q3_TX_PSOFF_CNT	PFC TX pause off count for port 2 priority 3
23:16	Q2_TX_PSOFF_CNT	PFC TX pause off count for port 2 priority 2
15:8	Q1_TX_PSOFF_CNT	PFC TX pause off count for port 2 priority 1
7:0	Q0_TX_PSOFF_CNT	PFC TX pause off count for port 2 priority 0

1511023C **MAC P2 PFC TX PSOFF CNT** Port 2 TX PFC pause off counter for high priority 00000000
H

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Q7_TX_PSOFF_CNT								Q6_TX_PSOFF_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Q5_TX_PSOFF_CNT								Q4_TX_PSOFF_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	Q7_TX_PSOFF_CNT	PFC TX pause off count for port 2 priority 7
23:16	Q6_TX_PSOFF_CNT	PFC TX pause off count for port 2 priority 6
15:8	Q5_TX_PSOFF_CNT	PFC TX pause off count for port 2 priority 5
7:0	Q4_TX_PSOFF_CNT	PFC TX pause off count for port 2 priority 4

15110400 **GMAC P1 RX UCST PKTCNT** Port 1 RX unicast packet count low word 00000000
L

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	P1_RX_UCST_PKTCNTL															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P1_RX_UCST_PKTCNTL															
Type	RC															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	P1_RX_UCST_PKTCTL	RX unicast packet count low word

15110404 GMAC P1 RX UCST PKTCNT Port 1 RX unicast packet count high word 00000000
H

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	P1_RX_UCST_PKTCTH															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P1_RX_UCST_PKTCTH															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	P1_RX_UCST_PKTCTH	RX unicast packet count high word

15110408 GMAC P1 RX UCST BYTECN Port 1 RX unicast byte count low word 00000000
TL

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	P1_RX_UCST_BYTECNL															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P1_RX_UCST_BYTECNL															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	P1_RX_UCST_BYTECNL	RX unicast byte count low word

Bit(s)	Name	Description

1511040C **GMAC P1_RX_UCST_BYTECN** Port 1 RX unicast byte count high word 00000000
TH

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	P1_RX_UCST_BYTECNTH															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P1_RX_UCST_BYTECNTH															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	P1_RX_UCST_BYTECNTH	RX unicast byte count high word

15110410 **GMAC P1_RX_MCST_PKT CNT** Port 1 RX multicast packet count low word 00000000
L

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	P1_RX_MCST_PKT CNTL															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P1_RX_MCST_PKT CNTL															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	P1_RX_MCST_PKT CNTL	RX multicast packet count low word

15110414 **GMAC P1_RX_MCST_PKT CNT** Port 1 RX multicast packet count high word 00000000
H

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	P1_RX_MCST_PKT CNTH															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P1_RX_MCST_PKT CNTH															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	P1_RX_MCST_PKT CNTH	RX multicast packet count high word

15110418 **GMAC_P1_RX_MCST_BYTECN** Port 1 RX multicast byte count low word **00000000**
TL

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	P1_RX_MCST_BYTECN TL															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P1_RX_MCST_BYTECN TL															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	P1_RX_MCST_BYTECN TL	RX multicast byte count low word

1511041C **GMAC_P1_RX_MCST_BYTECN** Port 1 RX multicast byte count high word **00000000**
TH

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	P1_RX_MCST_BYTECN TH															
Type	RC															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P1_RX_MCST_BYTECNTH															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	P1_RX_MCST_BYTECNTH	RX multicast byte count high word

15110420 GMAC P1 RX BCST PKTCNT Port 1 RX broadcast packet count low word 00000000

L

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	P1_RX_BCST_PKTCNTL															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P1_RX_BCST_PKTCNTL															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	P1_RX_BCST_PKTCNTL	RX broadcast packet count low word

15110424 GMAC P1 RX BCST PKTCNT Port 1 RX broadcast packet count high word 00000000

H

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	P1_RX_BCST_PKTCNTH															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P1_RX_BCST_PKTCNTH															

Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	P1_RX_BCST_PKT CNTH	RX broadcast packet count high word

15110428 **GMAC P1 RX BCST BYTECN TL** Port 1 RX broadcast byte count low word 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	P1_RX_BCST_BYTECN TL															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P1_RX_BCST_BYTECN TL															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	P1_RX_BCST_BYTECN TL	RX broadcast byte count low word

1511042C **GMAC P1 RX BCST BYTECN TH** Port 1 RX broadcast byte count high word 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	P1_RX_BCST_BYTECN TH															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P1_RX_BCST_BYTECN TH															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	P1_RX_BCST_BYTECNTH	RX broadcast byte count high word

15110430 **GMAC P1 TX UCST PKTCNTL** Port 1 TX unicast packet count low word 00000000

L

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	P1_TX_UCST_PKTCNTL															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P1_TX_UCST_PKTCNTL															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	P1_TX_UCST_PKTCNTL	TX unicast packet count low word

15110434 **GMAC P1 TX UCST PKTCNT** Port 1 TX unicast packet count high word 00000000

H

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	P1_TX_UCST_PKTCNTH															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P1_TX_UCST_PKTCNTH															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	P1_TX_UCST_PKTCNTH	TX unicast packet count high word

15110438 **GMAC P1_TX_UCST_BYTECN** Port 1 TX unicast byte count low word

00000000

TL

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	P1_TX_UCST_BYTECNL															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P1_TX_UCST_BYTECNL															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	P1_TX_UCST_BYTECNL	TX unicast byte count low word

1511043C **GMAC P1_TX_UCST_BYTECN** Port 1 TX unicast byte count high word

00000000

TH

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	P1_TX_UCST_BYTECNTH															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P1_TX_UCST_BYTECNTH															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	P1_TX_UCST_BYTECNTH	TX unicast byte count high word

15110440 **GMAC P1_TX_MCST_PKT CNT** Port 1 TX multicast packet count low word

00000000

L

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	P1_TX_MCST_PKT CNTL															

Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P1_TX_MCST_PKTCTL															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	P1_TX_MCST_PKTCTL	TX multicast packet count low word

15110444 **GMAC P1_TX_MCST_PKTCTL Port 1 TX multicast packet count high word** 00000000
H

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	P1_TX_MCST_PKTCTLH															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P1_TX_MCST_PKTCTLH															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	P1_TX_MCST_PKTCTLH	TX multicast packet count high word

15110448 **GMAC P1_TX_MCST_BYTECN Port 1 TX multicast byte count low word** 00000000
TL

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	P1_TX_MCST_BYTECNL															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	P1_TX_MCST_BYTECNL															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	P1_TX_MCST_BYTECNL	TX multicast byte count low word

1511044C GMAC_P1_TX_MCST_BYTECNL Port 1 TX multicast byte count high word 00000000

TH

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	P1_TX_MCST_BYTECNTH															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P1_TX_MCST_BYTECNTH															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	P1_TX_MCST_BYTECNTH	TX multicast byte count high word

15110450 GMAC_P1_TX_BCST_PKTCTRL Port 1 TX broadcast packet count low word 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	P1_TX_BCST_PKTCTRL															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P1_TX_BCST_PKTCTRL															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	P1_TX_BCST_PKTCTL	TX broadcast packet count low word

15110454 **GMAC P1 TX BCST PKTCNT** Port 1 TX broadcast packet count high word 00000000
H

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	P1_TX_BCST_PKTCTH															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P1_TX_BCST_PKTCTH															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	P1_TX_BCST_PKTCTH	TX broadcast packet count high word

15110458 **GMAC P1 TX BCST BYTECN** Port 1 TX broadcast byte count low word 00000000
TL

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	P1_TX_BCST_BYTECTL															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P1_TX_BCST_BYTECTL															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	P1_TX_BCST_BYTECTL	TX broadcast byte count low word

1511045C GMAC P1_TX_BCST_BYTECNTH Port 1 TX broadcast byte count high word **00000000**
TH

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	P1_TX_BCST_BYTECNTH															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P1_TX_BCST_BYTECNTH															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	P1_TX_BCST_BYTECNTH	TX broadcast byte count high word

15110460 GMAC P2_RX_UCST_PKT CNTL Port 2 RX unicast packet count low word **00000000**
L

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	P2_RX_UCST_PKT CNTL															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P2_RX_UCST_PKT CNTL															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	P2_RX_UCST_PKT CNTL	RX unicast packet count low word

15110464 GMAC P2_RX_UCST_PKT CNTL Port 2 RX unicast packet count high word **00000000**
H

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	P2_RX_UCST_PKT CNTH															

Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P2_RX_UCST_PKT CNTH															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	P2_RX_UCST_PKT CNTH	RX unicast packet count high word

15110468 **GMAC P2_RX_UCST_BYTECN TL** Port 2 RX unicast byte count low word 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	P2_RX_UCST_BYTECN TL															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P2_RX_UCST_BYTECN TL															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	P2_RX_UCST_BYTECN TL	RX unicast byte count low word

1511046C **GMAC P2_RX_UCST_BYTECN TH** Port 2 RX unicast byte count high word 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	P2_RX_UCST_BYTECN TH															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	P2_RX_UCST_BYTECNTH															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	P2_RX_UCST_BYTECNTH	RX unicast byte count high word

15110470 GMAC P2_RX_MCST_PKT CNT Port 2 RX multicast packet count low word 00000000

L

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	P2_RX_MCST_PKT CNTL															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P2_RX_MCST_PKT CNTL															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	P2_RX_MCST_PKT CNTL	RX multicast packet count low word

15110474 GMAC P2_RX_MCST_PKT CNT Port 2 RX multicast packet count high word 00000000

H

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	P2_RX_MCST_PKT CNTH															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P2_RX_MCST_PKT CNTH															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	P2_RX_MCST_PKTENTH	RX multicast packet count high word

15110478 **GMAC_P2_RX_MCST_BYTECNTL** Port 2 RX multicast byte count low word 00000000
TL

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	P2_RX_MCST_BYTECNTL															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P2_RX_MCST_BYTECNTL															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	P2_RX_MCST_BYTECNTL	RX multicast byte count low word

1511047C **GMAC_P2_RX_MCST_BYTECNTH** Port 2 RX multicast byte count high word 00000000
TH

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	P2_RX_MCST_BYTECNTH															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P2_RX_MCST_BYTECNTH															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	P2_RX_MCST_BYTECNTH	RX multicast byte count high word

15110480 GMAC P2 RX BCST PKTCNT Port 2 RX broadcast packet count low word

00000000

L

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	P2_RX_BCST_PKTCNTL															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P2_RX_BCST_PKTCNTL															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	P2_RX_BCST_PKTCNTL	RX broadcast packet count low word

15110484 GMAC P2 RX BCST PKTCNT Port 2 RX broadcast packet count high word

00000000

H

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	P2_RX_BCST_PKTCNTH															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P2_RX_BCST_PKTCNTH															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	P2_RX_BCST_PKTCNTH	RX broadcast packet count high word

15110488 GMAC P2 RX BCST BYTECN Port 2 RX broadcast byte count low word

00000000

TL

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	P2_RX_BCST_BYTECNTL															

Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P2_RX_BCST_BYTECNTRL															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	P2_RX_BCST_BYTECNTRL	RX broadcast byte count low word

1511048C GMAC P2_RX_BCST_BYTECNTH Port 2 RX broadcast byte count high word 00000000
TH

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	P2_RX_BCST_BYTECNTH															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P2_RX_BCST_BYTECNTH															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	P2_RX_BCST_BYTECNTH	RX broadcast byte count high word

15110490 GMAC P2_TX_UCST_PKT CNT Port 2 TX unicast packet count low word 00000000
L

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	P2_TX_UCST_PKT CNT															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	P2_TX_UCST_PKTCNTL															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	P2_TX_UCST_PKTCNTL	TX unicast packet count low word

15110494 **GMAC P2_TX_UCST_PKTCNT** Port 2 TX unicast packet count high word 00000000

H

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	P2_TX_UCST_PKTCNTH															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P2_TX_UCST_PKTCNTH															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	P2_TX_UCST_PKTCNTH	TX unicast packet count high word

15110498 **GMAC P2_TX_UCST_BYTECN** Port 2 TX unicast byte count low word 00000000

TL

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	P2_TX_UCST_BYTECNL															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P2_TX_UCST_BYTECNL															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	P2_TX_UCST_BYTECNTH	TX unicast byte count low word

1511049C **GMAC_P2_TX_UCST_BYTECNTH** Port 2 TX unicast byte count high word 00000000
TH

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	P2_TX_UCST_BYTECNTH															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P2_TX_UCST_BYTECNTH															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	P2_TX_UCST_BYTECNTH	TX unicast byte count high word

151104A0 **GMAC_P2_TX_MCST_PKTCLNT** Port 2 TX multicast packet count low word 00000000
L

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	P2_TX_MCST_PKTCLNT															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P2_TX_MCST_PKTCLNT															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	P2_TX_MCST_PKTCLNT	TX multicast packet count low word

151104A4 GMAC_P2_TX_MCST_PKT CNT Port 2 TX multicast packet count high word

00000000

H

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	P2_TX_MCST_PKT CNTH															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P2_TX_MCST_PKT CNTH															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	P2_TX_MCST_PKT CNTH	TX multicast packet count high word

151104A8 GMAC_P2_TX_MCST_BYTE CN Port 2 TX multicast byte count low word

00000000

TL

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	P2_TX_MCST_BYTE CN TL															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P2_TX_MCST_BYTE CN TL															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	P2_TX_MCST_BYTE CN TL	TX multicast byte count low word

151104AC GMAC_P2_TX_MCST_BYTE CN Port 2 TX multicast byte count high word

00000000

TH

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	P2_TX_MCST_BYTE CN TH															

Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P2_TX_MCST_BYTECNTH															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	P2_TX_MCST_BYTECNTH	TX multicast byte count high word

151104B0 **GMAC P2_TX_BCST_PKTCTL** Port 2 TX broadcast packet count low word 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	P2_TX_BCST_PKTCTL															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P2_TX_BCST_PKTCTL															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	P2_TX_BCST_PKTCTL	TX broadcast packet count low word

151104B4 **GMAC P2_TX_BCST_PKTCTL** Port 2 TX broadcast packet count high word 00000000
H

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	P2_TX_BCST_PKTCTL															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P2_TX_BCST_PKTCTL															

Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	P2_TX_BCST_PKT CNTH	TX broadcast packet count high word

151104B8 GMAC P2 TX BCST BYTECN TL Port 2 TX broadcast byte count low word 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	P2_TX_BCST_BYTECN TL															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P2_TX_BCST_BYTECN TL															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	P2_TX_BCST_BYTECN TL	TX broadcast byte count low word

151104BC GMAC P2 TX BCST BYTECN TH Port 2 TX broadcast byte count high word 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	P2_TX_BCST_BYTECN TH															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P2_TX_BCST_BYTECN TH															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	P2_TX_BCST_BYTECNTH	TX broadcast byte count high word

151A0000 **IRQ_SELO** IRQ Selection 0 Register 03020100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			IRQ3_SEL								IRQ2_SEL					
Type			RW								RW					
Reset			0	0	0	0	1	1			0	0	0	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			IRQ1_SEL								IRQ0_SEL					
Type			RW								RW					
Reset			0	0	0	0	0	1			0	0	0	0	0	0

Bit(s)	Name	Description
29:24	IRQ3_SEL	Interrupt source selector 6'h0~6'h3f: Please reference to interrupt source table
21:16	IRQ2_SEL	Interrupt source selector 6'h0~6'h3f: Please reference to interrupt source table
13:8	IRQ1_SEL	Interrupt source selector 6'h0~6'h3f: Please reference to interrupt source table
5:0	IRQ0_SEL	Interrupt source selector 6'h0~6'h3f: Please reference to interrupt source table

151A0004 **IRQ_SEL1** IRQ Selection 1 Register 07060504

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			IRQ7_SEL								IRQ6_SEL					
Type			RW								RW					
Reset			0	0	0	1	1	1			0	0	0	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			IRQ5_SEL								IRQ4_SEL					
Type			RW								RW					
Reset			0	0	0	1	0	1			0	0	0	1	0	0

Bit(s)	Name	Description
29:24	IRQ7_SEL	Interrupt source selector 6'h0~6'h3f: Please reference to interrupt source table
21:16	IRQ6_SEL	Interrupt source selector 6'h0~6'h3f: Please reference to interrupt source table
13:8	IRQ5_SEL	Interrupt source selector 6'h0~6'h3f: Please reference to interrupt source table
5:0	IRQ4_SEL	Interrupt source selector 6'h0~6'h3f: Please reference to interrupt source table

151A0008 IRQ_SEL2 IRQ Selection 2 Register 0B0A0908

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			IRQB_SEL								IRQA_SEL					
Type			RW								RW					
Reset			0	0	1	0	1	1			0	0	1	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			IRQ9_SEL								IRQ8_SEL					
Type			RW								RW					
Reset			0	0	1	0	0	1			0	0	1	0	0	0

Bit(s)	Name	Description
29:24	IRQB_SEL	Interrupt source selector 6'h0~6'h3f: Please reference to interrupt source table
21:16	IRQA_SEL	Interrupt source selector 6'h0~6'h3f: Please reference to interrupt source table
13:8	IRQ9_SEL	Interrupt source selector 6'h0~6'h3f: Please reference to interrupt source table
5:0	IRQ8_SEL	Interrupt source selector 6'h0~6'h3f: Please reference to interrupt source table

151A000C IRQ_SEL3 IRQ Selection 3 Register 0F0E0D0C

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			IRQF_SEL								IRQE_SEL					
Type			RW								RW					
Reset			0	0	1	1	1	1			0	0	1	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name			IRQD_SEL								IRQC_SEL					
Type			RW								RW					
Reset			0	0	1	1	0	1			0	0	1	1	0	0

Bit(s)	Name	Description
29:24	IRQF_SEL	Interrupt source selector 6'h0~6'h3f: Please reference to interrupt source table
21:16	IRQE_SEL	Interrupt source selector 6'h0~6'h3f: Please reference to interrupt source table
13:8	IRQD_SEL	Interrupt source selector 6'h0~6'h3f: Please reference to interrupt source table
5:0	IRQC_SEL	Interrupt source selector 6'h0~6'h3f: Please reference to interrupt source table

151A0010 IRQ_SEL4 IRQ Selection 4 Register 13121110

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			IRQ13_SEL								IRQ12_SEL					
Type			RW								RW					
Reset			0	1	0	0	1	1			0	1	0	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			IRQ11_SEL								IRQ10_SEL					
Type			RW								RW					
Reset			0	1	0	0	0	1			0	1	0	0	0	0

Bit(s)	Name	Description
29:24	IRQ13_SEL	Interrupt source selector 6'h0~6'h3f: Please reference to interrupt source table
21:16	IRQ12_SEL	Interrupt source selector 6'h0~6'h3f: Please reference to interrupt source table
13:8	IRQ11_SEL	Interrupt source selector 6'h0~6'h3f: Please reference to interrupt source table
5:0	IRQ10_SEL	Interrupt source selector 6'h0~6'h3f: Please reference to interrupt source table

151A0014 IRQ_SEL5 IRQ Selection 5 Register 17161514

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name			IRQ17_SEL								IRQ16_SEL					
Type			RW								RW					
Reset			0	1	0	1	1	1			0	1	0	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			IRQ15_SEL								IRQ14_SEL					
Type			RW								RW					
Reset			0	1	0	1	0	1			0	1	0	1	0	0

Bit(s)	Name	Description
29:24	IRQ17_SEL	Interrupt source selector 6'h0~6'h3f: Please reference to interrupt source table
21:16	IRQ16_SEL	Interrupt source selector 6'h0~6'h3f: Please reference to interrupt source table
13:8	IRQ15_SEL	Interrupt source selector 6'h0~6'h3f: Please reference to interrupt source table
5:0	IRQ14_SEL	Interrupt source selector 6'h0~6'h3f: Please reference to interrupt source table

151A0018 **IRQ_SEL6** **IRQ Selection 6 Register** 1B1A1918

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			IRQ1B_SEL								IRQ1A_SEL					
Type			RW								RW					
Reset			0	1	1	0	1	1			0	1	1	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			IRQ19_SEL								IRQ18_SEL					
Type			RW								RW					
Reset			0	1	1	0	0	1			0	1	1	0	0	0

Bit(s)	Name	Description
29:24	IRQ1B_SEL	Interrupt source selector 6'h0~6'h3f: Please reference to interrupt source table
21:16	IRQ1A_SEL	Interrupt source selector 6'h0~6'h3f: Please reference to interrupt source table
13:8	IRQ19_SEL	Interrupt source selector 6'h0~6'h3f: Please reference to interrupt source table
5:0	IRQ18_SEL	Interrupt source selector 6'h0~6'h3f: Please reference to interrupt source table

Bit(s)	Name	Description
6'h0~6'h3f: Please reference to interrupt source table		

151A001C IRQ_SEL7 IRQ Selection 7 Register 1F1E1D1C

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			IRQ1F_SEL								IRQ1E_SEL					
Type			RW								RW					
Reset			0	1	1	1	1	1			0	1	1	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			IRQ1D_SEL								IRQ1C_SEL					
Type			RW								RW					
Reset			0	1	1	1	0	1			0	1	1	1	0	0

Bit(s)	Name	Description
29:24	IRQ1F_SEL	Interrupt source selector 6'h0~6'h3f: Please reference to interrupt source table
21:16	IRQ1E_SEL	Interrupt source selector 6'h0~6'h3f: Please reference to interrupt source table
13:8	IRQ1D_SEL	Interrupt source selector 6'h0~6'h3f: Please reference to interrupt source table
5:0	IRQ1C_SEL	Interrupt source selector 6'h0~6'h3f: Please reference to interrupt source table

151A0020 IRQ_SEL8 IRQ Selection 8 Register 23222120

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			IRQ23_SEL								IRQ22_SEL					
Type			RW								RW					
Reset			1	0	0	0	1	1			1	0	0	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			IRQ21_SEL								IRQ20_SEL					
Type			RW								RW					
Reset			1	0	0	0	0	1			1	0	0	0	0	0

Bit(s)	Name	Description
29:24	IRQ23_SEL	Interrupt source selector 6'h0~6'h3f: Please reference to interrupt source table
21:16	IRQ22_SEL	Interrupt source selector 6'h0~6'h3f: Please reference to interrupt source table
13:8	IRQ21_SEL	Interrupt source selector 6'h0~6'h3f: Please reference to interrupt source table
5:0	IRQ20_SEL	Interrupt source selector 6'h0~6'h3f: Please reference to interrupt source table

151A0024 **IRQ_SEL9** IRQ Selection 9 Register 27262524

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			IRQ27_SEL								IRQ26_SEL					
Type			RW								RW					
Reset			1	0	0	1	1	1			1	0	0	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			IRQ25_SEL								IRQ24_SEL					
Type			RW								RW					
Reset			1	0	0	1	0	1			1	0	0	1	0	0

Bit(s)	Name	Description
29:24	IRQ27_SEL	Interrupt source selector 6'h0~6'h3f: Please reference to interrupt source table
21:16	IRQ26_SEL	Interrupt source selector 6'h0~6'h3f: Please reference to interrupt source table
13:8	IRQ25_SEL	Interrupt source selector 6'h0~6'h3f: Please reference to interrupt source table
5:0	IRQ24_SEL	Interrupt source selector 6'h0~6'h3f: Please reference to interrupt source table

151A0028 **IRQ_SEL10** IRQ Selection 10 Register 2B2A2928

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			IRQ2B_SEL								IRQ2A_SEL					
Type			RW								RW					
Reset			1	0	1	0	1	1			1	0	1	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name			IRQ29_SEL								IRQ28_SEL					
Type			RW								RW					
Reset			1	0	1	0	0	1			1	0	1	0	0	0

Bit(s)	Name	Description
29:24	IRQ2B_SEL	Interrupt source selector 6'h0~6'h3f: Please reference to interrupt source table
21:16	IRQ2A_SEL	Interrupt source selector 6'h0~6'h3f: Please reference to interrupt source table
13:8	IRQ29_SEL	Interrupt source selector 6'h0~6'h3f: Please reference to interrupt source table
5:0	IRQ28_SEL	Interrupt source selector 6'h0~6'h3f: Please reference to interrupt source table

151A002C IRQ_SEL11 IRQ Selection 11 Register 2F2E2D2C

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			IRQ2F_SEL								IRQ2E_SEL					
Type			RW								RW					
Reset			1	0	1	1	1	1			1	0	1	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			IRQ2D_SEL								IRQ2C_SEL					
Type			RW								RW					
Reset			1	0	1	1	0	1			1	0	1	1	0	0

Bit(s)	Name	Description
29:24	IRQ2F_SEL	Interrupt source selector 6'h0~6'h3f: Please reference to interrupt source table
21:16	IRQ2E_SEL	Interrupt source selector 6'h0~6'h3f: Please reference to interrupt source table
13:8	IRQ2D_SEL	Interrupt source selector 6'h0~6'h3f: Please reference to interrupt source table
5:0	IRQ2C_SEL	Interrupt source selector 6'h0~6'h3f: Please reference to interrupt source table

151A0030 IRQ_SEL12 IRQ Selection 12 Register 33323130

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name			IRQ33_SEL								IRQ32_SEL					
Type			RW								RW					
Reset			1	1	0	0	1	1			1	1	0	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			IRQ31_SEL								IRQ30_SEL					
Type			RW								RW					
Reset			1	1	0	0	0	1			1	1	0	0	0	0

Bit(s)	Name	Description
29:24	IRQ33_SEL	Interrupt source selector 6'h0~6'h3f: Please reference to interrupt source table
21:16	IRQ32_SEL	Interrupt source selector 6'h0~6'h3f: Please reference to interrupt source table
13:8	IRQ31_SEL	Interrupt source selector 6'h0~6'h3f: Please reference to interrupt source table
5:0	IRQ30_SEL	Interrupt source selector 6'h0~6'h3f: Please reference to interrupt source table

151A0034 **IRQ_SEL13** **IRQ Selection 13 Register** 37363534

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			IRQ37_SEL								IRQ36_SEL					
Type			RW								RW					
Reset			1	1	0	1	1	1			1	1	0	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			IRQ35_SEL								IRQ34_SEL					
Type			RW								RW					
Reset			1	1	0	1	0	1			1	1	0	1	0	0

Bit(s)	Name	Description
29:24	IRQ37_SEL	Interrupt source selector 6'h0~6'h3f: Please reference to interrupt source table
21:16	IRQ36_SEL	Interrupt source selector 6'h0~6'h3f: Please reference to interrupt source table
13:8	IRQ35_SEL	Interrupt source selector 6'h0~6'h3f: Please reference to interrupt source table
5:0	IRQ34_SEL	Interrupt source selector 6'h0~6'h3f: Please reference to interrupt source table

Bit(s)	Name	Description
6'h0~6'h3f: Please reference to interrupt source table		

151A0038 IRQ_SEL14 IRQ Selection 14 Register 3B3A3938

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			IRQ3B_SEL								IRQ3A_SEL					
Type			RW								RW					
Reset			1	1	1	0	1	1			1	1	1	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			IRQ39_SEL								IRQ38_SEL					
Type			RW								RW					
Reset			1	1	1	0	0	1			1	1	1	0	0	0

Bit(s)	Name	Description
29:24	IRQ3B_SEL	Interrupt source selector 6'h0~6'h3f: Please reference to interrupt source table
21:16	IRQ3A_SEL	Interrupt source selector 6'h0~6'h3f: Please reference to interrupt source table
13:8	IRQ39_SEL	Interrupt source selector 6'h0~6'h3f: Please reference to interrupt source table
5:0	IRQ38_SEL	Interrupt source selector 6'h0~6'h3f: Please reference to interrupt source table

151A003C IRQ_SEL15 IRQ Selection 15 Register 3F3E3D3C

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			IRQ3F_SEL								IRQ3E_SEL					
Type			RW								RW					
Reset			1	1	1	1	1	1			1	1	1	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			IRQ3D_SEL								IRQ3C_SEL					
Type			RW								RW					
Reset			1	1	1	1	0	1			1	1	1	1	0	0

Bit(s)	Name	Description
29:24	IRQ3F_SEL	Interrupt source selector 6'h0~6'h3f: Please reference to interrupt source table
21:16	IRQ3E_SEL	Interrupt source selector 6'h0~6'h3f: Please reference to interrupt source table
13:8	IRQ3D_SEL	Interrupt source selector 6'h0~6'h3f: Please reference to interrupt source table
5:0	IRQ3C_SEL	Interrupt source selector 6'h0~6'h3f: Please reference to interrupt source table

151A006C **FIQ_SEL** **FIQ Selection Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											FIQ_SEL					
Type											RW					
Reset											0	0	0	0	0	0

Bit(s)	Name	Description
5:0	FIQ_SEL	FIQ source selector 6'h0~6'h3f: Please reference to interrupt source table

151A0070 **IRQ_MASK** **IRQ Mask Register** **FFFFFFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	IRQ1F_MSK	IRQ1E_MSK	IRQ1D_MSK	IRQ1C_MSK	IRQ1B_MSK	IRQ1A_MSK	IRQ19_MSK	IRQ18_MSK	IRQ17_MSK	IRQ16_MSK	IRQ15_MSK	IRQ14_MSK	IRQ13_MSK	IRQ12_MSK	IRQ11_MSK	IRQ10_MSK
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IRQF_MSK	IRQE_MSK	IRQD_MSK	IRQC_MSK	IRQB_MSK	IRQA_MSK	IRQ9_MSK	IRQ8_MSK	IRQ7_MSK	IRQ6_MSK	IRQ5_MSK	IRQ4_MSK	IRQ3_MSK	IRQ2_MSK	IRQ1_MSK	IRQ0_MSK
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31	IRQ1F_MSK	Mask control for the associated interrupt source in the IRQ controller 0: Interrupt is enabled 1: Interrupt is disabled
30	IRQ1E_MSK	Mask control for the associated interrupt source in the IRQ controller 0: Interrupt is enabled 1: Interrupt is disabled
29	IRQ1D_MSK	Mask control for the associated interrupt source in the IRQ controller 0: Interrupt is enabled 1: Interrupt is disabled
28	IRQ1C_MSK	Mask control for the associated interrupt source in the IRQ controller 0: Interrupt is enabled 1: Interrupt is disabled
27	IRQ1B_MSK	Mask control for the associated interrupt source in the IRQ controller 0: Interrupt is enabled 1: Interrupt is disabled
26	IRQ1A_MSK	Mask control for the associated interrupt source in the IRQ controller 0: Interrupt is enabled 1: Interrupt is disabled
25	IRQ19_MSK	Mask control for the associated interrupt source in the IRQ controller 0: Interrupt is enabled 1: Interrupt is disabled
24	IRQ18_MSK	Mask control for the associated interrupt source in the IRQ controller 0: Interrupt is enabled 1: Interrupt is disabled
23	IRQ17_MSK	Mask control for the associated interrupt source in the IRQ controller 0: Interrupt is enabled 1: Interrupt is disabled
22	IRQ16_MSK	Mask control for the associated interrupt source in the IRQ controller 0: Interrupt is enabled 1: Interrupt is disabled
21	IRQ15_MSK	Mask control for the associated interrupt source in the IRQ controller 0: Interrupt is enabled 1: Interrupt is disabled
20	IRQ14_MSK	Mask control for the associated interrupt source in the IRQ controller 0: Interrupt is enabled 1: Interrupt is disabled
19	IRQ13_MSK	Mask control for the associated interrupt source in the IRQ controller 0: Interrupt is enabled 1: Interrupt is disabled
18	IRQ12_MSK	Mask control for the associated interrupt source in the IRQ controller 0: Interrupt is enabled 1: Interrupt is disabled
17	IRQ11_MSK	Mask control for the associated interrupt source in the IRQ controller 0: Interrupt is enabled 1: Interrupt is disabled
16	IRQ10_MSK	Mask control for the associated interrupt source in the IRQ controller 0: Interrupt is enabled 1: Interrupt is disabled
15	IRQF_MSK	Mask control for the associated interrupt source in the IRQ controller 0: Interrupt is enabled 1: Interrupt is disabled
14	IRQE_MSK	Mask control for the associated interrupt source in the IRQ controller

Bit(s)	Name	Description
13	IRQD_MSK	0: Interrupt is enabled 1: Interrupt is disabled Mask control for the associated interrupt source in the IRQ controller
12	IRQC_MSK	0: Interrupt is enabled 1: Interrupt is disabled Mask control for the associated interrupt source in the IRQ controller
11	IRQB_MSK	0: Interrupt is enabled 1: Interrupt is disabled Mask control for the associated interrupt source in the IRQ controller
10	IRQA_MSK	0: Interrupt is enabled 1: Interrupt is disabled Mask control for the associated interrupt source in the IRQ controller
9	IRQ9_MSK	0: Interrupt is enabled 1: Interrupt is disabled Mask control for the associated interrupt source in the IRQ controller
8	IRQ8_MSK	0: Interrupt is enabled 1: Interrupt is disabled Mask control for the associated interrupt source in the IRQ controller
7	IRQ7_MSK	0: Interrupt is enabled 1: Interrupt is disabled Mask control for the associated interrupt source in the IRQ controller
6	IRQ6_MSK	0: Interrupt is enabled 1: Interrupt is disabled Mask control for the associated interrupt source in the IRQ controller
5	IRQ5_MSK	0: Interrupt is enabled 1: Interrupt is disabled Mask control for the associated interrupt source in the IRQ controller
4	IRQ4_MSK	0: Interrupt is enabled 1: Interrupt is disabled Mask control for the associated interrupt source in the IRQ controller
3	IRQ3_MSK	0: Interrupt is enabled 1: Interrupt is disabled Mask control for the associated interrupt source in the IRQ controller
2	IRQ2_MSK	0: Interrupt is enabled 1: Interrupt is disabled Mask control for the associated interrupt source in the IRQ controller
1	IRQ1_MSK	0: Interrupt is enabled 1: Interrupt is disabled Mask control for the associated interrupt source in the IRQ controller
0	IRQ0_MSK	0: Interrupt is enabled 1: Interrupt is disabled Mask control for the associated interrupt source in the IRQ controller

151A0074	IRQ_MASKM										FFFFF					
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	IRQ3F_MSK	IRQ3E_MSK	IRQ3D_MSK	IRQ3C_MSK	IRQ3B_MSK	IRQ3A_MSK	IRQ39_MSK	IRQ38_MSK	IRQ37_MSK	IRQ36_MSK	IRQ35_MSK	IRQ34_MSK	IRQ33_MSK	IRQ32_MSK	IRQ31_MSK	IRQ30_MSK

Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IRQ2F_MSK	IRQ2E_MSK	IRQ2D_MSK	IRQ2C_MSK	IRQ2B_MSK	IRQ2A_MSK	IRQ29_MSK	IRQ28_MSK	IRQ27_MSK	IRQ26_MSK	IRQ25_MSK	IRQ24_MSK	IRQ23_MSK	IRQ22_MSK	IRQ21_MSK	IRQ20_MSK
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31	IRQ3F_MSK	Mask control for the associated interrupt source in the IRQ controller 0: Interrupt is enabled 1: Interrupt is disabled
30	IRQ3E_MSK	Mask control for the associated interrupt source in the IRQ controller 0: Interrupt is enabled 1: Interrupt is disabled
29	IRQ3D_MSK	Mask control for the associated interrupt source in the IRQ controller 0: Interrupt is enabled 1: Interrupt is disabled
28	IRQ3C_MSK	Mask control for the associated interrupt source in the IRQ controller 0: Interrupt is enabled 1: Interrupt is disabled
27	IRQ3B_MSK	Mask control for the associated interrupt source in the IRQ controller 0: Interrupt is enabled 1: Interrupt is disabled
26	IRQ3A_MSK	Mask control for the associated interrupt source in the IRQ controller 0: Interrupt is enabled 1: Interrupt is disabled
25	IRQ39_MSK	Mask control for the associated interrupt source in the IRQ controller 0: Interrupt is enabled 1: Interrupt is disabled
24	IRQ38_MSK	Mask control for the associated interrupt source in the IRQ controller 0: Interrupt is enabled 1: Interrupt is disabled
23	IRQ37_MSK	Mask control for the associated interrupt source in the IRQ controller 0: Interrupt is enabled 1: Interrupt is disabled
22	IRQ36_MSK	Mask control for the associated interrupt source in the IRQ controller 0: Interrupt is enabled 1: Interrupt is disabled
21	IRQ35_MSK	Mask control for the associated interrupt source in the IRQ controller 0: Interrupt is enabled 1: Interrupt is disabled
20	IRQ34_MSK	Mask control for the associated interrupt source in the IRQ controller 0: Interrupt is enabled 1: Interrupt is disabled
19	IRQ33_MSK	Mask control for the associated interrupt source in the IRQ controller 0: Interrupt is enabled 1: Interrupt is disabled
18	IRQ32_MSK	Mask control for the associated interrupt source in the IRQ controller

Bit(s)	Name	Description
17	IRQ31_MSK	0: Interrupt is enabled 1: Interrupt is disabled Mask control for the associated interrupt source in the IRQ controller
16	IRQ30_MSK	0: Interrupt is enabled 1: Interrupt is disabled Mask control for the associated interrupt source in the IRQ controller
15	IRQ2F_MSK	0: Interrupt is enabled 1: Interrupt is disabled Mask control for the associated interrupt source in the IRQ controller
14	IRQ2E_MSK	0: Interrupt is enabled 1: Interrupt is disabled Mask control for the associated interrupt source in the IRQ controller
13	IRQ2D_MSK	0: Interrupt is enabled 1: Interrupt is disabled Mask control for the associated interrupt source in the IRQ controller
12	IRQ2C_MSK	0: Interrupt is enabled 1: Interrupt is disabled Mask control for the associated interrupt source in the IRQ controller
11	IRQ2B_MSK	0: Interrupt is enabled 1: Interrupt is disabled Mask control for the associated interrupt source in the IRQ controller
10	IRQ2A_MSK	0: Interrupt is enabled 1: Interrupt is disabled Mask control for the associated interrupt source in the IRQ controller
9	IRQ29_MSK	0: Interrupt is enabled 1: Interrupt is disabled Mask control for the associated interrupt source in the IRQ controller
8	IRQ28_MSK	0: Interrupt is enabled 1: Interrupt is disabled Mask control for the associated interrupt source in the IRQ controller
7	IRQ27_MSK	0: Interrupt is enabled 1: Interrupt is disabled Mask control for the associated interrupt source in the IRQ controller
6	IRQ26_MSK	0: Interrupt is enabled 1: Interrupt is disabled Mask control for the associated interrupt source in the IRQ controller
5	IRQ25_MSK	0: Interrupt is enabled 1: Interrupt is disabled Mask control for the associated interrupt source in the IRQ controller
4	IRQ24_MSK	0: Interrupt is enabled 1: Interrupt is disabled Mask control for the associated interrupt source in the IRQ controller
3	IRQ23_MSK	0: Interrupt is enabled 1: Interrupt is disabled Mask control for the associated interrupt source in the IRQ controller
2	IRQ22_MSK	0: Interrupt is enabled 1: Interrupt is disabled Mask control for the associated interrupt source in the IRQ controller
1	IRQ21_MSK	0: Interrupt is enabled 1: Interrupt is disabled Mask control for the associated interrupt source in the IRQ controller

Bit(s)	Name	Description
0	IRQ20_MSK	Mask control for the associated interrupt source in the IRQ controller 0: Interrupt is enabled 1: Interrupt is disabled

151A0080 IRQ_MASK_CLR IRQ Mask Clear Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	IRQ1F_MCLR	IRQ1E_MCLR	IRQ1D_MCLR	IRQ1C_MCLR	IRQ1B_MCLR	IRQ1A_MCLR	IRQ19_MCLR	IRQ18_MCLR	IRQ17_MCLR	IRQ16_MCLR	IRQ15_MCLR	IRQ14_MCLR	IRQ13_MCLR	IRQ12_MCLR	IRQ11_MCLR	IRQ10_MCLR
Type	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IRQF_MCLR	IRQE_MCLR	IRQD_MCLR	IRQC_MCLR	IRQB_MCLR	IRQA_MCLR	IRQ9_MCLR	IRQ8_MCLR	IRQ7_MCLR	IRQ6_MCLR	IRQ5_MCLR	IRQ4_MCLR	IRQ3_MCLR	IRQ2_MCLR	IRQ1_MCLR	IRQ0_MCLR
Type	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	IRQ1F_MCLR	Clear corresponding bits in IRQ Mask Register. 0: No effect 1: Disable the corresponding MASK bit
30	IRQ1E_MCLR	Clear corresponding bits in IRQ Mask Register. 0: No effect 1: Disable the corresponding MASK bit
29	IRQ1D_MCLR	Clear corresponding bits in IRQ Mask Register. 0: No effect 1: Disable the corresponding MASK bit
28	IRQ1C_MCLR	Clear corresponding bits in IRQ Mask Register. 0: No effect 1: Disable the corresponding MASK bit
27	IRQ1B_MCLR	Clear corresponding bits in IRQ Mask Register. 0: No effect 1: Disable the corresponding MASK bit
26	IRQ1A_MCLR	Clear corresponding bits in IRQ Mask Register. 0: No effect 1: Disable the corresponding MASK bit
25	IRQ19_MCLR	Clear corresponding bits in IRQ Mask Register. 0: No effect 1: Disable the corresponding MASK bit
24	IRQ18_MCLR	Clear corresponding bits in IRQ Mask Register. 0: No effect 1: Disable the corresponding MASK bit
23	IRQ17_MCLR	Clear corresponding bits in IRQ Mask Register. 0: No effect 1: Disable the corresponding MASK bit

Bit(s)	Name	Description
22	IRQ16_MCLR	Clear corresponding bits in IRQ Mask Register. 0: No effect 1: Disable the corresponding MASK bit
21	IRQ15_MCLR	Clear corresponding bits in IRQ Mask Register. 0: No effect 1: Disable the corresponding MASK bit
20	IRQ14_MCLR	Clear corresponding bits in IRQ Mask Register. 0: No effect 1: Disable the corresponding MASK bit
19	IRQ13_MCLR	Clear corresponding bits in IRQ Mask Register. 0: No effect 1: Disable the corresponding MASK bit
18	IRQ12_MCLR	Clear corresponding bits in IRQ Mask Register. 0: No effect 1: Disable the corresponding MASK bit
17	IRQ11_MCLR	Clear corresponding bits in IRQ Mask Register. 0: No effect 1: Disable the corresponding MASK bit
16	IRQ10_MCLR	Clear corresponding bits in IRQ Mask Register. 0: No effect 1: Disable the corresponding MASK bit
15	IRQF_MCLR	Clear corresponding bits in IRQ Mask Register. 0: No effect 1: Disable the corresponding MASK bit
14	IRQE_MCLR	Clear corresponding bits in IRQ Mask Register. 0: No effect 1: Disable the corresponding MASK bit
13	IRQD_MCLR	Clear corresponding bits in IRQ Mask Register. 0: No effect 1: Disable the corresponding MASK bit
12	IRQC_MCLR	Clear corresponding bits in IRQ Mask Register. 0: No effect 1: Disable the corresponding MASK bit
11	IRQB_MCLR	Clear corresponding bits in IRQ Mask Register. 0: No effect 1: Disable the corresponding MASK bit
10	IRQA_MCLR	Clear corresponding bits in IRQ Mask Register. 0: No effect 1: Disable the corresponding MASK bit
9	IRQ9_MCLR	Clear corresponding bits in IRQ Mask Register. 0: No effect 1: Disable the corresponding MASK bit
8	IRQ8_MCLR	Clear corresponding bits in IRQ Mask Register. 0: No effect 1: Disable the corresponding MASK bit
7	IRQ7_MCLR	Clear corresponding bits in IRQ Mask Register. 0: No effect 1: Disable the corresponding MASK bit
6	IRQ6_MCLR	Clear corresponding bits in IRQ Mask Register. 0: No effect 1: Disable the corresponding MASK bit
5	IRQ5_MCLR	Clear corresponding bits in IRQ Mask Register. 0: No effect 1: Disable the corresponding MASK bit

Bit(s)	Name	Description
4	IRQ4_MCLR	1: Disable the corresponding MASK bit Clear corresponding bits in IRQ Mask Register. 0: No effect
3	IRQ3_MCLR	1: Disable the corresponding MASK bit Clear corresponding bits in IRQ Mask Register. 0: No effect
2	IRQ2_MCLR	1: Disable the corresponding MASK bit Clear corresponding bits in IRQ Mask Register. 0: No effect
1	IRQ1_MCLR	1: Disable the corresponding MASK bit Clear corresponding bits in IRQ Mask Register. 0: No effect
0	IRQ0_MCLR	1: Disable the corresponding MASK bit Clear corresponding bits in IRQ Mask Register. 0: No effect 1: Disable the corresponding MASK bit

151A0084 IRQ_MASK_CLRM IRQ Mask Clear Register Middle 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	IRQ3F_MCLR	IRQ3E_MCLR	IRQ3D_MCLR	IRQ3C_MCLR	IRQ3B_MCLR	IRQ3A_MCLR	IRQ39_MCLR	IRQ38_MCLR	IRQ37_MCLR	IRQ36_MCLR	IRQ35_MCLR	IRQ34_MCLR	IRQ33_MCLR	IRQ32_MCLR	IRQ31_MCLR	IRQ30_MCLR
Type	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IRQ2F_MCLR	IRQ2E_MCLR	IRQ2D_MCLR	IRQ2C_MCLR	IRQ2B_MCLR	IRQ2A_MCLR	IRQ29_MCLR	IRQ28_MCLR	IRQ27_MCLR	IRQ26_MCLR	IRQ25_MCLR	IRQ24_MCLR	IRQ23_MCLR	IRQ22_MCLR	IRQ21_MCLR	IRQ20_MCLR
Type	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	IRQ3F_MCLR	Clear corresponding bits in IRQ Mask Register. 0: No effect
30	IRQ3E_MCLR	1: Disable the corresponding MASK bit Clear corresponding bits in IRQ Mask Register. 0: No effect
29	IRQ3D_MCLR	1: Disable the corresponding MASK bit Clear corresponding bits in IRQ Mask Register. 0: No effect
28	IRQ3C_MCLR	1: Disable the corresponding MASK bit Clear corresponding bits in IRQ Mask Register. 0: No effect
27	IRQ3B_MCLR	1: Disable the corresponding MASK bit Clear corresponding bits in IRQ Mask Register. 0: No effect

Bit(s)	Name	Description
26	IRQ3A_MCLR	1: Disable the corresponding MASK bit Clear corresponding bits in IRQ Mask Register. 0: No effect
25	IRQ39_MCLR	1: Disable the corresponding MASK bit Clear corresponding bits in IRQ Mask Register. 0: No effect
24	IRQ38_MCLR	1: Disable the corresponding MASK bit Clear corresponding bits in IRQ Mask Register. 0: No effect
23	IRQ37_MCLR	1: Disable the corresponding MASK bit Clear corresponding bits in IRQ Mask Register. 0: No effect
22	IRQ36_MCLR	1: Disable the corresponding MASK bit Clear corresponding bits in IRQ Mask Register. 0: No effect
21	IRQ35_MCLR	1: Disable the corresponding MASK bit Clear corresponding bits in IRQ Mask Register. 0: No effect
20	IRQ34_MCLR	1: Disable the corresponding MASK bit Clear corresponding bits in IRQ Mask Register. 0: No effect
19	IRQ33_MCLR	1: Disable the corresponding MASK bit Clear corresponding bits in IRQ Mask Register. 0: No effect
18	IRQ32_MCLR	1: Disable the corresponding MASK bit Clear corresponding bits in IRQ Mask Register. 0: No effect
17	IRQ31_MCLR	1: Disable the corresponding MASK bit Clear corresponding bits in IRQ Mask Register. 0: No effect
16	IRQ30_MCLR	1: Disable the corresponding MASK bit Clear corresponding bits in IRQ Mask Register. 0: No effect
15	IRQ2F_MCLR	1: Disable the corresponding MASK bit Clear corresponding bits in IRQ Mask Register. 0: No effect
14	IRQ2E_MCLR	1: Disable the corresponding MASK bit Clear corresponding bits in IRQ Mask Register. 0: No effect
13	IRQ2D_MCLR	1: Disable the corresponding MASK bit Clear corresponding bits in IRQ Mask Register. 0: No effect
12	IRQ2C_MCLR	1: Disable the corresponding MASK bit Clear corresponding bits in IRQ Mask Register. 0: No effect
11	IRQ2B_MCLR	1: Disable the corresponding MASK bit Clear corresponding bits in IRQ Mask Register. 0: No effect
10	IRQ2A_MCLR	1: Disable the corresponding MASK bit Clear corresponding bits in IRQ Mask Register. 0: No effect
9	IRQ29_MCLR	1: Disable the corresponding MASK bit Clear corresponding bits in IRQ Mask Register.

Bit(s)	Name	Description
8	IRQ28_MCLR	0: No effect 1: Disable the corresponding MASK bit Clear corresponding bits in IRQ Mask Register.
7	IRQ27_MCLR	0: No effect 1: Disable the corresponding MASK bit Clear corresponding bits in IRQ Mask Register.
6	IRQ26_MCLR	0: No effect 1: Disable the corresponding MASK bit Clear corresponding bits in IRQ Mask Register.
5	IRQ25_MCLR	0: No effect 1: Disable the corresponding MASK bit Clear corresponding bits in IRQ Mask Register.
4	IRQ24_MCLR	0: No effect 1: Disable the corresponding MASK bit Clear corresponding bits in IRQ Mask Register.
3	IRQ23_MCLR	0: No effect 1: Disable the corresponding MASK bit Clear corresponding bits in IRQ Mask Register.
2	IRQ22_MCLR	0: No effect 1: Disable the corresponding MASK bit Clear corresponding bits in IRQ Mask Register.
1	IRQ21_MCLR	0: No effect 1: Disable the corresponding MASK bit Clear corresponding bits in IRQ Mask Register.
0	IRQ20_MCLR	0: No effect 1: Disable the corresponding MASK bit Clear corresponding bits in IRQ Mask Register.

151A0090 IRQ_MASK_SET IRQ Mask Set Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	IRQ1F_MSET	IRQ1E_MSET	IRQ1D_MSET	IRQ1C_MSET	IRQ1B_MSET	IRQ1A_MSET	IRQ19_MSET	IRQ18_MSET	IRQ17_MSET	IRQ16_MSET	IRQ15_MSET	IRQ14_MSET	IRQ13_MSET	IRQ12_MSET	IRQ11_MSET	IRQ10_MSET
Type	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IRQF_MSET	IRQE_MSET	IRQD_MSET	IRQC_MSET	IRQB_MSET	IRQA_MSET	IRQ9_MSET	IRQ8_MSET	IRQ7_MSET	IRQ6_MSET	IRQ5_MSET	IRQ4_MSET	IRQ3_MSET	IRQ2_MSET	IRQ1_MSET	IRQ0_MSET
Type	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	IRQ1F_MSET	Set corresponding bits in IRQ Mask Register.

Bit(s)	Name	Description
30	IRQ1E_MSET	0: No effect 1: Enable corresponding MASK bit Set corresponding bits in IRQ Mask Register.
29	IRQ1D_MSET	0: No effect 1: Enable corresponding MASK bit Set corresponding bits in IRQ Mask Register.
28	IRQ1C_MSET	0: No effect 1: Enable corresponding MASK bit Set corresponding bits in IRQ Mask Register.
27	IRQ1B_MSET	0: No effect 1: Enable corresponding MASK bit Set corresponding bits in IRQ Mask Register.
26	IRQ1A_MSET	0: No effect 1: Enable corresponding MASK bit Set corresponding bits in IRQ Mask Register.
25	IRQ19_MSET	0: No effect 1: Enable corresponding MASK bit Set corresponding bits in IRQ Mask Register.
24	IRQ18_MSET	0: No effect 1: Enable corresponding MASK bit Set corresponding bits in IRQ Mask Register.
23	IRQ17_MSET	0: No effect 1: Enable corresponding MASK bit Set corresponding bits in IRQ Mask Register.
22	IRQ16_MSET	0: No effect 1: Enable corresponding MASK bit Set corresponding bits in IRQ Mask Register.
21	IRQ15_MSET	0: No effect 1: Enable corresponding MASK bit Set corresponding bits in IRQ Mask Register.
20	IRQ14_MSET	0: No effect 1: Enable corresponding MASK bit Set corresponding bits in IRQ Mask Register.
19	IRQ13_MSET	0: No effect 1: Enable corresponding MASK bit Set corresponding bits in IRQ Mask Register.
18	IRQ12_MSET	0: No effect 1: Enable corresponding MASK bit Set corresponding bits in IRQ Mask Register.
17	IRQ11_MSET	0: No effect 1: Enable corresponding MASK bit Set corresponding bits in IRQ Mask Register.
16	IRQ10_MSET	0: No effect 1: Enable corresponding MASK bit Set corresponding bits in IRQ Mask Register.
15	IRQF_MSET	0: No effect 1: Enable corresponding MASK bit Set corresponding bits in IRQ Mask Register.
14	IRQE_MSET	0: No effect 1: Enable corresponding MASK bit Set corresponding bits in IRQ Mask Register.

Bit(s)	Name	Description
13	IRQD_MSET	Set corresponding bits in IRQ Mask Register. 0: No effect 1: Enable corresponding MASK bit
12	IRQC_MSET	Set corresponding bits in IRQ Mask Register. 0: No effect 1: Enable corresponding MASK bit
11	IRQB_MSET	Set corresponding bits in IRQ Mask Register. 0: No effect 1: Enable corresponding MASK bit
10	IRQA_MSET	Set corresponding bits in IRQ Mask Register. 0: No effect 1: Enable corresponding MASK bit
9	IRQ9_MSET	Set corresponding bits in IRQ Mask Register. 0: No effect 1: Enable corresponding MASK bit
8	IRQ8_MSET	Set corresponding bits in IRQ Mask Register. 0: No effect 1: Enable corresponding MASK bit
7	IRQ7_MSET	Set corresponding bits in IRQ Mask Register. 0: No effect 1: Enable corresponding MASK bit
6	IRQ6_MSET	Set corresponding bits in IRQ Mask Register. 0: No effect 1: Enable corresponding MASK bit
5	IRQ5_MSET	Set corresponding bits in IRQ Mask Register. 0: No effect 1: Enable corresponding MASK bit
4	IRQ4_MSET	Set corresponding bits in IRQ Mask Register. 0: No effect 1: Enable corresponding MASK bit
3	IRQ3_MSET	Set corresponding bits in IRQ Mask Register. 0: No effect 1: Enable corresponding MASK bit
2	IRQ2_MSET	Set corresponding bits in IRQ Mask Register. 0: No effect 1: Enable corresponding MASK bit
1	IRQ1_MSET	Set corresponding bits in IRQ Mask Register. 0: No effect 1: Enable corresponding MASK bit
0	IRQ0_MSET	Set corresponding bits in IRQ Mask Register. 0: No effect 1: Enable corresponding MASK bit

151A0094	IRQ_MASK_SETM				IRQ Mask Set Register Middle								00000000			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	IRQ3F_MSET	IRQ3E_MSET	IRQ3D_MSET	IRQ3C_MSET	IRQ3B_MSET	IRQ3A_MSET	IRQ39_MSET	IRQ38_MSET	IRQ37_MSET	IRQ36_MSET	IRQ35_MSET	IRQ34_MSET	IRQ33_MSET	IRQ32_MSET	IRQ31_MSET	IRQ30_MSET
Type	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IRQ2F_MSET	IRQ2E_MSET	IRQ2D_MSET	IRQ2C_MSET	IRQ2B_MSET	IRQ2A_MSET	IRQ29_MSET	IRQ28_MSET	IRQ27_MSET	IRQ26_MSET	IRQ25_MSET	IRQ24_MSET	IRQ23_MSET	IRQ22_MSET	IRQ21_MSET	IRQ20_MSET
Type	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	IRQ3F_MSET	Set corresponding bits in IRQ Mask Register. 0: No effect 1: Enable corresponding MASK bit
30	IRQ3E_MSET	Set corresponding bits in IRQ Mask Register. 0: No effect 1: Enable corresponding MASK bit
29	IRQ3D_MSET	Set corresponding bits in IRQ Mask Register. 0: No effect 1: Enable corresponding MASK bit
28	IRQ3C_MSET	Set corresponding bits in IRQ Mask Register. 0: No effect 1: Enable corresponding MASK bit
27	IRQ3B_MSET	Set corresponding bits in IRQ Mask Register. 0: No effect 1: Enable corresponding MASK bit
26	IRQ3A_MSET	Set corresponding bits in IRQ Mask Register. 0: No effect 1: Enable corresponding MASK bit
25	IRQ39_MSET	Set corresponding bits in IRQ Mask Register. 0: No effect 1: Enable corresponding MASK bit
24	IRQ38_MSET	Set corresponding bits in IRQ Mask Register. 0: No effect 1: Enable corresponding MASK bit
23	IRQ37_MSET	Set corresponding bits in IRQ Mask Register. 0: No effect 1: Enable corresponding MASK bit
22	IRQ36_MSET	Set corresponding bits in IRQ Mask Register. 0: No effect 1: Enable corresponding MASK bit
21	IRQ35_MSET	Set corresponding bits in IRQ Mask Register. 0: No effect 1: Enable corresponding MASK bit
20	IRQ34_MSET	Set corresponding bits in IRQ Mask Register. 0: No effect 1: Enable corresponding MASK bit
19	IRQ33_MSET	Set corresponding bits in IRQ Mask Register. 0: No effect 1: Enable corresponding MASK bit
18	IRQ32_MSET	Set corresponding bits in IRQ Mask Register. 0: No effect 1: Enable corresponding MASK bit

Bit(s)	Name	Description
17	IRQ31_MSET	Set corresponding bits in IRQ Mask Register. 0: No effect 1: Enable corresponding MASK bit
16	IRQ30_MSET	Set corresponding bits in IRQ Mask Register. 0: No effect 1: Enable corresponding MASK bit
15	IRQ2F_MSET	Set corresponding bits in IRQ Mask Register. 0: No effect 1: Enable corresponding MASK bit
14	IRQ2E_MSET	Set corresponding bits in IRQ Mask Register. 0: No effect 1: Enable corresponding MASK bit
13	IRQ2D_MSET	Set corresponding bits in IRQ Mask Register. 0: No effect 1: Enable corresponding MASK bit
12	IRQ2C_MSET	Set corresponding bits in IRQ Mask Register. 0: No effect 1: Enable corresponding MASK bit
11	IRQ2B_MSET	Set corresponding bits in IRQ Mask Register. 0: No effect 1: Enable corresponding MASK bit
10	IRQ2A_MSET	Set corresponding bits in IRQ Mask Register. 0: No effect 1: Enable corresponding MASK bit
9	IRQ29_MSET	Set corresponding bits in IRQ Mask Register. 0: No effect 1: Enable corresponding MASK bit
8	IRQ28_MSET	Set corresponding bits in IRQ Mask Register. 0: No effect 1: Enable corresponding MASK bit
7	IRQ27_MSET	Set corresponding bits in IRQ Mask Register. 0: No effect 1: Enable corresponding MASK bit
6	IRQ26_MSET	Set corresponding bits in IRQ Mask Register. 0: No effect 1: Enable corresponding MASK bit
5	IRQ25_MSET	Set corresponding bits in IRQ Mask Register. 0: No effect 1: Enable corresponding MASK bit
4	IRQ24_MSET	Set corresponding bits in IRQ Mask Register. 0: No effect 1: Enable corresponding MASK bit
3	IRQ23_MSET	Set corresponding bits in IRQ Mask Register. 0: No effect 1: Enable corresponding MASK bit
2	IRQ22_MSET	Set corresponding bits in IRQ Mask Register. 0: No effect 1: Enable corresponding MASK bit
1	IRQ21_MSET	Set corresponding bits in IRQ Mask Register. 0: No effect 1: Enable corresponding MASK bit
0	IRQ20_MSET	Set corresponding bits in IRQ Mask Register. 0: No effect 1: Enable corresponding MASK bit

Bit(s)	Name	Description
		1: Enable corresponding MASK bit

151A00A0 IRQ_EOI IRQ End of Interrupt Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	IRQ1F_EOI	IRQ1E_EOI	IRQ1D_EOI	IRQ1C_EOI	IRQ1B_EOI	IRQ1A_EOI	IRQ19_EOI	IRQ18_EOI	IRQ17_EOI	IRQ16_EOI	IRQ15_EOI	IRQ14_EOI	IRQ13_EOI	IRQ12_EOI	IRQ11_EOI	IRQ10_EOI
Type	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IRQF_EOI	IRQE_EOI	IRQD_EOI	IRQC_EOI	IRQB_EOI	IRQA_EOI	IRQ9_EOI	IRQ8_EOI	IRQ7_EOI	IRQ6_EOI	IRQ5_EOI	IRQ4_EOI	IRQ3_EOI	IRQ2_EOI	IRQ1_EOI	IRQ0_EOI
Type	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	IRQ1F_EOI	End of Interrupt command for the associated interrupt line. 0: No service is currently in progress or pending 1: Interrupt request is in-service
30	IRQ1E_EOI	End of Interrupt command for the associated interrupt line. 0: No service is currently in progress or pending 1: Interrupt request is in-service
29	IRQ1D_EOI	End of Interrupt command for the associated interrupt line. 0: No service is currently in progress or pending 1: Interrupt request is in-service
28	IRQ1C_EOI	End of Interrupt command for the associated interrupt line. 0: No service is currently in progress or pending 1: Interrupt request is in-service
27	IRQ1B_EOI	End of Interrupt command for the associated interrupt line. 0: No service is currently in progress or pending 1: Interrupt request is in-service
26	IRQ1A_EOI	End of Interrupt command for the associated interrupt line. 0: No service is currently in progress or pending 1: Interrupt request is in-service
25	IRQ19_EOI	End of Interrupt command for the associated interrupt line. 0: No service is currently in progress or pending 1: Interrupt request is in-service
24	IRQ18_EOI	End of Interrupt command for the associated interrupt line. 0: No service is currently in progress or pending 1: Interrupt request is in-service
23	IRQ17_EOI	End of Interrupt command for the associated interrupt line. 0: No service is currently in progress or pending 1: Interrupt request is in-service
22	IRQ16_EOI	End of Interrupt command for the associated interrupt line. 0: No service is currently in progress or pending

Bit(s)	Name	Description
21	IRQ15_EOI	1: Interrupt request is in-service End of Interrupt command for the associated interrupt line. 0: No service is currently in progress or pending
20	IRQ14_EOI	1: Interrupt request is in-service End of Interrupt command for the associated interrupt line. 0: No service is currently in progress or pending
19	IRQ13_EOI	1: Interrupt request is in-service End of Interrupt command for the associated interrupt line. 0: No service is currently in progress or pending
18	IRQ12_EOI	1: Interrupt request is in-service End of Interrupt command for the associated interrupt line. 0: No service is currently in progress or pending
17	IRQ11_EOI	1: Interrupt request is in-service End of Interrupt command for the associated interrupt line. 0: No service is currently in progress or pending
16	IRQ10_EOI	1: Interrupt request is in-service End of Interrupt command for the associated interrupt line. 0: No service is currently in progress or pending
15	IRQF_EOI	1: Interrupt request is in-service End of Interrupt command for the associated interrupt line. 0: No service is currently in progress or pending
14	IRQE_EOI	1: Interrupt request is in-service End of Interrupt command for the associated interrupt line. 0: No service is currently in progress or pending
13	IRQD_EOI	1: Interrupt request is in-service End of Interrupt command for the associated interrupt line. 0: No service is currently in progress or pending
12	IRQC_EOI	1: Interrupt request is in-service End of Interrupt command for the associated interrupt line. 0: No service is currently in progress or pending
11	IRQB_EOI	1: Interrupt request is in-service End of Interrupt command for the associated interrupt line. 0: No service is currently in progress or pending
10	IRQA_EOI	1: Interrupt request is in-service End of Interrupt command for the associated interrupt line. 0: No service is currently in progress or pending
9	IRQ9_EOI	1: Interrupt request is in-service End of Interrupt command for the associated interrupt line. 0: No service is currently in progress or pending
8	IRQ8_EOI	1: Interrupt request is in-service End of Interrupt command for the associated interrupt line. 0: No service is currently in progress or pending
7	IRQ7_EOI	1: Interrupt request is in-service End of Interrupt command for the associated interrupt line. 0: No service is currently in progress or pending
6	IRQ6_EOI	1: Interrupt request is in-service End of Interrupt command for the associated interrupt line. 0: No service is currently in progress or pending
5	IRQ5_EOI	1: Interrupt request is in-service End of Interrupt command for the associated interrupt line. 0: No service is currently in progress or pending
4	IRQ4_EOI	1: Interrupt request is in-service End of Interrupt command for the associated interrupt line.

Bit(s)	Name	Description
3	IRQ3_EOI	0: No service is currently in progress or pending 1: Interrupt request is in-service End of Interrupt command for the associated interrupt line.
2	IRQ2_EOI	0: No service is currently in progress or pending 1: Interrupt request is in-service End of Interrupt command for the associated interrupt line.
1	IRQ1_EOI	0: No service is currently in progress or pending 1: Interrupt request is in-service End of Interrupt command for the associated interrupt line.
0	IRQ0_EOI	0: No service is currently in progress or pending 1: Interrupt request is in-service End of Interrupt command for the associated interrupt line.

151A00A4 IRQ_EOIM IRQ End of Interrupt Register Middle 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	IRQ3F_EOI	IRQ3E_EOI	IRQ3D_EOI	IRQ3C_EOI	IRQ3B_EOI	IRQ3A_EOI	IRQ39_EOI	IRQ38_EOI	IRQ37_EOI	IRQ36_EOI	IRQ35_EOI	IRQ34_EOI	IRQ33_EOI	IRQ32_EOI	IRQ31_EOI	IRQ30_EOI
Type	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IRQ2F_EOI	IRQ2E_EOI	IRQ2D_EOI	IRQ2C_EOI	IRQ2B_EOI	IRQ2A_EOI	IRQ29_EOI	IRQ28_EOI	IRQ27_EOI	IRQ26_EOI	IRQ25_EOI	IRQ24_EOI	IRQ23_EOI	IRQ22_EOI	IRQ21_EOI	IRQ20_EOI
Type	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	IRQ3F_EOI	End of Interrupt command for the associated interrupt line. 0: No service is currently in progress or pending 1: Interrupt request is in-service
30	IRQ3E_EOI	End of Interrupt command for the associated interrupt line. 0: No service is currently in progress or pending 1: Interrupt request is in-service
29	IRQ3D_EOI	End of Interrupt command for the associated interrupt line. 0: No service is currently in progress or pending 1: Interrupt request is in-service
28	IRQ3C_EOI	End of Interrupt command for the associated interrupt line. 0: No service is currently in progress or pending 1: Interrupt request is in-service
27	IRQ3B_EOI	End of Interrupt command for the associated interrupt line. 0: No service is currently in progress or pending 1: Interrupt request is in-service
26	IRQ3A_EOI	End of Interrupt command for the associated interrupt line. 0: No service is currently in progress or pending 1: Interrupt request is in-service

Bit(s)	Name	Description
25	IRQ39_EOI	0: No service is currently in progress or pending 1: Interrupt request is in-service End of Interrupt command for the associated interrupt line.
24	IRQ38_EOI	0: No service is currently in progress or pending 1: Interrupt request is in-service End of Interrupt command for the associated interrupt line.
23	IRQ37_EOI	0: No service is currently in progress or pending 1: Interrupt request is in-service End of Interrupt command for the associated interrupt line.
22	IRQ36_EOI	0: No service is currently in progress or pending 1: Interrupt request is in-service End of Interrupt command for the associated interrupt line.
21	IRQ35_EOI	0: No service is currently in progress or pending 1: Interrupt request is in-service End of Interrupt command for the associated interrupt line.
20	IRQ34_EOI	0: No service is currently in progress or pending 1: Interrupt request is in-service End of Interrupt command for the associated interrupt line.
19	IRQ33_EOI	0: No service is currently in progress or pending 1: Interrupt request is in-service End of Interrupt command for the associated interrupt line.
18	IRQ32_EOI	0: No service is currently in progress or pending 1: Interrupt request is in-service End of Interrupt command for the associated interrupt line.
17	IRQ31_EOI	0: No service is currently in progress or pending 1: Interrupt request is in-service End of Interrupt command for the associated interrupt line.
16	IRQ30_EOI	0: No service is currently in progress or pending 1: Interrupt request is in-service End of Interrupt command for the associated interrupt line.
15	IRQ2F_EOI	0: No service is currently in progress or pending 1: Interrupt request is in-service End of Interrupt command for the associated interrupt line.
14	IRQ2E_EOI	0: No service is currently in progress or pending 1: Interrupt request is in-service End of Interrupt command for the associated interrupt line.
13	IRQ2D_EOI	0: No service is currently in progress or pending 1: Interrupt request is in-service End of Interrupt command for the associated interrupt line.
12	IRQ2C_EOI	0: No service is currently in progress or pending 1: Interrupt request is in-service End of Interrupt command for the associated interrupt line.
11	IRQ2B_EOI	0: No service is currently in progress or pending 1: Interrupt request is in-service End of Interrupt command for the associated interrupt line.
10	IRQ2A_EOI	0: No service is currently in progress or pending 1: Interrupt request is in-service End of Interrupt command for the associated interrupt line.
9	IRQ29_EOI	0: No service is currently in progress or pending 1: Interrupt request is in-service End of Interrupt command for the associated interrupt line.

Bit(s)	Name	Description
8	IRQ28_EOI	End of Interrupt command for the associated interrupt line. 0: No service is currently in progress or pending 1: Interrupt request is in-service
7	IRQ27_EOI	End of Interrupt command for the associated interrupt line. 0: No service is currently in progress or pending 1: Interrupt request is in-service
6	IRQ26_EOI	End of Interrupt command for the associated interrupt line. 0: No service is currently in progress or pending 1: Interrupt request is in-service
5	IRQ25_EOI	End of Interrupt command for the associated interrupt line. 0: No service is currently in progress or pending 1: Interrupt request is in-service
4	IRQ24_EOI	End of Interrupt command for the associated interrupt line. 0: No service is currently in progress or pending 1: Interrupt request is in-service
3	IRQ23_EOI	End of Interrupt command for the associated interrupt line. 0: No service is currently in progress or pending 1: Interrupt request is in-service
2	IRQ22_EOI	End of Interrupt command for the associated interrupt line. 0: No service is currently in progress or pending 1: Interrupt request is in-service
1	IRQ21_EOI	End of Interrupt command for the associated interrupt line. 0: No service is currently in progress or pending 1: Interrupt request is in-service
0	IRQ20_EOI	End of Interrupt command for the associated interrupt line. 0: No service is currently in progress or pending 1: Interrupt request is in-service

151A00B0				IRQ_SENS				IRQ Sensitive Register								00000000			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16			
Name	IRQ1F_SENS	IRQ1E_SENS	IRQ1D_SENS	IRQ1C_SENS	IRQ1B_SENS	IRQ1A_SENS	IRQ19_SENS	IRQ18_SENS	IRQ17_SENS	IRQ16_SENS	IRQ15_SENS	IRQ14_SENS	IRQ13_SENS	IRQ12_SENS	IRQ11_SENS	IRQ10_SENS			
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0			
Name	IRQF_SENS	IRQE_SENS	IRQD_SENS	IRQC_SENS	IRQB_SENS	IRQA_SENS	IRQ9_SENS	IRQ8_SENS	IRQ7_SENS	IRQ6_SENS	IRQ5_SENS	IRQ4_SENS	IRQ3_SENS	IRQ2_SENS	IRQ1_SENS	IRQ0_SENS			
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			

Bit(s)	Name	Description
31	IRQ1F_SENS	Sensitivity type of the associated Interrupt Source 0: Edge sensitivity with active LOW 1: Level sensitivity with active LOW

Bit(s)	Name	Description
30	IRQ1E_SENS	Sensitivity type of the associated Interrupt Source 0: Edge sensitivity with active LOW 1: Level sensitivity with active LOW
29	IRQ1D_SENS	Sensitivity type of the associated Interrupt Source 0: Edge sensitivity with active LOW 1: Level sensitivity with active LOW
28	IRQ1C_SENS	Sensitivity type of the associated Interrupt Source 0: Edge sensitivity with active LOW 1: Level sensitivity with active LOW
27	IRQ1B_SENS	Sensitivity type of the associated Interrupt Source 0: Edge sensitivity with active LOW 1: Level sensitivity with active LOW
26	IRQ1A_SENS	Sensitivity type of the associated Interrupt Source 0: Edge sensitivity with active LOW 1: Level sensitivity with active LOW
25	IRQ19_SENS	Sensitivity type of the associated Interrupt Source 0: Edge sensitivity with active LOW 1: Level sensitivity with active LOW
24	IRQ18_SENS	Sensitivity type of the associated Interrupt Source 0: Edge sensitivity with active LOW 1: Level sensitivity with active LOW
23	IRQ17_SENS	Sensitivity type of the associated Interrupt Source 0: Edge sensitivity with active LOW 1: Level sensitivity with active LOW
22	IRQ16_SENS	Sensitivity type of the associated Interrupt Source 0: Edge sensitivity with active LOW 1: Level sensitivity with active LOW
21	IRQ15_SENS	Sensitivity type of the associated Interrupt Source 0: Edge sensitivity with active LOW 1: Level sensitivity with active LOW
20	IRQ14_SENS	Sensitivity type of the associated Interrupt Source 0: Edge sensitivity with active LOW 1: Level sensitivity with active LOW
19	IRQ13_SENS	Sensitivity type of the associated Interrupt Source 0: Edge sensitivity with active LOW 1: Level sensitivity with active LOW
18	IRQ12_SENS	Sensitivity type of the associated Interrupt Source 0: Edge sensitivity with active LOW 1: Level sensitivity with active LOW
17	IRQ11_SENS	Sensitivity type of the associated Interrupt Source 0: Edge sensitivity with active LOW 1: Level sensitivity with active LOW
16	IRQ10_SENS	Sensitivity type of the associated Interrupt Source 0: Edge sensitivity with active LOW 1: Level sensitivity with active LOW
15	IRQF_SENS	Sensitivity type of the associated Interrupt Source 0: Edge sensitivity with active LOW 1: Level sensitivity with active LOW
14	IRQE_SENS	Sensitivity type of the associated Interrupt Source 0: Edge sensitivity with active LOW 1: Level sensitivity with active LOW
13	IRQD_SENS	Sensitivity type of the associated Interrupt Source 0: Edge sensitivity with active LOW

Bit(s)	Name	Description
12	IRQC_SENS	1: Level sensitivity with active LOW Sensitivity type of the associated Interrupt Source 0: Edge sensitivity with active LOW
11	IRQB_SENS	1: Level sensitivity with active LOW Sensitivity type of the associated Interrupt Source 0: Edge sensitivity with active LOW
10	IRQA_SENS	1: Level sensitivity with active LOW Sensitivity type of the associated Interrupt Source 0: Edge sensitivity with active LOW
9	IRQ9_SENS	1: Level sensitivity with active LOW Sensitivity type of the associated Interrupt Source 0: Edge sensitivity with active LOW
8	IRQ8_SENS	1: Level sensitivity with active LOW Sensitivity type of the associated Interrupt Source 0: Edge sensitivity with active LOW
7	IRQ7_SENS	1: Level sensitivity with active LOW Sensitivity type of the associated Interrupt Source 0: Edge sensitivity with active LOW
6	IRQ6_SENS	1: Level sensitivity with active LOW Sensitivity type of the associated Interrupt Source 0: Edge sensitivity with active LOW
5	IRQ5_SENS	1: Level sensitivity with active LOW Sensitivity type of the associated Interrupt Source 0: Edge sensitivity with active LOW
4	IRQ4_SENS	1: Level sensitivity with active LOW Sensitivity type of the associated Interrupt Source 0: Edge sensitivity with active LOW
3	IRQ3_SENS	1: Level sensitivity with active LOW Sensitivity type of the associated Interrupt Source 0: Edge sensitivity with active LOW
2	IRQ2_SENS	1: Level sensitivity with active LOW Sensitivity type of the associated Interrupt Source 0: Edge sensitivity with active LOW
1	IRQ1_SENS	1: Level sensitivity with active LOW Sensitivity type of the associated Interrupt Source 0: Edge sensitivity with active LOW
0	IRQ0_SENS	1: Level sensitivity with active LOW Sensitivity type of the associated Interrupt Source 0: Edge sensitivity with active LOW

151A00B4 IRQ_SENSM IRQ Sensitive Register Middle 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	IRQ3F_SENS	IRQ3E_SENS	IRQ3D_SENS	IRQ3C_SENS	IRQ3B_SENS	IRQ3A_SENS	IRQ39_SENS	IRQ38_SENS	IRQ37_SENS	IRQ36_SENS	IRQ35_SENS	IRQ34_SENS	IRQ33_SENS	IRQ32_SENS	IRQ31_SENS	IRQ30_SENS
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IRQ2F_SENS	IRQ2E_SENS	IRQ2D_SENS	IRQ2C_SENS	IRQ2B_SENS	IRQ2A_SENS	IRQ29_SENS	IRQ28_SENS	IRQ27_SENS	IRQ26_SENS	IRQ25_SENS	IRQ24_SENS	IRQ23_SENS	IRQ22_SENS	IRQ21_SENS	IRQ20_SENS
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	IRQ3F_SENS	Sensitivity type of the associated Interrupt Source 0: Edge sensitivity with active LOW 1: Level sensitivity with active LOW
30	IRQ3E_SENS	Sensitivity type of the associated Interrupt Source 0: Edge sensitivity with active LOW 1: Level sensitivity with active LOW
29	IRQ3D_SENS	Sensitivity type of the associated Interrupt Source 0: Edge sensitivity with active LOW 1: Level sensitivity with active LOW
28	IRQ3C_SENS	Sensitivity type of the associated Interrupt Source 0: Edge sensitivity with active LOW 1: Level sensitivity with active LOW
27	IRQ3B_SENS	Sensitivity type of the associated Interrupt Source 0: Edge sensitivity with active LOW 1: Level sensitivity with active LOW
26	IRQ3A_SENS	Sensitivity type of the associated Interrupt Source 0: Edge sensitivity with active LOW 1: Level sensitivity with active LOW
25	IRQ39_SENS	Sensitivity type of the associated Interrupt Source 0: Edge sensitivity with active LOW 1: Level sensitivity with active LOW
24	IRQ38_SENS	Sensitivity type of the associated Interrupt Source 0: Edge sensitivity with active LOW 1: Level sensitivity with active LOW
23	IRQ37_SENS	Sensitivity type of the associated Interrupt Source 0: Edge sensitivity with active LOW 1: Level sensitivity with active LOW
22	IRQ36_SENS	Sensitivity type of the associated Interrupt Source 0: Edge sensitivity with active LOW 1: Level sensitivity with active LOW
21	IRQ35_SENS	Sensitivity type of the associated Interrupt Source 0: Edge sensitivity with active LOW 1: Level sensitivity with active LOW
20	IRQ34_SENS	Sensitivity type of the associated Interrupt Source 0: Edge sensitivity with active LOW 1: Level sensitivity with active LOW
19	IRQ33_SENS	Sensitivity type of the associated Interrupt Source 0: Edge sensitivity with active LOW 1: Level sensitivity with active LOW
18	IRQ32_SENS	Sensitivity type of the associated Interrupt Source 0: Edge sensitivity with active LOW 1: Level sensitivity with active LOW
17	IRQ31_SENS	Sensitivity type of the associated Interrupt Source 0: Edge sensitivity with active LOW

Bit(s)	Name	Description
16	IRQ30_SENS	1: Level sensitivity with active LOW Sensitivity type of the associated Interrupt Source 0: Edge sensitivity with active LOW
15	IRQ2F_SENS	1: Level sensitivity with active LOW Sensitivity type of the associated Interrupt Source 0: Edge sensitivity with active LOW
14	IRQ2E_SENS	1: Level sensitivity with active LOW Sensitivity type of the associated Interrupt Source 0: Edge sensitivity with active LOW
13	IRQ2D_SENS	1: Level sensitivity with active LOW Sensitivity type of the associated Interrupt Source 0: Edge sensitivity with active LOW
12	IRQ2C_SENS	1: Level sensitivity with active LOW Sensitivity type of the associated Interrupt Source 0: Edge sensitivity with active LOW
11	IRQ2B_SENS	1: Level sensitivity with active LOW Sensitivity type of the associated Interrupt Source 0: Edge sensitivity with active LOW
10	IRQ2A_SENS	1: Level sensitivity with active LOW Sensitivity type of the associated Interrupt Source 0: Edge sensitivity with active LOW
9	IRQ29_SENS	1: Level sensitivity with active LOW Sensitivity type of the associated Interrupt Source 0: Edge sensitivity with active LOW
8	IRQ28_SENS	1: Level sensitivity with active LOW Sensitivity type of the associated Interrupt Source 0: Edge sensitivity with active LOW
7	IRQ27_SENS	1: Level sensitivity with active LOW Sensitivity type of the associated Interrupt Source 0: Edge sensitivity with active LOW
6	IRQ26_SENS	1: Level sensitivity with active LOW Sensitivity type of the associated Interrupt Source 0: Edge sensitivity with active LOW
5	IRQ25_SENS	1: Level sensitivity with active LOW Sensitivity type of the associated Interrupt Source 0: Edge sensitivity with active LOW
4	IRQ24_SENS	1: Level sensitivity with active LOW Sensitivity type of the associated Interrupt Source 0: Edge sensitivity with active LOW
3	IRQ23_SENS	1: Level sensitivity with active LOW Sensitivity type of the associated Interrupt Source 0: Edge sensitivity with active LOW
2	IRQ22_SENS	1: Level sensitivity with active LOW Sensitivity type of the associated Interrupt Source 0: Edge sensitivity with active LOW
1	IRQ21_SENS	1: Level sensitivity with active LOW Sensitivity type of the associated Interrupt Source 0: Edge sensitivity with active LOW
0	IRQ20_SENS	1: Level sensitivity with active LOW Sensitivity type of the associated Interrupt Source 0: Edge sensitivity with active LOW

151A00C0 IRQ_SOFT IRQ Software Interrupt Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	IRQ1F_SOFT	IRQ1E_SOFT	IRQ1D_SOFT	IRQ1C_SOFT	IRQ1B_SOFT	IRQ1A_SOFT	IRQ19_SOFT	IRQ18_SOFT	IRQ17_SOFT	IRQ16_SOFT	IRQ15_SOFT	IRQ14_SOFT	IRQ13_SOFT	IRQ12_SOFT	IRQ11_SOFT	IRQ10_SOFT
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IRQF_SOFT	IRQE_SOFT	IRQD_SOFT	IRQC_SOFT	IRQB_SOFT	IRQA_SOFT	IRQ9_SOFT	IRQ8_SOFT	IRQ7_SOFT	IRQ6_SOFT	IRQ5_SOFT	IRQ4_SOFT	IRQ3_SOFT	IRQ2_SOFT	IRQ1_SOFT	IRQ0_SOFT
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	IRQ1F_SOFT	Software Interrupt
30	IRQ1E_SOFT	Software Interrupt
29	IRQ1D_SOFT	Software Interrupt
28	IRQ1C_SOFT	Software Interrupt
27	IRQ1B_SOFT	Software Interrupt
26	IRQ1A_SOFT	Software Interrupt
25	IRQ19_SOFT	Software Interrupt
24	IRQ18_SOFT	Software Interrupt
23	IRQ17_SOFT	Software Interrupt
22	IRQ16_SOFT	Software Interrupt
21	IRQ15_SOFT	Software Interrupt
20	IRQ14_SOFT	Software Interrupt
19	IRQ13_SOFT	Software Interrupt
18	IRQ12_SOFT	Software Interrupt
17	IRQ11_SOFT	Software Interrupt
16	IRQ10_SOFT	Software Interrupt
15	IRQF_SOFT	Software Interrupt
14	IRQE_SOFT	Software Interrupt
13	IRQD_SOFT	Software Interrupt
12	IRQC_SOFT	Software Interrupt
11	IRQB_SOFT	Software Interrupt
10	IRQA_SOFT	Software Interrupt
9	IRQ9_SOFT	Software Interrupt
8	IRQ8_SOFT	Software Interrupt
7	IRQ7_SOFT	Software Interrupt
6	IRQ6_SOFT	Software Interrupt
5	IRQ5_SOFT	Software Interrupt
4	IRQ4_SOFT	Software Interrupt
3	IRQ3_SOFT	Software Interrupt
2	IRQ2_SOFT	Software Interrupt
1	IRQ1_SOFT	Software Interrupt
0	IRQ0_SOFT	Software Interrupt

Bit(s)	Name	Description

151A00C4	<u>IRQ_SOFTM</u>			IRQ Software Interrupt Register Middle										00000000		
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	IRQ3F_SOFT	IRQ3E_SOFT	IRQ3D_SOFT	IRQ3C_SOFT	IRQ3B_SOFT	IRQ3A_SOFT	IRQ39_SOFT	IRQ38_SOFT	IRQ37_SOFT	IRQ36_SOFT	IRQ35_SOFT	IRQ34_SOFT	IRQ33_SOFT	IRQ32_SOFT	IRQ31_SOFT	IRQ30_SOFT
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IRQ2F_SOFT	IRQ2E_SOFT	IRQ2D_SOFT	IRQ2C_SOFT	IRQ2B_SOFT	IRQ2A_SOFT	IRQ29_SOFT	IRQ28_SOFT	IRQ27_SOFT	IRQ26_SOFT	IRQ25_SOFT	IRQ24_SOFT	IRQ23_SOFT	IRQ22_SOFT	IRQ21_SOFT	IRQ20_SOFT
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	IRQ3F_SOFT	Software Interrupt
30	IRQ3E_SOFT	Software Interrupt
29	IRQ3D_SOFT	Software Interrupt
28	IRQ3C_SOFT	Software Interrupt
27	IRQ3B_SOFT	Software Interrupt
26	IRQ3A_SOFT	Software Interrupt
25	IRQ39_SOFT	Software Interrupt
24	IRQ38_SOFT	Software Interrupt
23	IRQ37_SOFT	Software Interrupt
22	IRQ36_SOFT	Software Interrupt
21	IRQ35_SOFT	Software Interrupt
20	IRQ34_SOFT	Software Interrupt
19	IRQ33_SOFT	Software Interrupt
18	IRQ32_SOFT	Software Interrupt
17	IRQ31_SOFT	Software Interrupt
16	IRQ30_SOFT	Software Interrupt
15	IRQ2F_SOFT	Software Interrupt
14	IRQ2E_SOFT	Software Interrupt
13	IRQ2D_SOFT	Software Interrupt
12	IRQ2C_SOFT	Software Interrupt
11	IRQ2B_SOFT	Software Interrupt
10	IRQ2A_SOFT	Software Interrupt
9	IRQ29_SOFT	Software Interrupt
8	IRQ28_SOFT	Software Interrupt
7	IRQ27_SOFT	Software Interrupt
6	IRQ26_SOFT	Software Interrupt
5	IRQ25_SOFT	Software Interrupt
4	IRQ24_SOFT	Software Interrupt
3	IRQ23_SOFT	Software Interrupt
2	IRQ22_SOFT	Software Interrupt

Bit(s)	Name	Description
1	IRQ21_SOFT	Software Interrupt
0	IRQ20_SOFT	Software Interrupt

151A00D0 **FIQ_CON** **FIQ Control Register** 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															FIQ_SE NS	FIQ_M ASK
Type															RW	RW
Reset															0	1

Bit(s)	Name	Description
1	FIQ_SENS	Sensitivity type of the FIQ Interrupt Source 0: Edge sensitivity with active LOW 1: Level sensitivity with active LOW
0	FIQ_MASK	Mask control for the FIQ Interrupt Source 0: Interrupt is enabled 1: Interrupt is disabled

151A00D4 **FIQ_EOI** **FIQ End of Interrupt Register** 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																FIQ_EO I
Type																WO
Reset																0

Bit(s)	Name	Description
0	FIQ_EOI	End of Interrupt command 0: No interrupt request is generated 1: Interrupt request is in-service

151A00D8 IRQ_STA2 Binary Coded Value of IRQ_STATUS 00000100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								NOIRQ			IRQ_STA2					
Type								RS			RC					
Reset								1			0	0	0	0	0	0

Bit(s)	Name	Description
8	NOIRQ	Indicating if there is an IRQ or not. If there is no IRQ, this bit is HIGH
5:0	IRQ_STA2	Binary coded value of IRQ_STA

151A00DC IRQ_EOI2 Binary Coded Value of IRQ_EOI 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											IRQ_EOI2					
Type											WO					
Reset											0	0	0	0	0	0

Bit(s)	Name	Description
5:0	IRQ_EOI2	Binary coded value of IRQ_EOI

151A00E0 IRQ_ASTA Binary Value of IRQ Source Status 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	IRQ1F_ASTA	IRQ1E_ASTA	IRQ1D_ASTA	IRQ1C_ASTA	IRQ1B_ASTA	IRQ1A_ASTA	IRQ19_ASTA	IRQ18_ASTA	IRQ17_ASTA	IRQ16_ASTA	IRQ15_ASTA	IRQ14_ASTA	IRQ13_ASTA	IRQ12_ASTA	IRQ11_ASTA	IRQ10_ASTA
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IRQF_A_STA	IRQE_A_STA	IRQD_ASTA	IRQC_A_STA	IRQB_A_STA	IRQA_ASTA	IRQ9_A_STA	IRQ8_A_STA	IRQ7_A_STA	IRQ6_A_STA	IRQ5_A_STA	IRQ4_A_STA	IRQ3_A_STA	IRQ2_A_STA	IRQ1_A_STA	IRQ0_A_STA
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	IRQ1F_ASTA	Status of interrupt source 0: no interrupt. 1: interrupt occurs
30	IRQ1E_ASTA	Status of interrupt source 0: no interrupt. 1: interrupt occurs
29	IRQ1D_ASTA	Status of interrupt source 0: no interrupt. 1: interrupt occurs
28	IRQ1C_ASTA	Status of interrupt source 0: no interrupt. 1: interrupt occurs
27	IRQ1B_ASTA	Status of interrupt source 0: no interrupt. 1: interrupt occurs
26	IRQ1A_ASTA	Status of interrupt source 0: no interrupt. 1: interrupt occurs
25	IRQ19_ASTA	Status of interrupt source 0: no interrupt. 1: interrupt occurs
24	IRQ18_ASTA	Status of interrupt source 0: no interrupt. 1: interrupt occurs
23	IRQ17_ASTA	Status of interrupt source 0: no interrupt. 1: interrupt occurs
22	IRQ16_ASTA	Status of interrupt source 0: no interrupt. 1: interrupt occurs
21	IRQ15_ASTA	Status of interrupt source 0: no interrupt. 1: interrupt occurs

Bit(s)	Name	Description
20	IRQ14_ASTA	Status of interrupt source 0: no interrupt. 1: interrupt occurs
19	IRQ13_ASTA	Status of interrupt source 0: no interrupt. 1: interrupt occurs
18	IRQ12_ASTA	Status of interrupt source 0: no interrupt. 1: interrupt occurs
17	IRQ11_ASTA	Status of interrupt source 0: no interrupt. 1: interrupt occurs
16	IRQ10_ASTA	Status of interrupt source 0: no interrupt. 1: interrupt occurs
15	IRQF_ASTA	Status of interrupt source 0: no interrupt. 1: interrupt occurs
14	IRQE_ASTA	Status of interrupt source 0: no interrupt. 1: interrupt occurs
13	IRQD_ASTA	Status of interrupt source 0: no interrupt. 1: interrupt occurs
12	IRQC_ASTA	Status of interrupt source 0: no interrupt. 1: interrupt occurs
11	IRQB_ASTA	Status of interrupt source 0: no interrupt. 1: interrupt occurs
10	IRQA_ASTA	Status of interrupt source 0: no interrupt. 1: interrupt occurs
9	IRQ9_ASTA	Status of interrupt source 0: no interrupt. 1: interrupt occurs
8	IRQ8_ASTA	Status of interrupt source 0: no interrupt. 1: interrupt occurs
7	IRQ7_ASTA	Status of interrupt source 0: no interrupt. 1: interrupt occurs
6	IRQ6_ASTA	Status of interrupt source 0: no interrupt. 1: interrupt occurs
5	IRQ5_ASTA	Status of interrupt source 0: no interrupt. 1: interrupt occurs
4	IRQ4_ASTA	Status of interrupt source 0: no interrupt. 1: interrupt occurs
3	IRQ3_ASTA	Status of interrupt source 0: no interrupt.

Bit(s)	Name	Description
2	IRQ2_ASTA	1: interrupt occurs Status of interrupt source 0: no interrupt.
1	IRQ1_ASTA	1: interrupt occurs Status of interrupt source 0: no interrupt.
0	IRQ0_ASTA	1: interrupt occurs Status of interrupt source 0: no interrupt.

151A00E4 IRQ_ASTAM Binary Value of IRQ Source Status Middle 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	IRQ3F_ASTA	IRQ3E_ASTA	IRQ3D_ASTA	IRQ3C_ASTA	IRQ3B_ASTA	IRQ3A_ASTA	IRQ39_ASTA	IRQ38_ASTA	IRQ37_ASTA	IRQ36_ASTA	IRQ35_ASTA	IRQ34_ASTA	IRQ33_ASTA	IRQ32_ASTA	IRQ31_ASTA	IRQ30_ASTA
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IRQ2F_ASTA	IRQ2E_ASTA	IRQ2D_ASTA	IRQ2C_ASTA	IRQ2B_ASTA	IRQ2A_ASTA	IRQ29_ASTA	IRQ28_ASTA	IRQ27_ASTA	IRQ26_ASTA	IRQ25_ASTA	IRQ24_ASTA	IRQ23_ASTA	IRQ22_ASTA	IRQ21_ASTA	IRQ20_ASTA
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	IRQ3F_ASTA	Status of interrupt source 0: no interrupt. 1: interrupt occurs
30	IRQ3E_ASTA	Status of interrupt source 0: no interrupt. 1: interrupt occurs
29	IRQ3D_ASTA	Status of interrupt source 0: no interrupt. 1: interrupt occurs
28	IRQ3C_ASTA	Status of interrupt source 0: no interrupt. 1: interrupt occurs
27	IRQ3B_ASTA	Status of interrupt source 0: no interrupt. 1: interrupt occurs
26	IRQ3A_ASTA	Status of interrupt source 0: no interrupt. 1: interrupt occurs
25	IRQ39_ASTA	Status of interrupt source 0: no interrupt.

Bit(s)	Name	Description
24	IRQ38_ASTA	1: interrupt occurs Status of interrupt source 0: no interrupt.
23	IRQ37_ASTA	1: interrupt occurs Status of interrupt source 0: no interrupt.
22	IRQ36_ASTA	1: interrupt occurs Status of interrupt source 0: no interrupt.
21	IRQ35_ASTA	1: interrupt occurs Status of interrupt source 0: no interrupt.
20	IRQ34_ASTA	1: interrupt occurs Status of interrupt source 0: no interrupt.
19	IRQ33_ASTA	1: interrupt occurs Status of interrupt source 0: no interrupt.
18	IRQ32_ASTA	1: interrupt occurs Status of interrupt source 0: no interrupt.
17	IRQ31_ASTA	1: interrupt occurs Status of interrupt source 0: no interrupt.
16	IRQ30_ASTA	1: interrupt occurs Status of interrupt source 0: no interrupt.
15	IRQ2F_ASTA	1: interrupt occurs Status of interrupt source 0: no interrupt.
14	IRQ2E_ASTA	1: interrupt occurs Status of interrupt source 0: no interrupt.
13	IRQ2D_ASTA	1: interrupt occurs Status of interrupt source 0: no interrupt.
12	IRQ2C_ASTA	1: interrupt occurs Status of interrupt source 0: no interrupt.
11	IRQ2B_ASTA	1: interrupt occurs Status of interrupt source 0: no interrupt.
10	IRQ2A_ASTA	1: interrupt occurs Status of interrupt source 0: no interrupt.
9	IRQ29_ASTA	1: interrupt occurs Status of interrupt source 0: no interrupt.
8	IRQ28_ASTA	1: interrupt occurs Status of interrupt source 0: no interrupt.
7	IRQ27_ASTA	1: interrupt occurs Status of interrupt source

Bit(s)	Name	Description
6	IRQ26_ASTA	0: no interrupt. 1: interrupt occurs Status of interrupt source
5	IRQ25_ASTA	0: no interrupt. 1: interrupt occurs Status of interrupt source
4	IRQ24_ASTA	0: no interrupt. 1: interrupt occurs Status of interrupt source
3	IRQ23_ASTA	0: no interrupt. 1: interrupt occurs Status of interrupt source
2	IRQ22_ASTA	0: no interrupt. 1: interrupt occurs Status of interrupt source
1	IRQ21_ASTA	0: no interrupt. 1: interrupt occurs Status of interrupt source
0	IRQ20_ASTA	0: no interrupt. 1: interrupt occurs Status of interrupt source

151A00F0		<u>IRQ_EEVT</u>		Binary Value of EINT Event												00000000	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
Name																	
Type																	
Reset																	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Name																	EINT_E VENT
Type																	RO
Reset																	0

Bit(s)	Name	Description
0	EINT_EVENT	EINT event status 0: no EINT event. 1: EINT event occurs.

151A0100	<u>EINT_STA</u>	EINT Status Register	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													EINT13_STA	EINT12_STA	EINT11_STA	EINT10_STA
Type													RO	RO	RO	RO
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINTF_STA	EINTE_STA	EINTD_STA	EINTC_STA	EINTB_STA	EINTA_STA	EINT9_STA	EINT8_STA	EINT7_STA	EINT6_STA	EINT5_STA	EINT4_STA	EINT3_STA	EINT2_STA	EINT1_STA	EINT0_STA
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
19	EINT13_STA	Interrupt Status 0: No interrupt request is generated 1: Interrupt request is pending
18	EINT12_STA	Interrupt Status 0: No interrupt request is generated 1: Interrupt request is pending
17	EINT11_STA	Interrupt Status 0: No interrupt request is generated 1: Interrupt request is pending
16	EINT10_STA	Interrupt Status 0: No interrupt request is generated 1: Interrupt request is pending
15	EINTF_STA	Interrupt Status 0: No interrupt request is generated 1: Interrupt request is pending
14	EINTE_STA	Interrupt Status 0: No interrupt request is generated 1: Interrupt request is pending
13	EINTD_STA	Interrupt Status 0: No interrupt request is generated 1: Interrupt request is pending
12	EINTC_STA	Interrupt Status 0: No interrupt request is generated 1: Interrupt request is pending
11	EINTB_STA	Interrupt Status 0: No interrupt request is generated 1: Interrupt request is pending
10	EINTA_STA	Interrupt Status 0: No interrupt request is generated 1: Interrupt request is pending
9	EINT9_STA	Interrupt Status 0: No interrupt request is generated 1: Interrupt request is pending
8	EINT8_STA	Interrupt Status 0: No interrupt request is generated 1: Interrupt request is pending

Bit(s)	Name	Description
7	EINT7_STA	1: Interrupt request is pending Interrupt Status 0: No interrupt request is generated
6	EINT6_STA	1: Interrupt request is pending Interrupt Status 0: No interrupt request is generated
5	EINT5_STA	1: Interrupt request is pending Interrupt Status 0: No interrupt request is generated
4	EINT4_STA	1: Interrupt request is pending Interrupt Status 0: No interrupt request is generated
3	EINT3_STA	1: Interrupt request is pending Interrupt Status 0: No interrupt request is generated
2	EINT2_STA	1: Interrupt request is pending Interrupt Status 0: No interrupt request is generated
1	EINT1_STA	1: Interrupt request is pending Interrupt Status 0: No interrupt request is generated
0	EINT0_STA	1: Interrupt request is pending Interrupt Status 0: No interrupt request is generated

151A0104		EINT_MASK				EINT Mask Register								000FFFFF			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
Name													EINT13_MASK	EINT12_MASK	EINT11_MASK	EINT10_MASK	
Type													RW	RW	RW	RW	
Reset													1	1	1	1	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Name	EINTF_MASK	EINTE_MASK	EINTD_MASK	EINTC_MASK	EINTB_MASK	EINTA_MASK	EINT9_MASK	EINT8_MASK	EINT7_MASK	EINT6_MASK	EINT5_MASK	EINT4_MASK	EINT3_MASK	EINT2_MASK	EINT1_MASK	EINT0_MASK	
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	

Bit(s)	Name	Description
19	EINT13_MASK	Mask control for the associated interrupt source in the IRQ controller 0: Interrupt is enabled 1: Interrupt is disabled
18	EINT12_MASK	Mask control for the associated interrupt source in the IRQ controller

Bit(s)	Name	Description
17	EINT11_MASK	0: Interrupt is enabled 1: Interrupt is disabled Mask control for the associated interrupt source in the IRQ controller
16	EINT10_MASK	0: Interrupt is enabled 1: Interrupt is disabled Mask control for the associated interrupt source in the IRQ controller
15	EINTF_MASK	0: Interrupt is enabled 1: Interrupt is disabled Mask control for the associated interrupt source in the IRQ controller
14	EINTE_MASK	0: Interrupt is enabled 1: Interrupt is disabled Mask control for the associated interrupt source in the IRQ controller
13	EINTD_MASK	0: Interrupt is enabled 1: Interrupt is disabled Mask control for the associated interrupt source in the IRQ controller
12	EINTC_MASK	0: Interrupt is enabled 1: Interrupt is disabled Mask control for the associated interrupt source in the IRQ controller
11	EINTB_MASK	0: Interrupt is enabled 1: Interrupt is disabled Mask control for the associated interrupt source in the IRQ controller
10	EINTA_MASK	0: Interrupt is enabled 1: Interrupt is disabled Mask control for the associated interrupt source in the IRQ controller
9	EINT9_MASK	0: Interrupt is enabled 1: Interrupt is disabled Mask control for the associated interrupt source in the IRQ controller
8	EINT8_MASK	0: Interrupt is enabled 1: Interrupt is disabled Mask control for the associated interrupt source in the IRQ controller
7	EINT7_MASK	0: Interrupt is enabled 1: Interrupt is disabled Mask control for the associated interrupt source in the IRQ controller
6	EINT6_MASK	0: Interrupt is enabled 1: Interrupt is disabled Mask control for the associated interrupt source in the IRQ controller
5	EINT5_MASK	0: Interrupt is enabled 1: Interrupt is disabled Mask control for the associated interrupt source in the IRQ controller
4	EINT4_MASK	0: Interrupt is enabled 1: Interrupt is disabled Mask control for the associated interrupt source in the IRQ controller
3	EINT3_MASK	0: Interrupt is enabled 1: Interrupt is disabled Mask control for the associated interrupt source in the IRQ controller
2	EINT2_MASK	0: Interrupt is enabled 1: Interrupt is disabled Mask control for the associated interrupt source in the IRQ controller
1	EINT1_MASK	0: Interrupt is enabled 1: Interrupt is disabled Mask control for the associated interrupt source in the IRQ controller

Bit(s)	Name	Description
0	EINT0_MASK	Mask control for the associated interrupt source in the IRQ controller 0: Interrupt is enabled 1: Interrupt is disabled

151A0108 EINT_MASK_CLR EINT Mask Clear Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													EINT13_MCLR	EINT12_MCLR	EINT11_MCLR	EINT10_MCLR
Type													WO	WO	WO	WO
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINTF_MCLR	EINTE_MCLR	EINTD_MCLR	EINTC_MCLR	EINTB_MCLR	EINTA_MCLR	EINT9_MCLR	EINT8_MCLR	EINT7_MCLR	EINT6_MCLR	EINT5_MCLR	EINT4_MCLR	EINT3_MCLR	EINT2_MCLR	EINT1_MCLR	EINT0_MCLR
Type	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
19	EINT13_MCLR	Disable mask for the associated external interrupt source 0: No effect. 1: Disable the corresponding MASK bit.
18	EINT12_MCLR	Disable mask for the associated external interrupt source 0: No effect. 1: Disable the corresponding MASK bit.
17	EINT11_MCLR	Disable mask for the associated external interrupt source 0: No effect. 1: Disable the corresponding MASK bit.
16	EINT10_MCLR	Disable mask for the associated external interrupt source 0: No effect. 1: Disable the corresponding MASK bit.
15	EINTF_MCLR	Disable mask for the associated external interrupt source 0: No effect. 1: Disable the corresponding MASK bit.
14	EINTE_MCLR	Disable mask for the associated external interrupt source 0: No effect. 1: Disable the corresponding MASK bit.
13	EINTD_MCLR	Disable mask for the associated external interrupt source 0: No effect. 1: Disable the corresponding MASK bit.
12	EINTC_MCLR	Disable mask for the associated external interrupt source 0: No effect. 1: Disable the corresponding MASK bit.
11	EINTB_MCLR	Disable mask for the associated external interrupt source 0: No effect.

Bit(s)	Name	Description
10	EINTA_MCLR	1: Disable the corresponding MASK bit. Disable mask for the associated external interrupt source 0: No effect.
9	EINT9_MCLR	1: Disable the corresponding MASK bit. Disable mask for the associated external interrupt source 0: No effect.
8	EINT8_MCLR	1: Disable the corresponding MASK bit. Disable mask for the associated external interrupt source 0: No effect.
7	EINT7_MCLR	1: Disable the corresponding MASK bit. Disable mask for the associated external interrupt source 0: No effect.
6	EINT6_MCLR	1: Disable the corresponding MASK bit. Disable mask for the associated external interrupt source 0: No effect.
5	EINT5_MCLR	1: Disable the corresponding MASK bit. Disable mask for the associated external interrupt source 0: No effect.
4	EINT4_MCLR	1: Disable the corresponding MASK bit. Disable mask for the associated external interrupt source 0: No effect.
3	EINT3_MCLR	1: Disable the corresponding MASK bit. Disable mask for the associated external interrupt source 0: No effect.
2	EINT2_MCLR	1: Disable the corresponding MASK bit. Disable mask for the associated external interrupt source 0: No effect.
1	EINT1_MCLR	1: Disable the corresponding MASK bit. Disable mask for the associated external interrupt source 0: No effect.
0	EINT0_MCLR	1: Disable the corresponding MASK bit. Disable mask for the associated external interrupt source 0: No effect.

151A010C	EINT_MASK_SET				EINT Mask Set Register								00000000			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													EINT13_MSET	EINT12_MSET	EINT11_MSET	EINT10_MSET
Type													WO	WO	WO	WO
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINTF_MSET	EINTE_MSET	EINTD_MSET	EINTC_MSET	EINTB_MSET	EINTA_MSET	EINT9_MSET	EINT8_MSET	EINT7_MSET	EINT6_MSET	EINT5_MSET	EINT4_MSET	EINT3_MSET	EINT2_MSET	EINT1_MSET	EINT0_MSET
Type	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
19	EINT13_MSET	Enable mask for the associated external interrupt source. 0: No effect. 1: Enable corresponding MASK bit.
18	EINT12_MSET	Enable mask for the associated external interrupt source. 0: No effect. 1: Enable corresponding MASK bit.
17	EINT11_MSET	Enable mask for the associated external interrupt source. 0: No effect. 1: Enable corresponding MASK bit.
16	EINT10_MSET	Enable mask for the associated external interrupt source. 0: No effect. 1: Enable corresponding MASK bit.
15	EINTF_MSET	Enable mask for the associated external interrupt source. 0: No effect. 1: Enable corresponding MASK bit.
14	EINTE_MSET	Enable mask for the associated external interrupt source. 0: No effect. 1: Enable corresponding MASK bit.
13	EINTD_MSET	Enable mask for the associated external interrupt source. 0: No effect. 1: Enable corresponding MASK bit.
12	EINTC_MSET	Enable mask for the associated external interrupt source. 0: No effect. 1: Enable corresponding MASK bit.
11	EINTB_MSET	Enable mask for the associated external interrupt source. 0: No effect. 1: Enable corresponding MASK bit.
10	EINTA_MSET	Enable mask for the associated external interrupt source. 0: No effect. 1: Enable corresponding MASK bit.
9	EINT9_MSET	Enable mask for the associated external interrupt source. 0: No effect. 1: Enable corresponding MASK bit.
8	EINT8_MSET	Enable mask for the associated external interrupt source. 0: No effect. 1: Enable corresponding MASK bit.
7	EINT7_MSET	Enable mask for the associated external interrupt source. 0: No effect. 1: Enable corresponding MASK bit.
6	EINT6_MSET	Enable mask for the associated external interrupt source. 0: No effect. 1: Enable corresponding MASK bit.
5	EINT5_MSET	Enable mask for the associated external interrupt source. 0: No effect. 1: Enable corresponding MASK bit.
4	EINT4_MSET	Enable mask for the associated external interrupt source. 0: No effect. 1: Enable corresponding MASK bit.
3	EINT3_MSET	Enable mask for the associated external interrupt source. 0: No effect.

Bit(s)	Name	Description
2	EINT2_MSET	1: Enable corresponding MASK bit. Enable mask for the associated external interrupt source. 0: No effect.
1	EINT1_MSET	1: Enable corresponding MASK bit. Enable mask for the associated external interrupt source. 0: No effect.
0	EINT0_MSET	1: Enable corresponding MASK bit. Enable mask for the associated external interrupt source. 0: No effect.

151A0110 EINT_INTACK EINT Interrupt Acknowledge Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													EINT13_ACK	EINT12_ACK	EINT11_ACK	EINT10_ACK
Type													WO	WO	WO	WO
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINTF_ACK	EINTE_ACK	EINTD_ACK	EINTC_ACK	EINTB_ACK	EINTA_ACK	EINT9_ACK	EINT8_ACK	EINT7_ACK	EINT6_ACK	EINT5_ACK	EINT4_ACK	EINT3_ACK	EINT2_ACK	EINT1_ACK	EINT0_ACK
Type	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
19	EINT13_ACK	Interrupt acknowledgement 0: No effect. 1: Interrupt Request is acknowledged.
18	EINT12_ACK	Interrupt acknowledgement 0: No effect. 1: Interrupt Request is acknowledged.
17	EINT11_ACK	Interrupt acknowledgement 0: No effect. 1: Interrupt Request is acknowledged.
16	EINT10_ACK	Interrupt acknowledgement 0: No effect. 1: Interrupt Request is acknowledged.
15	EINTF_ACK	Interrupt acknowledgement 0: No effect. 1: Interrupt Request is acknowledged.
14	EINTE_ACK	Interrupt acknowledgement 0: No effect. 1: Interrupt Request is acknowledged.
13	EINTD_ACK	Interrupt acknowledgement

Bit(s)	Name	Description
12	EINTC_ACK	0: No effect. 1: Interrupt Request is acknowledged. Interrupt acknowledgement 0: No effect.
11	EINTB_ACK	1: Interrupt Request is acknowledged. Interrupt acknowledgement 0: No effect.
10	EINTA_ACK	1: Interrupt Request is acknowledged. Interrupt acknowledgement 0: No effect.
9	EINT9_ACK	1: Interrupt Request is acknowledged. Interrupt acknowledgement 0: No effect.
8	EINT8_ACK	1: Interrupt Request is acknowledged. Interrupt acknowledgement 0: No effect.
7	EINT7_ACK	1: Interrupt Request is acknowledged. Interrupt acknowledgement 0: No effect.
6	EINT6_ACK	1: Interrupt Request is acknowledged. Interrupt acknowledgement 0: No effect.
5	EINT5_ACK	1: Interrupt Request is acknowledged. Interrupt acknowledgement 0: No effect.
4	EINT4_ACK	1: Interrupt Request is acknowledged. Interrupt acknowledgement 0: No effect.
3	EINT3_ACK	1: Interrupt Request is acknowledged. Interrupt acknowledgement 0: No effect.
2	EINT2_ACK	1: Interrupt Request is acknowledged. Interrupt acknowledgement 0: No effect.
1	EINT1_ACK	1: Interrupt Request is acknowledged. Interrupt acknowledgement 0: No effect.
0	EINT0_ACK	1: Interrupt Request is acknowledged. Interrupt acknowledgement 0: No effect.

151A0114	EINT_SENS				EINT Sensitive Register								000FFFFF			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													EINT13_SENS	EINT12_SENS	EINT11_SENS	EINT10_SENS
Type													RW	RW	RW	RW

Reset													1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINTF_SENS	EINTE_SENS	EINTD_SENS	EINTC_SENS	EINTB_SENS	EINTA_SENS	EINT9_SENS	EINT8_SENS	EINT7_SENS	EINT6_SENS	EINT5_SENS	EINT4_SENS	EINT3_SENS	EINT2_SENS	EINT1_SENS	EINT0_SENS
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
19	EINT13_SENS	Sensitive type of the associated external interrupt source 0: Edge sensitivity. 1: Level sensitivity.
18	EINT12_SENS	Sensitive type of the associated external interrupt source 0: Edge sensitivity. 1: Level sensitivity.
17	EINT11_SENS	Sensitive type of the associated external interrupt source 0: Edge sensitivity. 1: Level sensitivity.
16	EINT10_SENS	Sensitive type of the associated external interrupt source 0: Edge sensitivity. 1: Level sensitivity.
15	EINTF_SENS	Sensitive type of the associated external interrupt source 0: Edge sensitivity. 1: Level sensitivity.
14	EINTE_SENS	Sensitive type of the associated external interrupt source 0: Edge sensitivity. 1: Level sensitivity.
13	EINTD_SENS	Sensitive type of the associated external interrupt source 0: Edge sensitivity. 1: Level sensitivity.
12	EINTC_SENS	Sensitive type of the associated external interrupt source 0: Edge sensitivity. 1: Level sensitivity.
11	EINTB_SENS	Sensitive type of the associated external interrupt source 0: Edge sensitivity. 1: Level sensitivity.
10	EINTA_SENS	Sensitive type of the associated external interrupt source 0: Edge sensitivity. 1: Level sensitivity.
9	EINT9_SENS	Sensitive type of the associated external interrupt source 0: Edge sensitivity. 1: Level sensitivity.
8	EINT8_SENS	Sensitive type of the associated external interrupt source 0: Edge sensitivity. 1: Level sensitivity.
7	EINT7_SENS	Sensitive type of the associated external interrupt source 0: Edge sensitivity. 1: Level sensitivity.
6	EINT6_SENS	Sensitive type of the associated external interrupt source 0: Edge sensitivity.

Bit(s)	Name	Description
5	EINT5_SENS	1: Level sensitivity. Sensitive type of the associated external interrupt source 0: Edge sensitivity.
4	EINT4_SENS	1: Level sensitivity. Sensitive type of the associated external interrupt source 0: Edge sensitivity.
3	EINT3_SENS	1: Level sensitivity. Sensitive type of the associated external interrupt source 0: Edge sensitivity.
2	EINT2_SENS	1: Level sensitivity. Sensitive type of the associated external interrupt source 0: Edge sensitivity.
1	EINT1_SENS	1: Level sensitivity. Sensitive type of the associated external interrupt source 0: Edge sensitivity.
0	EINT0_SENS	1: Level sensitivity. Sensitive type of the associated external interrupt source 0: Edge sensitivity.

151A0118 **EINT_SOFT** EINT Software Interrupt Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													EINT13_SOFT	EINT12_SOFT	EINT11_SOFT	EINT10_SOFT
Type													RW	RW	RW	RW
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINTF_SOFT	EINTE_SOFT	EINTD_SOFT	EINTC_SOFT	EINTB_SOFT	EINTA_SOFT	EINT9_SOFT	EINT8_SOFT	EINT7_SOFT	EINT6_SOFT	EINT5_SOFT	EINT4_SOFT	EINT3_SOFT	EINT2_SOFT	EINT1_SOFT	EINT0_SOFT
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
19	EINT13_SOFT	Software Interrupt
18	EINT12_SOFT	Software Interrupt
17	EINT11_SOFT	Software Interrupt
16	EINT10_SOFT	Software Interrupt
15	EINTF_SOFT	Software Interrupt
14	EINTE_SOFT	Software Interrupt
13	EINTD_SOFT	Software Interrupt
12	EINTC_SOFT	Software Interrupt
11	EINTB_SOFT	Software Interrupt
10	EINTA_SOFT	Software Interrupt

Bit(s)	Name	Description
9	EINT9_SOFT	Software Interrupt
8	EINT8_SOFT	Software Interrupt
7	EINT7_SOFT	Software Interrupt
6	EINT6_SOFT	Software Interrupt
5	EINT5_SOFT	Software Interrupt
4	EINT4_SOFT	Software Interrupt
3	EINT3_SOFT	Software Interrupt
2	EINT2_SOFT	Software Interrupt
1	EINT1_SOFT	Software Interrupt
0	EINT0_SOFT	Software Interrupt

151A0120 EINT0_CON EINT 0 De-bounce Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT0_EN	EINT0_PRESCALER				EINT0_POL	EINT0_CNT									
Type	RW	RW				RW	RW									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	EINT0_EN	De-bounce control circuit 0: Disable 1: Enable
14:12	EINT0_PRESCALER	Determine the clock cycle period for debounce count. 3'b000: 32768Hz, max 3'b001: 16384Hz 3'b010: 8192Hz 3'b011: 4096Hz 3'b100: 2048Hz, max 3'b101: 1024Hz 3'b110: 512Hz 3'b111: 256Hz, max
11	EINT0_POL	Activation type of the EINT source 0: Negative polarity 1: Positive polarity
10:0	EINT0_CNT	De-bounce duration in terms of numbers of 32768Hz clock cycles. The cycle length is determined by PRESCALER

151A0130 EINT1_CON EINT 1 De-bounce Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT1_EN	EINT1_PRESCALER				EINT1_POL	EINT1_CNT									
Type	RW	RW				RW	RW									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	EINT1_EN	De-bounce control circuit 0: Disable 1: Enable
14:12	EINT1_PRESCALER	Determine the clock cycle period for debounce count. 3'b000: 32768Hz, max 3'b001: 16384Hz 3'b010: 8192Hz 3'b011: 4096Hz 3'b100: 2048Hz, max 3'b101: 1024Hz 3'b110: 512Hz 3'b111: 256Hz, max
11	EINT1_POL	Activation type of the EINT source 0: Negative polarity 1: Positive polarity
10:0	EINT1_CNT	De-bounce duration in terms of numbers of 32768Hz clock cycles. The cycle length is determined by PRESCALER

151A0140 EINT2_CON EINT 2 De-bounce Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT2_EN	EINT2_PRESCALER				EINT2_POL	EINT2_CNT									

Type	RW	RW			RW	RW										
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	EINT2_EN	De-bounce control circuit 0: Disable 1: Enable
14:12	EINT2_PRESCALER	Determine the clock cycle period for debounce count. 3'b000: 32768Hz, max 3'b001: 16384Hz 3'b010: 8192Hz 3'b011: 4096Hz 3'b100: 2048Hz, max 3'b101: 1024Hz 3'b110: 512Hz 3'b111: 256Hz, max
11	EINT2_POL	Activation type of the EINT source 0: Negative polarity 1: Positive polarity
10:0	EINT2_CNT	De-bounce duration in terms of numbers of 32768Hz clock cycles. The cycle length is determined by PRESCALER

151A0150		EINT3_CON				EINT 3 De-bounce Control Register											00000000	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16		
Name																		
Type																		
Reset																		
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
Name	EINT3_EN	EINT3_PRESCALER				EINT3_POL	EINT3_CNT											
Type	RW	RW				RW	RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

Bit(s)	Name	Description
15	EINT3_EN	De-bounce control circuit 0: Disable 1: Enable
14:12	EINT3_PRESCALER	Determine the clock cycle period for debounce count. 3'b000: 32768Hz, max 3'b001: 16384Hz 3'b010: 8192Hz 3'b011: 4096Hz

Bit(s)	Name	Description
11	EINT3_POL	3'b100: 2048Hz, max 3'b101: 1024Hz 3'b110: 512Hz 3'b111: 256Hz, max Activation type of the EINT source 0: Negative polarity 1: Positive polarity
10:0	EINT3_CNT	De-bounce duration in terms of numbers of 32768Hz clock cycles. The cycle length is determined by PRESCALER

151A0160 EINT4_CON EINT 4 De-bounce Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT4_EN	EINT4_PRESCALER				EINT4_POL	EINT4_CNT									
Type	RW	RW				RW	RW									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	EINT4_EN	De-bounce control circuit 0: Disable 1: Enable
14:12	EINT4_PRESCALER	Determine the clock cycle period for debounce count. 3'b000: 32768Hz, max 3'b001: 16384Hz 3'b010: 8192Hz 3'b011: 4096Hz 3'b100: 2048Hz, max 3'b101: 1024Hz 3'b110: 512Hz 3'b111: 256Hz, max
11	EINT4_POL	Activation type of the EINT source 0: Negative polarity 1: Positive polarity
10:0	EINT4_CNT	De-bounce duration in terms of numbers of 32768Hz clock cycles. The cycle length is determined by PRESCALER

151A0170 EINT5_CON EINT 5 De-bounce Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT5_EN	EINT5_PRESCALER				EINT5_POL	EINT5_CNT									
Type	RW	RW				RW	RW									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	EINT5_EN	De-bounce control circuit 0: Disable 1: Enable
14:12	EINT5_PRESCALER	Determine the clock cycle period for debounce count. 3'b000: 32768Hz, max 3'b001: 16384Hz 3'b010: 8192Hz 3'b011: 4096Hz 3'b100: 2048Hz, max 3'b101: 1024Hz 3'b110: 512Hz 3'b111: 256Hz, max
11	EINT5_POL	Activation type of the EINT source 0: Negative polarity 1: Positive polarity
10:0	EINT5_CNT	De-bounce duration in terms of numbers of 32768Hz clock cycles. The cycle length is determined by PRESCALER

151A0180 EINT6_CON EINT 6 De-bounce Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT6_EN	EINT6_PRESCALER				EINT6_POL	EINT6_CNT									
Type	RW	RW				RW	RW									

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	EINT6_EN	De-bounce control circuit 0: Disable 1: Enable
14:12	EINT6_PRESCALER	Determine the clock cycle period for debounce count. 3'b000: 32768Hz, max 3'b001: 16384Hz 3'b010: 8192Hz 3'b011: 4096Hz 3'b100: 2048Hz, max 3'b101: 1024Hz 3'b110: 512Hz 3'b111: 256Hz, max
11	EINT6_POL	Activation type of the EINT source 0: Negative polarity 1: Positive polarity
10:0	EINT6_CNT	De-bounce duration in terms of numbers of 32768Hz clock cycles. The cycle length is determined by PRESCALER

151A0190		EINT7_CON				EINT 7 De-bounce Control Register											00000000	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16		
Name																		
Type																		
Reset																		
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
Name	EINT7_EN	EINT7_PRESCALER			EINT7_POL	EINT7_CNT												
Type	RW	RW			RW	RW												
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

Bit(s)	Name	Description
15	EINT7_EN	De-bounce control circuit 0: Disable 1: Enable
14:12	EINT7_PRESCALER	Determine the clock cycle period for debounce count. 3'b000: 32768Hz, max 3'b001: 16384Hz 3'b010: 8192Hz 3'b011: 4096Hz 3'b100: 2048Hz, max 3'b101: 1024Hz

Bit(s)	Name	Description
11	EINT7_POL	3'b110: 512Hz 3'b111: 256Hz, max Activation type of the EINT source 0: Negative polarity 1: Positive polarity
10:0	EINT7_CNT	De-bounce duration in terms of numbers of 32768Hz clock cycles. The cycle length is determined by PRESCALER

151A01A0		EINT8_CON										EINT 8 De-bounce Control Register					00000000	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16		
Name																		
Type																		
Reset																		
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
Name	EINT8_EN	EINT8_PRESCALER				EINT8_POL	EINT8_CNT											
Type	RW	RW				RW	RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

Bit(s)	Name	Description
15	EINT8_EN	De-bounce control circuit 0: Disable 1: Enable
14:12	EINT8_PRESCALER	Determine the clock cycle period for debounce count. 3'b000: 32768Hz, max 3'b001: 16384Hz 3'b010: 8192Hz 3'b011: 4096Hz 3'b100: 2048Hz, max 3'b101: 1024Hz 3'b110: 512Hz 3'b111: 256Hz, max
11	EINT8_POL	Activation type of the EINT source 0: Negative polarity 1: Positive polarity
10:0	EINT8_CNT	De-bounce duration in terms of numbers of 32768Hz clock cycles. The cycle length is determined by PRESCALER

151A01B0		EINT9_CON										EINT 9 De-bounce Control Register					00000000	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16		

Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT9_EN	EINT9_PRESCALER				EINT9_POL	EINT9_CNT									
Type	RW	RW				RW	RW									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	EINT9_EN	De-bounce control circuit 0: Disable 1: Enable
14:12	EINT9_PRESCALER	Determine the clock cycle period for debounce count. 3'b000: 32768Hz, max 3'b001: 16384Hz 3'b010: 8192Hz 3'b011: 4096Hz 3'b100: 2048Hz, max 3'b101: 1024Hz 3'b110: 512Hz 3'b111: 256Hz, max
11	EINT9_POL	Activation type of the EINT source 0: Negative polarity 1: Positive polarity
10:0	EINT9_CNT	De-bounce duration in terms of numbers of 32768Hz clock cycles. The cycle length is determined by PRESCALER

151A01C0		EINTA_CON				EINTA De-bounce Control Register											00000000	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16		
Name																		
Type																		
Reset																		
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
Name	EINTA_EN	EINTA_PRESCALER			EINTA_POL	EINTA_CNT												
Type	RW	RW			RW	RW												
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

Bit(s)	Name	Description
15	EINTA_EN	De-bounce control circuit 0: Disable 1: Enable
14:12	EINTA_PRESCALER	Determine the clock cycle period for debounce count. 3'b000: 32768Hz, max 3'b001: 16384Hz 3'b010: 8192Hz 3'b011: 4096Hz 3'b100: 2048Hz, max 3'b101: 1024Hz 3'b110: 512Hz 3'b111: 256Hz, max
11	EINTA_POL	Activation type of the EINT source 0: Negative polarity 1: Positive polarity
10:0	EINTA_CNT	De-bounce duration in terms of numbers of 32768Hz clock cycles. The cycle length is determined by PRESCALER

151A01D0		EINTB_CON				EINT B De-bounce Control Register											00000000	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16		
Name																		
Type																		
Reset																		
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
Name	EINTB_EN	EINTB_PRESCALER				EINTB_POL	EINTB_CNT											
Type	RW	RW				RW	RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

Bit(s)	Name	Description
15	EINTB_EN	De-bounce control circuit 0: Disable 1: Enable
14:12	EINTB_PRESCALER	Determine the clock cycle period for debounce count. 3'b000: 32768Hz, max 3'b001: 16384Hz 3'b010: 8192Hz 3'b011: 4096Hz 3'b100: 2048Hz, max 3'b101: 1024Hz 3'b110: 512Hz 3'b111: 256Hz, max

Bit(s)	Name	Description
11	EINTB_POL	Activation type of the EINT source 0: Negative polarity 1: Positive polarity
10:0	EINTB_CNT	De-bounce duration in terms of numbers of 32768Hz clock cycles. The cycle length is determined by PRESCALER

151A01E0 EINTC_CON EINT C De-bounce Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINTC_EN	EINTC_PRESCALER				EINTC_POL	EINTC_CNT									
Type	RW	RW				RW	RW									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	EINTC_EN	De-bounce control circuit 0: Disable 1: Enable
14:12	EINTC_PRESCALER	Determine the clock cycle period for debounce count. 3'b000: 32768Hz, max 3'b001: 16384Hz 3'b010: 8192Hz 3'b011: 4096Hz 3'b100: 2048Hz, max 3'b101: 1024Hz 3'b110: 512Hz 3'b111: 256Hz, max
11	EINTC_POL	Activation type of the EINT source 0: Negative polarity 1: Positive polarity
10:0	EINTC_CNT	De-bounce duration in terms of numbers of 32768Hz clock cycles. The cycle length is determined by PRESCALER

151A01F0 EINTD_CON EINT D De-bounce Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																

Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINTD_EN	EINTD_PRESCALER				EINTD_POL	EINTD_CNT									
Type	RW	RW				RW	RW									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	EINTD_EN	De-bounce control circuit 0: Disable 1: Enable
14:12	EINTD_PRESCALER	Determine the clock cycle period for debounce count. 3'b000: 32768Hz, max 3'b001: 16384Hz 3'b010: 8192Hz 3'b011: 4096Hz 3'b100: 2048Hz, max 3'b101: 1024Hz 3'b110: 512Hz 3'b111: 256Hz, max
11	EINTD_POL	Activation type of the EINT source 0: Negative polarity 1: Positive polarity
10:0	EINTD_CNT	De-bounce duration in terms of numbers of 32768Hz clock cycles. The cycle length is determined by PRESCALER

151A0200		EINTE_CON				EINT E De-bounce Control Register											00000000	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16		
Name																		
Type																		
Reset																		
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
Name	EINTE_EN	EINTE_PRESCALER				EINTE_POL	EINTE_CNT											
Type	RW	RW				RW	RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

Bit(s)	Name	Description
15	EINTE_EN	De-bounce control circuit 0: Disable 1: Enable
14:12	EINTE_PRESCALER	Determine the clock cycle period for debounce count. 3'b000: 32768Hz, max 3'b001: 16384Hz 3'b010: 8192Hz 3'b011: 4096Hz 3'b100: 2048Hz, max 3'b101: 1024Hz 3'b110: 512Hz 3'b111: 256Hz, max
11	EINTE_POL	Activation type of the EINT source 0: Negative polarity 1: Positive polarity
10:0	EINTE_CNT	De-bounce duration in terms of numbers of 32768Hz clock cycles. The cycle length is determined by PRESCALER

151A0210 **EINTF_CON** EINT F De-bounce Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINTF_EN	EINTF_PRESCALER				EINTF_POL	EINTF_CNT									
Type	RW	RW				RW	RW									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	EINTF_EN	De-bounce control circuit 0: Disable 1: Enable
14:12	EINTF_PRESCALER	Determine the clock cycle period for debounce count. 3'b000: 32768Hz, max 3'b001: 16384Hz 3'b010: 8192Hz 3'b011: 4096Hz 3'b100: 2048Hz, max 3'b101: 1024Hz 3'b110: 512Hz 3'b111: 256Hz, max
11	EINTF_POL	Activation type of the EINT source

Bit(s)	Name	Description
10:0	EINTF_CNT	0: Negative polarity 1: Positive polarity De-bounce duration in terms of numbers of 32768Hz clock cycles. The cycle length is determined by PRESCALER

151A0220 EINT10_CON EINT 10 De-bounce Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT10_EN	EINT10_PRESCALER				EINT10_POL	EINT10_CNT									
Type	RW	RW				RW	RW									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	EINT10_EN	De-bounce control circuit 0: Disable 1: Enable
14:12	EINT10_PRESCALER	Determine the clock cycle period for debounce count. 3'b000: 32768Hz, max 3'b001: 16384Hz 3'b010: 8192Hz 3'b011: 4096Hz 3'b100: 2048Hz, max 3'b101: 1024Hz 3'b110: 512Hz 3'b111: 256Hz, max
11	EINT10_POL	Activation type of the EINT source 0: Negative polarity 1: Positive polarity
10:0	EINT10_CNT	De-bounce duration in terms of numbers of 32768Hz clock cycles. The cycle length is determined by PRESCALER

151A0230 EINT11_CON EINT 11 De-bounce Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																

Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT11_EN	EINT11_PRESCALER			EINT11_POL	EINT11_CNT										
Type	RW	RW			RW	RW										
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	EINT11_EN	De-bounce control circuit 0: Disable 1: Enable
14:12	EINT11_PRESCALER	Determine the clock cycle period for debounce count. 3'b000: 32768Hz, max 3'b001: 16384Hz 3'b010: 8192Hz 3'b011: 4096Hz 3'b100: 2048Hz, max 3'b101: 1024Hz 3'b110: 512Hz 3'b111: 256Hz, max
11	EINT11_POL	Activation type of the EINT source 0: Negative polarity 1: Positive polarity
10:0	EINT11_CNT	De-bounce duration in terms of numbers of 32768Hz clock cycles. The cycle length is determined by PRESCALER

151A0240		EINT12_CON				EINT 12 De-bounce Control Register											00000000	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16		
Name																		
Type																		
Reset																		
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
Name	EINT12_EN	EINT12_PRESCALER			EINT12_POL	EINT12_CNT												
Type	RW	RW			RW	RW												
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

Bit(s)	Name	Description
15	EINT12_EN	De-bounce control circuit 0: Disable 1: Enable
14:12	EINT12_PRESCALER	Determine the clock cycle period for debounce count. 3'b000: 32768Hz, max 3'b001: 16384Hz 3'b010: 8192Hz 3'b011: 4096Hz 3'b100: 2048Hz, max 3'b101: 1024Hz 3'b110: 512Hz 3'b111: 256Hz, max
11	EINT12_POL	Activation type of the EINT source 0: Negative polarity 1: Positive polarity
10:0	EINT12_CNT	De-bounce duration in terms of numbers of 32768Hz clock cycles. The cycle length is determined by PRESCALER

151A0250 **EINT13_CON** EINT 13 De-bounce Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT13_EN	EINT13_PRESCALER				EINT13_POL	EINT13_CNT									
Type	RW	RW				RW	RW									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	EINT13_EN	De-bounce control circuit 0: Disable 1: Enable
14:12	EINT13_PRESCALER	Determine the clock cycle period for debounce count. 3'b000: 32768Hz, max 3'b001: 16384Hz 3'b010: 8192Hz 3'b011: 4096Hz 3'b100: 2048Hz, max 3'b101: 1024Hz 3'b110: 512Hz 3'b111: 256Hz, max
11	EINT13_POL	Activation type of the EINT source

Bit(s)	Name	Description
10:0	EINT13_CNT	0: Negative polarity 1: Positive polarity De-bounce duration in terms of numbers of 32768Hz clock cycles. The cycle length is determined by PRESCALER

151A0400 **IRQ_SRC** monitor IRQ source 0~31 for debug 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	IRQ_SRC															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IRQ_SRC															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	IRQ_SRC	monitor IRQ source 0~31 for debug

151A0404 **IRQ_SRCM** monitor IRQ source 32~63 for debug 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													IRQ_SRCM			
Type													RU			
Reset													0	0	0	0

Bit(s)	Name	Description
3:0	IRQ_SRCM	monitor IRQ source 32~63 for debug

151A0408 EINT_SRC monitor EINT source for debug 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																EINT_SRC
Type																RU
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SRC															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16:0	EINT_SRC	monitor EINT source for debug

151A1000 GPT_ISR GPT Interrupt Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															GPT1_INT	GPT0_INT
Type															W1C	W1C
Reset															0	0

Bit(s)	Name	Description
1	GPT1_INT	Timer 1 interrupt. Firmware writes 1 to clear this bit, write 0 is meaningless.
0	GPT0_INT	Timer 0 interrupt. Firmware writes 1 to clear this bit, write 0 is meaningless.

151A1004 GPT_IER GPT Interrupt Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															GPT1_INT_EN	GPT0_INT_EN
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	GPT1_INT_EN	Timer 1 interrupt enable 0: Disable interrupt 1: Enable interrupt
0	GPT0_INT_EN	Timer 0 interrupt enable 0: Disable interrupt 1: Enable interrupt

151A1010 **GPT0_CTRL** **GPT0 Control Register** 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													RESTART	SPEED	MODE	EN
Type													WO	RW	RW	RW
Reset													0	0	0	0

Bit(s)	Name	Description
3	RESTART	This register will be auto-clear after restart the counter 0: No any change 1: Restart counter
2	SPEED	This register controls the unit of counter. 0: unit of 32 x 32.768/32KHz cycle 1: unit of 1 x 32.768KHz cycle
1	MODE	This register controls the timer to count repeatedly (in a loop) or just one-shot. SW needs to set this register when GPT0_CTRL[0] = 0.

Bit(s)	Name	Description
0	EN	0: One-shot mode is selected. 1: Auto-repeat mode is selected. This register controls timer to start counting or to stop. 0: timer is disabled. 1: timer is enabled

151A1014 GPT0_ICNT GPT0 Initial Counter Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CNT	Initial counting value, in unit of 32 x 32.768/32KHz (or 1 x 32.768KHz) cycle. The unit depends on the value of GPT0_CTRL[2]. The timer runs on 32.768KHz and counts down from this value whenever enabled. When timer counts down to zero, an interrupt is generated. SW needs to set this register when GPT0_CTRL[0] = 0.

151A1020 GPT1_CTRL GPT1 Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													RESTART	SPEED	MODE	EN
Type													WO	RW	RW	RW
Reset													0	0	0	0

Bit(s)	Name	Description
3	RESTART	This register will be auto-clear after restart the counter 0: No any change 1: Restart counter
2	SPEED	This register controls the unit of counter. 0: unit of 32 x 32.768/32KHz cycle 1: unit of 1 x 32.768KHz cycle
1	MODE	This register controls the timer to count repeatedly (in a loop) or just one-shot. SW needs to set this register when GPT1_CTRL[0] = 0. 0: One-shot mode is selected. 1: Auto-repeat mode is selected.
0	EN	This register controls timer to start counting or to stop. 0: timer is disabled. 1: timer is enabled

151A1024	GPT1 ICNT			GPT1 Initial Counter Register												00000000	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
Name	CNT																
Type	RW																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Name	CNT																
Type	RW																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Bit(s)	Name	Description
31:0	CNT	Initial counting value, in unit of 32 x 32.768/32KHz (or 1 x 32.768KHz) cycle. The unit depends on the value of GPT1_CTRL[2]. The timer runs on 32.768KHz and counts down from this value whenever enabled. When timer counts down to zero, an interrupt is generated. SW needs to set this register when GPT1_CTRL[0] = 0.

151A1030		GPT2_CTRL		GPT2 Control Register												00000000	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
Name																	
Type																	
Reset																	

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															SPEED	EN
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	SPEED	This register controls the unit of counter. 0: unit of 32.768/32KHz cycle 1: unit of 1 x 32.768KHz cycle
0	EN	This register controls timer to start counting or to stop. 0: timer is disabled. 1: timer is enabled

151A1034 GPT2_CNT GPT2 Counter Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CNT															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CNT															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CNT	Initial / Counting value, in unit of 32 x 32.768/32KHz cycle. This counter counts from initial value after enable. When GPT2_CTRL[0] (ie. gpt2_en) is 0, this register is used to for counter initial value setting. Its type is R/W. When GPT2_CTRL[0] (ie. gpt2_en) is 1, this register is used to for current counting value reading. Once the gpt2_en is turned on, the current counting value can be read out after 3T 32kHz clock.

151A1040 GPT0_CNT GPT0 Counter Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CNT															
Type	RU															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CNT															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CNT	Current counter value, in unit of 32 x 32.768/32KHz cycle (or 1 x 32.768KHz cycle). Once the gpt0_en is turned on, the current counting value can be read out after 3T 32kHz clock.

151A1044 GPT1_CNT GPT1 Counter Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CNT															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CNT															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CNT	Current counter value, in unit of 32 x 32.768/32KHz cycle (or 1 x 32.768KHz cycle). Once the gpt1_en is turned on, the current counting value can be read out after 3T 32kHz clock.

151A1050 GPT3_CTRL GPT3 Control Register 00190000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											OSC_CNT_1US					
Type											RW					
Reset											0	1	1	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	GPT3_I CLR											GPT3_I NT_EN				GPT3_ EN
Type	RW											RW				RW
Reset	0											0				0

Bit(s)	Name	Description
21:16	OSC_CNT_1US	The interval of tick of GPT3 [for 7615]. When osc_ck is 26MHz, OSC_CNT_1US = 26-1=25.
15	GPT3_ICLR	GPT3 interrupt clear. [6630 E2] 0: interrupt clear is disabled 1: interrupt clear is enable
4	GPT3_INT_EN	Enable interrupt of GPT3. 0: GPT3 interrupt is disabled. 1: GPT3 interrupt is enabled.
0	GPT3_EN	Enable of GPT3. 0: GPT3 is disabled. 1: GPT3 is enabled, it will +1 for each 1us tick [6630 E2]

[illegible]

Bit(s)	Name	Description
31:0	GPT3_INIT	Initial value of GPT3. When GPT3 is disabled, this value will be automatically loaded into GPT3 counter.

151A1058		<u>GPT3_CNT</u>			GPT3 Counter Register											00000000	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
Name	GPT3_CNT																

Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPT3_CNT															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	GPT3_CNT	Current counter value of GPT3 When GPT3 is enabled (GPT3_EN=1), the counter will be increased by every 1us tick. This is a free-run counter[6630 E2]

151A105C GPT3_EXPIRE GPT3 Expire Value 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPT3_EXPIRE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPT3_EXPIRE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	GPT3_EXPIRE	Expire value of GPT3. When GPT3 counts to GPT3_EXPIRE, GPT3_int_b will be set to low.

151A1060 GPT4_CTRL GPT4 Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										GPT4_DIV						GPT4_EN
Type										RW						RW
Reset										0	0	0	0	0	0	0

Bit(s)	Name	Description
6:1	GPT4_DIV	This register indicates the frequency of counter = OSC_FREQ/(GPT4_DIV+1). When 1us counter is required, GPT4_DIV = OSC_FREQ-1. GPT4_DIV can't be set to the value < 3, to prevent from
0	GPT4_EN	This register controls counter to start counting or to stop. 0: counter is disabled. 1: counter is enabled

151A1064 GPT4_INIT GPT4 Initial Value 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPT4_INIT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPT4_INIT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	GPT4_INIT	Initial value of GPT4. When GPT4 is disabled, this value will be automatically loaded into GPT4 counter.

151A1068 GPT4_CNT GPT4 Counter Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPT4_CNT															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPT4_CNT															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	GPT4_CNT	Current counter value of GPT4 when GPT4 is enabled (GPT4_EN=1)

151A1070 GPT_DBGSEL GPT debug selection register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									GPT_DBGSEL							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	GPT_DBGSEL	GPT debug selection for debug probe signal

151A2030 WDT_MODE Watchdog Timer Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MODE_KEY												IRQ			ENAB LE
Type	WO												RW			RW

Reset	0	0	0	0	0	0	0	0					0			0

Bit(s)	Name	Description
15:8	MODE_KEY	Write access is allowed if MODE_KEY=0x22
3	IRQ	Issue an interrupt instead of a Watchdog Timer reset. For debug purposes, RGU issues an interrupt to the MCU instead of resetting the system. 0 Disable. 1 Enable.
0	ENABLE	Enables the Watchdog Timer. Default watchdog timer is disabled. 0: Disables the Watchdog Timer. 1: Enables the Watchdog Timer.

151A2034 **WDT_TIMEOUT** Watchdog Time-Out Interval Register 0000FFE0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TIMEOUT											TO_KEY				
Type	RW											WO				
Reset	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0

Bit(s)	Name	Description
15:5	TIMEOUT	The counter is restarted with {TIMEOUT [10:0], 11_1111_1111b}. Thus the Watchdog Timer time-out period is a multiple of $1024 * T32k = 32ms * (TIMEOUT + 1)$ if T32K is ideal. Software needs to use the timeout value for this calculation in order to closely reflect the actual time-out period.
4:0	TO_KEY	Write access is allowed if TO_KEY=08h

151A2038 **WDT_RESTART** Watchdog Timer Restart Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RESTART_KEY															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESTART_KEY															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RESTART_KEY	Restart the counter if RESTART_KEY=1971h. Only when counter is restarted, the WDT_TIMEOUT and WDT_RST_DT are loaded into the counter

151A203C WDT_STA Watchdog Timer Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HW_STA	SW_STA														
Type	RU	RU														
Reset	0	0														

Bit(s)	Name	Description
15	HW_STA	Indicates the cause of the watchdog reset. 0: Reset not due to Watchdog Timer. 1: Reset because the Watchdog Timer time-out period expired.
14	SW_STA	Indicates if the watchdog was triggered by software. 0: Reset not due to software-triggered Watchdog Timer. 1: Reset due to software-triggered Watchdog Timer.

151A2040 WDT_RST_DT Watchdog Reset Duration Register 00000FFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RST_DURATION											
Type					RW											
Reset					1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
11:0	RST_DURATION	This register indicates the reset duration when Watchdog Timer times out. However, if the WDT_MODE register IRQ bit is set to 1, an interrupt is issued instead of a reset.

151A2044 WDT_SWRST Watchdog Timer Software Reset Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SWRST_KEY															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	SWRST_KEY	Software-triggered Watchdog Timer reset. If the register content matches the SWRST_KEY, a watchdog reset is issued. However, if the WDT_MODE register IRQ bit is set to 1, an interrupt is issued instead of a reset. SWRST_Key = 1209h

151A2050 WDT_IRQEN_B Watchdog Timer IRQ Enable Register 00000002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name																	IRQEN_B_1	IRQEN_B_0
Type																	RW	RW
Reset																	1	0

Bit(s)	Name	Description
1	IRQEN_B_1	active low interrupt enable to AP side, 1: disable, 0: enable
0	IRQEN_B_0	active low interrupt enable to CONN_MCU_CIRQ, 1: disable, 0: enable

151A3000 BT_WR_DATA UART BT TX Write Data Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BT_WR_DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	BT_WR_DATA	BT TX data register. If BT_TX_BSY is low, ARM can write data into this data register. If BT_TX_BSY is high, ARM cannot write data into this register and BT_TX_OVF will hold high. Write Command is asserted to send the output data through the "TXD" pin.

151A3004 WF_WR_DATA UART WF TX Write Data Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WF_WR_DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	WF_WR_DATA	WiFi TX data register. If WF_TX_BSY is low, ARM can write data into this data register. If WF_TX_BSY is high, ARM cannot write data into this register and WF_TX_OVF will hold high. Write Command is asserted to send the output data through the "TXD" pin.

151A3008 STA Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													WF_TX_OVF	BT_TX_OVF	WF_TX_BSY	BT_TX_BSY
Type													RU	RU	RU	RU
Reset													0	0	0	0

Bit(s)	Name	Description
3	WF_TX_OVF	WiFi TX data overflow flag. If WF_TX_BSY is high and ARM write WF_WR_DATA again, this flag would hold high and only cleared by software reset. SW can clear it by write 1 to CTRL1[0].
2	BT_TX_OVF	BT TX data overflow flag. If BT_TX_BSY is high and ARM write BT_WR_DATA again, this flag would hold high and only cleared by software reset. SW can clear it by write 1 to CTRL1[0].
1	WF_TX_BSY	When ARM set the WF_WR_DATA, this flag will set to "1". Data will not transmit until BT_TX_BSY is low. This flag will be low when WF_WR_DATA transmit finished. SW can abort Tx by write 1 to CTRL1[0]. This is for debug purpose.
0	BT_TX_BSY	When ARM set the BT_WR_DATA, this flag will set to "1". Data will not transmit until WF_TX_BSY is low. This flag will be low when BT_WR_DATA transmit finished. SW can abort Tx by write 1 to CTRL1[0]. This is for debug purpose.

151A300C CTRL1 UART Control 1 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											BAUD_RATE					TXCLR
Type											RW					WO
Reset											0	0				0

Bit(s)	Name	Description
5:4	BAUD_RATE	UART serial port baud rate select. "00": 115200bps "01": 230400bps "10": 460800bps "11": 921600bps
0	TXCLR	Write this bit "1" to clear TX registers.

151A3010 BCDF_BASE0 Baud Rate Divider 0 000000E1

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							BCDF_BASE0									
Type							RW									
Reset							0	0	1	1	1	0	0	0	0	1

Bit(s)	Name	Description
9:0	BCDF_BASE0	BCDF_BASE0 = TCXO/115200. De-sense UART will support baud from 115200 to 921600. They are 115200, 230400, 460800, and 921600. These baud rates are multiples of 115200. Processor can set baud rate selection register BCDF_RATE[1:0] to obtain what you want. Example: The TCXO=26M, BCDF_BASE0 default is 26M/115200= 0xE1.

Bit(s)	Name	Description
		If you need different Baud Rate, please set 0x800A000C[5:4] = 0 and BCDF_BASE0 = TCXO/Baud Rate. Example: If you need Baud Rate = 3.25M, the BCDF_BASE0 = 26M/3.25M = 0x8.

151A3014 **ADJUST** Baud Rate Adjust 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									ADJUST							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	ADJUST	Baud rate counter adjustment. The baud rate counter will be BCDF register bitwise plus 1.

151A7000 **HANG_DET_CTL** Hang Detection Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	INT_STS		INT_EN													
Type	W1C		RW													
Reset	0	0	0	0												
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RST_CYC_CNT	HANG_DET_EN
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
31:30	INT_STS	INT status write 1 to clear bit[30] for INT_EN[28] bit[31] for INT_EN[29] 1: INT pending 0: INT not pending
29:28	INT_EN	NMI Interrupt enable bit[28] for PC hang INT enable bit[29] for PC hit INT enable 1: enable 0: disable
1	RST_CYC_CNT	Reset hang cycle counter write 1 to reset, then write 0 to release reset
0	HANG_DET_EN	CPU hang detection enable 1: enable 0: disable

151A7004 HANG_CYC_THRE Hang cycle threshold 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	HANG_CYC_THRE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HANG_CYC_THRE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	HANG_CYC_THRE	Hang cycle threshold If checked PC remains the same for the specified cycle number, it is detected as CPU hang, and INT is issued if enabled.

151A7008 PC_CHK_BITMAP PC check bitmap FFFFFFFC

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PC_CHK_BITMAP															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PC_CHK_BITMAP															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	PC_CHK_BITMAP	Program Counter Check Bitmap Don't check LSB parts to mimic locality. When the check part of PC remains the same, it is thought that PC resides in a loop. 1: check 0: don't check

151A700C IGN_ADDR_CFG Ignored Address Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									IGN_EN							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	IGN_EN	Ignore enable Bit N is enable bit for ignore address CR N 1: ignore address CR N 0: don't ignore address CR N

151A7010 IGN_ADDR_0 Ignored Address 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	IGN_ADDR_0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IGN_ADDR_0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	IGN_ADDR_0	Ignore address 0

151A7014 IGN_ADDR_1 Ignore Address 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	IGN_ADDR_1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IGN_ADDR_1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	IGN_ADDR_1	Ignore address 1

151A7018 IGN_ADDR_2 Ignore Address 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	IGN_ADDR_2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IGN_ADDR_2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	IGN_ADDR_2	Ignore address 2

151A701C **IGN_ADDR_3** **Ignore Address 3** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	IGN_ADDR_3															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IGN_ADDR_3															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	IGN_ADDR_3	Ignore address 3

151A7020 **IGN_ADDR_4** **Ignore Address 4** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	IGN_ADDR_4															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IGN_ADDR_4															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	IGN_ADDR_4	Ignore address 4

151A7024 **IGN_ADDR_5** **Ignore Address 5** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	IGN_ADDR_5															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IGN_ADDR_5															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	IGN_ADDR_5	Ignore address 5

151A7028 IGN_ADDR_6 Ignore Address 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	IGN_ADDR_6															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IGN_ADDR_6															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	IGN_ADDR_6	Ignore address 6

151A702C IGN_ADDR_7 Ignore Address 7 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	IGN_ADDR_7															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	IGN_ADDR_7															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	IGN_ADDR_7	Ignore address 7

151A7030 RO_CHK_PC current checked PC 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RO_CHK_PC															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RO_CHK_PC															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_CHK_PC	current checked PC

151A7034 RO_CYC_CNT current cycle counter 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RO_CYC_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RO_CYC_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_CYC_CNT	current cycle counter (of current checked PC)

151A7038 PC_MON_CTL PC monitor control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RST_PC_MON_STS															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PC_MON_EN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	RST_PC_MON_STS	Reset PC monitor status write 1, and then write 0 to reset PC_MON_STS
15:0	PC_MON_EN	PC monitor enable bit[0] is corresponding to MON_PC_CFG0 bit[1] is corresponding to MON_PC_CFG1, etc. 1: enable 0: disable

151A703C PC_MON_STS PC monitor status 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RO_PC_MON_STS															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RO_PC_MON_STS	Latched PC_MON_STS when INT is triggered If INT is enabled, for SW to find which monitor address is hit 1: monitor enable, and corresponding PC was hit 0: monitor disable, or corresponding PC was not hit

151A7040 MON_PC_CFG0 Monitor PC config 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MON_ADDR_0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MON_ADDR_0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MON_ADDR_0	monitor address

151A7044 MON_PC_CFG1 Monitor PC config 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MON_ADDR_1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MON_ADDR_1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MON_ADDR_1	monitor address

151A7048 MON_PC_CFG2 Monitor PC config 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MON_ADDR_2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MON_ADDR_2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MON_ADDR_2	monitor address

151A704C MON_PC_CFG3 Monitor PC config 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MON_ADDR_3															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MON_ADDR_3															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MON_ADDR_3	monitor address

151A7050 MON_PC_CFG4 Monitor PC config 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MON_ADDR_4															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MON_ADDR_4															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MON_ADDR_4	monitior address

151A7054 MON_PC_CFG5 Monitor PC config 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MON_ADDR_5															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MON_ADDR_5															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MON_ADDR_5	monitior address

151A7058 MON_PC_CFG6 Monitor PC config 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MON_ADDR_6															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MON_ADDR_6															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MON_ADDR_6	montior address

151A705C MON_PC_CFG7 Monitor PC config 7 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MON_ADDR_7															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MON_ADDR_7															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MON_ADDR_7	montior address

151A7060 MON_PC_CFG8 Monitor PC config 8 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MON_ADDR_8															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MON_ADDR_8															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MON_ADDR_8	montior address

151A7064 MON_PC_CFG9 Monitor PC config 9 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	MON_ADDR_9															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MON_ADDR_9															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MON_ADDR_9	monitior address

151A7068 MON_PC_CFG10 Monitor PC config 10 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MON_ADDR_10															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MON_ADDR_10															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MON_ADDR_10	monitior address

151A706C MON_PC_CFG11 Monitor PC config 11 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MON_ADDR_11															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	MON_ADDR_11															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MON_ADDR_11	monitior address

151A7070 MON_PC_CFG12 Monitor PC config 12 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MON_ADDR_12															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MON_ADDR_12															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MON_ADDR_12	monitior address

151A7074 MON_PC_CFG13 Monitor PC config 13 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MON_ADDR_13															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MON_ADDR_13															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MON_ADDR_13	montior address

151A7078 MON_PC_CFG14 Monitor PC config 14 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MON_ADDR_14															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MON_ADDR_14															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MON_ADDR_14	montior address

151A707C MON_PC_CFG15 Monitor PC config 15 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MON_ADDR_15															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MON_ADDR_15															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MON_ADDR_15	montior address

151A7080 SW_DBG_CTL SW DEBUG CONTROL 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	SW_DBG_CTL															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SW_DBG_CTL															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SW_DBG_CTL	SW debug index

151A7090 MCU_DBG_IF_CMD MCU_DBG_IF_CMD 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MCU_DBG_IF_CMD															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MCU_DBG_IF_CMD															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MCU_DBG_IF_CMD	MCU_DBG_IF_CMD

151A7094 MCU_DBG_IF_ARG0 MCU_DBG_IF_ARG0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MCU_DBG_IF_ARG0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	MCU_DBG_IF_ARG0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MCU_DBG_IF_ARG0	MCU_DBG_IF_ARG0

151A7098 MCU_DBG_IF_ARG1 MCU_DBG_IF_ARG1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MCU_DBG_IF_ARG1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MCU_DBG_IF_ARG1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MCU_DBG_IF_ARG1	MCU_DBG_IF_ARG1

151A709C MCU_DBG_IF_CTL MCU_DBG_IF_CTL 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																MCU_DBG_IF_SW_I RQ
Type																RW
Reset																0

Bit(s)	Name	Description
0	MCU_DBG_IF_SW_IRQ	MCU_DBG_IF_SW_IRQ 1'b0: Not issue interrupt 1'b1: Issue interrupt

151A7100 DBG_PC_LOG_CTL DBG_PC_LOG_CTL 001E06FC

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DBG_PC_LOG_THRESHOLD								DBG_PC_LOG_SEL							DBG_PC_LOG_SEL_SRC
Type	RW								RW							RW
Reset	0	0	0	0	0	1	1	0	1	1	1	1	1	1	0	0

Bit(s)	Name	Description
15:8	DBG_PC_LOG_THRESHOLD	DBG_PC_LOG_THRESHOLD
7:2	DBG_PC_LOG_SEL	DBG_PC_LOG_SEL
1	DBG_PC_LOG_SEL_SRC	DBG_PC_LOG_SEL_SRC 1'b0 : mux selection source from AP/HIF 1'b1 : mux selection source from MCUSYS
0	DBG_PC_LOG_EN	DBG_PC_LOG_EN

151A7104 DBG_PC_LOG_0 DBG_PC_LOG_0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RO_DBG_PC_LOG_0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RO_DBG_PC_LOG_0															
Type	RO															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_DBG_PC_LOG_0	DBG_PC_LOG_0 (source pc 1)

151A7108 DBG_PC_LOG_1 DBG_PC_LOG_1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RO_DBG_PC_LOG_1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RO_DBG_PC_LOG_1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_DBG_PC_LOG_1	DBG_PC_LOG_1 (destination pc 1)

151A710C DBG_PC_LOG_2 DBG_PC_LOG_2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RO_DBG_PC_LOG_2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RO_DBG_PC_LOG_2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_DBG_PC_LOG_2	DBG_PC_LOG_2 (source pc 2)

151A7110 **DBG_PC_LOG_3** **DBG_PC_LOG_3** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RO_DBG_PC_LOG_3															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RO_DBG_PC_LOG_3															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_DBG_PC_LOG_3	DBG_PC_LOG_3 (destination pc 2)

151A7114 **DBG_PC_LOG_4** **DBG_PC_LOG_4** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RO_DBG_PC_LOG_4															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RO_DBG_PC_LOG_4															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_DBG_PC_LOG_4	DBG_PC_LOG_4 (source pc 3)

151A7118 **DBG_PC_LOG_5** **DBG_PC_LOG_5** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RO_DBG_PC_LOG_5															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RO_DBG_PC_LOG_5															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_DBG_PC_LOG_5	DBG_PC_LOG_5 (destination pc 3)

151A711C DBG_PC_LOG_6 DBG_PC_LOG_6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RO_DBG_PC_LOG_6															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RO_DBG_PC_LOG_6															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_DBG_PC_LOG_6	DBG_PC_LOG_6 (source pc 4)

151A7120 DBG_PC_LOG_7 DBG_PC_LOG_7 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RO_DBG_PC_LOG_7															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RO_DBG_PC_LOG_7															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_DBG_PC_LOG_7	DBG_PC_LOG_7 (destination pc 4)

151A7124 **DBG_PC_LOG_8** **DBG_PC_LOG_8** 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RO_DBG_PC_LOG_8															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RO_DBG_PC_LOG_8															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_DBG_PC_LOG_8	DBG_PC_LOG_8 (source pc 5)

151A7128 **DBG_PC_LOG_9** **DBG_PC_LOG_9** 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RO_DBG_PC_LOG_9															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RO_DBG_PC_LOG_9															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_DBG_PC_LOG_9	DBG_PC_LOG_9 (destination pc 5)

151A712C **DBG_PC_LOG_10** **DBG_PC_LOG_10** 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	RO_DBG_PC_LOG_10															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RO_DBG_PC_LOG_10															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_DBG_PC_LOG_10	DBG_PC_LOG_10 (source pc 6)

151A7130 DBG_PC_LOG_11 DBG_PC_LOG_11 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RO_DBG_PC_LOG_11															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RO_DBG_PC_LOG_11															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_DBG_PC_LOG_11	DBG_PC_LOG_11 (destination pc 6)

151A7134 DBG_PC_LOG_12 DBG_PC_LOG_12 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RO_DBG_PC_LOG_12															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	RO_DBG_PC_LOG_12															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_DBG_PC_LOG_12	DBG_PC_LOG_12 (source pc 7)

151A7138 DBG_PC_LOG_13 DBG_PC_LOG_13 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RO_DBG_PC_LOG_13															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RO_DBG_PC_LOG_13															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_DBG_PC_LOG_13	DBG_PC_LOG_13 (destination pc 7)

151A713C DBG_PC_LOG_14 DBG_PC_LOG_14 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RO_DBG_PC_LOG_14															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RO_DBG_PC_LOG_14															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_DBG_PC_LOG_14	DBG_PC_LOG_14 (source pc 8)

151A7140 **DBG_PC_LOG_15** **DBG_PC_LOG_15** 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RO_DBG_PC_LOG_15															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RO_DBG_PC_LOG_15															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_DBG_PC_LOG_15	DBG_PC_LOG_15 (destination pc 8)

151A7144 **DBG_PC_LOG_16** **DBG_PC_LOG_16** 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RO_DBG_PC_LOG_16															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RO_DBG_PC_LOG_16															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_DBG_PC_LOG_16	DBG_PC_LOG_16 (source pc 9)

151A7148 **DBG_PC_LOG_17** **DBG_PC_LOG_17** 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	RO_DBG_PC_LOG_17															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RO_DBG_PC_LOG_17															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_DBG_PC_LOG_17	DBG_PC_LOG_17 (destination pc 9)

151A714C DBG_PC_LOG_18 DBG_PC_LOG_18 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RO_DBG_PC_LOG_18															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RO_DBG_PC_LOG_18															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_DBG_PC_LOG_18	DBG_PC_LOG_18 (source pc 10)

151A7150 DBG_PC_LOG_19 DBG_PC_LOG_19 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RO_DBG_PC_LOG_19															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	RO_DBG_PC_LOG_19															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_DBG_PC_LOG_19	DBG_PC_LOG_19 (destination pc 10)

151A7154 DBG_PC_LOG_20 DBG_PC_LOG_20 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RO_DBG_PC_LOG_20															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RO_DBG_PC_LOG_20															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_DBG_PC_LOG_20	DBG_PC_LOG_20 (source pc 11)

151A7158 DBG_PC_LOG_21 DBG_PC_LOG_21 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RO_DBG_PC_LOG_21															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RO_DBG_PC_LOG_21															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_DBG_PC_LOG_21	DBG_PC_LOG_21 (destination pc 11)

151A715C **DBG_PC_LOG_22** **DBG_PC_LOG_22** 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RO_DBG_PC_LOG_22															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RO_DBG_PC_LOG_22															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_DBG_PC_LOG_22	DBG_PC_LOG_22 (source pc 12)

151A7160 **DBG_PC_LOG_23** **DBG_PC_LOG_23** 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RO_DBG_PC_LOG_23															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RO_DBG_PC_LOG_23															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_DBG_PC_LOG_23	DBG_PC_LOG_23 (destination pc 12)

151A7164 **DBG_PC_LOG_24** **DBG_PC_LOG_24** 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	RO_DBG_PC_LOG_24															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RO_DBG_PC_LOG_24															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_DBG_PC_LOG_24	DBG_PC_LOG_24 (source pc 13)

151A7168 DBG_PC_LOG_25 DBG_PC_LOG_25 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RO_DBG_PC_LOG_25															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RO_DBG_PC_LOG_25															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_DBG_PC_LOG_25	DBG_PC_LOG_25 (destination pc 13)

151A716C DBG_PC_LOG_26 DBG_PC_LOG_26 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RO_DBG_PC_LOG_26															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	RO_DBG_PC_LOG_26															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_DBG_PC_LOG_26	DBG_PC_LOG_26 (source pc 14)

151A7170 DBG_PC_LOG_27 DBG_PC_LOG_27 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RO_DBG_PC_LOG_27															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RO_DBG_PC_LOG_27															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_DBG_PC_LOG_27	DBG_PC_LOG_27 (destination pc 14)

151A7174 DBG_PC_LOG_28 DBG_PC_LOG_28 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RO_DBG_PC_LOG_28															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RO_DBG_PC_LOG_28															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_DBG_PC_LOG_28	DBG_PC_LOG_28 (source pc 15)

151A7178 **DBG_PC_LOG_29** **DBG_PC_LOG_29** 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RO_DBG_PC_LOG_29															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RO_DBG_PC_LOG_29															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_DBG_PC_LOG_29	DBG_PC_LOG_29 (destination pc 15)

151A717C **DBG_PC_LOG_30** **DBG_PC_LOG_30** 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RO_DBG_PC_LOG_30															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RO_DBG_PC_LOG_30															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_DBG_PC_LOG_30	DBG_PC_LOG_30 (source pc 16)

151A7180 **DBG_PC_LOG_31** **DBG_PC_LOG_31** 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	RO_DBG_PC_LOG_31															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RO_DBG_PC_LOG_31															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_DBG_PC_LOG_31	DBG_PC_LOG_31 (destination pc 16)

151A7200	DBG_GPR_LOG_CTL					DBG_GPR_LOG_CTL							03DE01FC				
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
Name						DBG_GPR_SEL											
Type						RW											
Reset						0	1	1	1	1	0						
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Name	DBG_GPR_LOG_THRESHOLD								DBG_GPR_LOG_SEL						DBG_GPR_LOG_SEL_SRC	DBG_GPR_LOG_EN	
Type	RW								RW						RW	RW	
Reset	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	

Bit(s)	Name	Description
26:21	DBG_GPR_SEL	DBG_GPR_SEL 6'd0~6'd5 : a0~a5 6'd6~6'd14 : s0~s8 6'd15 : ta 6'd16~6'd25 : t0~t9 6'd26~6'd27 : p0~p1 6'd28 : fp 6'd29 : gp 6'd30 : lp 6'd31 : sp
15:8	DBG_GPR_LOG_THRESHOLD	DBG_GPR_LOG_THRESHOLD
7:2	DBG_GPR_LOG_SEL	DBG_GPR_LOG_SEL
1	DBG_GPR_LOG_SEL_SRC	DBG_GPR_LOG_SEL_SRC

Bit(s)	Name	Description
		1'b0 : mux selection source from AP/HIF 1'b1 : mux selection source from MCUSYS
0	DBG_GPR_LOG_EN	DBG_GPR_LOG_EN

151A7204 DBG_GPR_LOG_0 DBG_GPR_LOG_0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RO_DBG_GPR_LOG_0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RO_DBG_GPR_LOG_0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_DBG_GPR_LOG_0	DBG_GPR_LOG_0 (source gpr 1)

151A7208 DBG_GPR_LOG_1 DBG_GPR_LOG_1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RO_DBG_GPR_LOG_1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RO_DBG_GPR_LOG_1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_DBG_GPR_LOG_1	DBG_GPR_LOG_1 (destination gpr 1)

151A720C DBG_GPR_LOG_2 DBG_GPR_LOG_2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RO_DBG_GPR_LOG_2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RO_DBG_GPR_LOG_2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_DBG_GPR_LOG_2	DBG_GPR_LOG_2 (source gpr 2)

151A7210 DBG_GPR_LOG_3 DBG_GPR_LOG_3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RO_DBG_GPR_LOG_3															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RO_DBG_GPR_LOG_3															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_DBG_GPR_LOG_3	DBG_GPR_LOG_3 (destination gpr 2)

151A7214 DBG_GPR_LOG_4 DBG_GPR_LOG_4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RO_DBG_GPR_LOG_4															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RO_DBG_GPR_LOG_4															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_DBG_GPR_LOG_4	DBG_GPR_LOG_4 (source gpr 3)

151A7218 DBG GPR LOG 5 DBG_GPR_LOG_5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RO_DBG_GPR_LOG_5															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RO_DBG_GPR_LOG_5															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_DBG_GPR_LOG_5	DBG_GPR_LOG_5 (destination gpr 3)

151A721C DBG GPR LOG 6 DBG_GPR_LOG_6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RO_DBG_GPR_LOG_6															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RO_DBG_GPR_LOG_6															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_DBG_GPR_LOG_6	DBG_GPR_LOG_6 (source gpr 4)

151A7220 **DBG GPR LOG 7** **DBG_GPR_LOG_7** 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RO_DBG_GPR_LOG_7															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RO_DBG_GPR_LOG_7															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_DBG_GPR_LOG_7	DBG_GPR_LOG_7 (destination gpr 4)

151A7224 **DBG GPR LOG 8** **DBG_GPR_LOG_8** 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RO_DBG_GPR_LOG_8															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RO_DBG_GPR_LOG_8															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_DBG_GPR_LOG_8	DBG_GPR_LOG_8 (source gpr 5)

151A7228 **DBG GPR LOG 9** **DBG_GPR_LOG_9** 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	RO_DBG_GPR_LOG_9															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RO_DBG_GPR_LOG_9															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_DBG_GPR_LOG_9	DBG_GPR_LOG_9 (destination gpr 5)

151A722C DBG_GPR_LOG_10 DBG_GPR_LOG_10 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RO_DBG_GPR_LOG_10															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RO_DBG_GPR_LOG_10															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_DBG_GPR_LOG_10	DBG_GPR_LOG_10 (source gpr 6)

151A7230 DBG_GPR_LOG_11 DBG_GPR_LOG_11 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RO_DBG_GPR_LOG_11															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	RO_DBG_GPR_LOG_11															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_DBG_GPR_LOG_11	DBG_GPR_LOG_11 (destination gpr 6)

151A7234 DBG_GPR_LOG_12 DBG_GPR_LOG_12 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RO_DBG_GPR_LOG_12															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RO_DBG_GPR_LOG_12															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_DBG_GPR_LOG_12	DBG_GPR_LOG_12 (source gpr 7)

151A7238 DBG_GPR_LOG_13 DBG_GPR_LOG_13 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RO_DBG_GPR_LOG_13															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RO_DBG_GPR_LOG_13															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_DBG_GPR_LOG_13	DBG_GPR_LOG_13 (destination gpr 7)

151A723C **DBG GPR LOG 14** **DBG_GPR_LOG_14** 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RO_DBG_GPR_LOG_14															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RO_DBG_GPR_LOG_14															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_DBG_GPR_LOG_14	DBG_GPR_LOG_14 (source gpr 8)

151A7240 **DBG GPR LOG 15** **DBG_GPR_LOG_15** 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RO_DBG_GPR_LOG_15															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RO_DBG_GPR_LOG_15															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_DBG_GPR_LOG_15	DBG_GPR_LOG_15 (destination gpr 8)

151A7244 **DBG GPR LOG 16** **DBG_GPR_LOG_16** 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	RO_DBG_GPR_LOG_16															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RO_DBG_GPR_LOG_16															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_DBG_GPR_LOG_16	DBG_GPR_LOG_16 (source gpr 9)

151A7248 DBG_GPR_LOG_17 DBG_GPR_LOG_17 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RO_DBG_GPR_LOG_17															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RO_DBG_GPR_LOG_17															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_DBG_GPR_LOG_17	DBG_GPR_LOG_17 (destination gpr 9)

151A724C DBG_GPR_LOG_18 DBG_GPR_LOG_18 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RO_DBG_GPR_LOG_18															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	RO_DBG_GPR_LOG_18															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_DBG_GPR_LOG_18	DBG_GPR_LOG_18 (source gpr 10)

151A7250 DBG_GPR_LOG_19 DBG_GPR_LOG_19 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RO_DBG_GPR_LOG_19															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RO_DBG_GPR_LOG_19															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_DBG_GPR_LOG_19	DBG_GPR_LOG_19 (destination gpr 10)

151A7254 DBG_GPR_LOG_20 DBG_GPR_LOG_20 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RO_DBG_GPR_LOG_20															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RO_DBG_GPR_LOG_20															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_DBG_GPR_LOG_20	DBG_GPR_LOG_20 (source gpr 11)

151A7258 **DBG_GPR_LOG_21** **DBG_GPR_LOG_21** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RO_DBG_GPR_LOG_21															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RO_DBG_GPR_LOG_21															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_DBG_GPR_LOG_21	DBG_GPR_LOG_21 (destination gpr 11)

151A725C **DBG_GPR_LOG_22** **DBG_GPR_LOG_22** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RO_DBG_GPR_LOG_22															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RO_DBG_GPR_LOG_22															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_DBG_GPR_LOG_22	DBG_GPR_LOG_22 (source gpr 12)

151A7260 **DBG_GPR_LOG_23** **DBG_GPR_LOG_23** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	RO_DBG_GPR_LOG_23															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RO_DBG_GPR_LOG_23															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_DBG_GPR_LOG_23	DBG_GPR_LOG_23 (destination gpr 12)

151A7264 DBG_GPR_LOG_24 DBG_GPR_LOG_24 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RO_DBG_GPR_LOG_24															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RO_DBG_GPR_LOG_24															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_DBG_GPR_LOG_24	DBG_GPR_LOG_24 (source gpr 13)

151A7268 DBG_GPR_LOG_25 DBG_GPR_LOG_25 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RO_DBG_GPR_LOG_25															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	RO_DBG_GPR_LOG_25															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_DBG_GPR_LOG_25	DBG_GPR_LOG_25 (destination gpr 13)

151A726C DBG_GPR_LOG_26 DBG_GPR_LOG_26 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RO_DBG_GPR_LOG_26															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RO_DBG_GPR_LOG_26															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_DBG_GPR_LOG_26	DBG_GPR_LOG_26 (source gpr 14)

151A7270 DBG_GPR_LOG_27 DBG_GPR_LOG_27 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RO_DBG_GPR_LOG_27															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RO_DBG_GPR_LOG_27															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_DBG_GPR_LOG_27	DBG_GPR_LOG_27 (destination gpr 14)

151A7274 **DBG GPR LOG 28** **DBG_GPR_LOG_28** 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RO_DBG_GPR_LOG_28															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RO_DBG_GPR_LOG_28															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_DBG_GPR_LOG_28	DBG_GPR_LOG_28 (source gpr 15)

151A7278 **DBG GPR LOG 29** **DBG_GPR_LOG_29** 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RO_DBG_GPR_LOG_29															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RO_DBG_GPR_LOG_29															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_DBG_GPR_LOG_29	DBG_GPR_LOG_29 (destination gpr 15)

151A727C **DBG GPR LOG 30** **DBG_GPR_LOG_30** 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	RO_DBG_GPR_LOG_30															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RO_DBG_GPR_LOG_30															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_DBG_GPR_LOG_30	DBG_GPR_LOG_30 (source gpr 16)

151A7280 DBG_GPR_LOG_31 DBG_GPR_LOG_31 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RO_DBG_GPR_LOG_31															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RO_DBG_GPR_LOG_31															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_DBG_GPR_LOG_31	DBG_GPR_LOG_31 (destination gpr 16)

151A8000 IRQ_SELO IRQ Selection 0 Register 03020100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	IRQ3_SEL								IRQ2_SEL							
Type	RW								RW							
Reset			0	0	0	0	1	1			0	0	0	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name			IRQ1_SEL								IRQ0_SEL					
Type			RW								RW					
Reset			0	0	0	0	0	1			0	0	0	0	0	0

Bit(s)	Name	Description
29:24	IRQ3_SEL	Interrupt source selector 6'h0~6'h3f: Please reference to interrupt source table
21:16	IRQ2_SEL	Interrupt source selector 6'h0~6'h3f: Please reference to interrupt source table
13:8	IRQ1_SEL	Interrupt source selector 6'h0~6'h3f: Please reference to interrupt source table
5:0	IRQ0_SEL	Interrupt source selector 6'h0~6'h3f: Please reference to interrupt source table

151A8004 IRQ_SEL1 IRQ Selection 1 Register 07060504

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			IRQ7_SEL								IRQ6_SEL					
Type			RW								RW					
Reset			0	0	0	1	1	1			0	0	0	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			IRQ5_SEL								IRQ4_SEL					
Type			RW								RW					
Reset			0	0	0	1	0	1			0	0	0	1	0	0

Bit(s)	Name	Description
29:24	IRQ7_SEL	Interrupt source selector 6'h0~6'h3f: Please reference to interrupt source table
21:16	IRQ6_SEL	Interrupt source selector 6'h0~6'h3f: Please reference to interrupt source table
13:8	IRQ5_SEL	Interrupt source selector 6'h0~6'h3f: Please reference to interrupt source table
5:0	IRQ4_SEL	Interrupt source selector 6'h0~6'h3f: Please reference to interrupt source table

151A8008 IRQ_SEL2 IRQ Selection 2 Register 0B0A0908

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name			IRQB_SEL								IRQA_SEL					
Type			RW								RW					
Reset			0	0	1	0	1	1			0	0	1	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			IRQ9_SEL								IRQ8_SEL					
Type			RW								RW					
Reset			0	0	1	0	0	1			0	0	1	0	0	0

Bit(s)	Name	Description
29:24	IRQB_SEL	Interrupt source selector 6'h0~6'h3f: Please reference to interrupt source table
21:16	IRQA_SEL	Interrupt source selector 6'h0~6'h3f: Please reference to interrupt source table
13:8	IRQ9_SEL	Interrupt source selector 6'h0~6'h3f: Please reference to interrupt source table
5:0	IRQ8_SEL	Interrupt source selector 6'h0~6'h3f: Please reference to interrupt source table

151A800C **IRQ_SEL3** IRQ Selection 3 Register 0F0E0D0C

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			IRQF_SEL								IRQE_SEL					
Type			RW								RW					
Reset			0	0	1	1	1	1			0	0	1	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			IRQD_SEL								IRQC_SEL					
Type			RW								RW					
Reset			0	0	1	1	0	1			0	0	1	1	0	0

Bit(s)	Name	Description
29:24	IRQF_SEL	Interrupt source selector 6'h0~6'h3f: Please reference to interrupt source table
21:16	IRQE_SEL	Interrupt source selector 6'h0~6'h3f: Please reference to interrupt source table
13:8	IRQD_SEL	Interrupt source selector 6'h0~6'h3f: Please reference to interrupt source table
5:0	IRQC_SEL	Interrupt source selector 6'h0~6'h3f: Please reference to interrupt source table

Bit(s)	Name	Description
6'h0~6'h3f: Please reference to interrupt source table		

151A8010 **IRQ_SEL4** **IRQ Selection 4 Register** 13121110

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			IRQ13_SEL								IRQ12_SEL					
Type			RW								RW					
Reset			0	1	0	0	1	1			0	1	0	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			IRQ11_SEL								IRQ10_SEL					
Type			RW								RW					
Reset			0	1	0	0	0	1			0	1	0	0	0	0

Bit(s)	Name	Description
29:24	IRQ13_SEL	Interrupt source selector 6'h0~6'h3f: Please reference to interrupt source table
21:16	IRQ12_SEL	Interrupt source selector 6'h0~6'h3f: Please reference to interrupt source table
13:8	IRQ11_SEL	Interrupt source selector 6'h0~6'h3f: Please reference to interrupt source table
5:0	IRQ10_SEL	Interrupt source selector 6'h0~6'h3f: Please reference to interrupt source table

151A8014 **IRQ_SEL5** **IRQ Selection 5 Register** 17161514

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			IRQ17_SEL								IRQ16_SEL					
Type			RW								RW					
Reset			0	1	0	1	1	1			0	1	0	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			IRQ15_SEL								IRQ14_SEL					
Type			RW								RW					
Reset			0	1	0	1	0	1			0	1	0	1	0	0

Bit(s)	Name	Description
29:24	IRQ17_SEL	Interrupt source selector 6'h0~6'h3f: Please reference to interrupt source table
21:16	IRQ16_SEL	Interrupt source selector 6'h0~6'h3f: Please reference to interrupt source table
13:8	IRQ15_SEL	Interrupt source selector 6'h0~6'h3f: Please reference to interrupt source table
5:0	IRQ14_SEL	Interrupt source selector 6'h0~6'h3f: Please reference to interrupt source table

151A8018 **IRQ_SEL6** **IRQ Selection 6 Register** **1B1A1918**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			IRQ1B_SEL								IRQ1A_SEL					
Type			RW								RW					
Reset			0	1	1	0	1	1			0	1	1	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			IRQ19_SEL								IRQ18_SEL					
Type			RW								RW					
Reset			0	1	1	0	0	1			0	1	1	0	0	0

Bit(s)	Name	Description
29:24	IRQ1B_SEL	Interrupt source selector 6'h0~6'h3f: Please reference to interrupt source table
21:16	IRQ1A_SEL	Interrupt source selector 6'h0~6'h3f: Please reference to interrupt source table
13:8	IRQ19_SEL	Interrupt source selector 6'h0~6'h3f: Please reference to interrupt source table
5:0	IRQ18_SEL	Interrupt source selector 6'h0~6'h3f: Please reference to interrupt source table

151A801C **IRQ_SEL7** **IRQ Selection 7 Register** **1F1E1D1C**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			IRQ1F_SEL								IRQ1E_SEL					
Type			RW								RW					
Reset			0	1	1	1	1	1			0	1	1	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name			IRQ1D_SEL								IRQ1C_SEL					
Type			RW								RW					
Reset			0	1	1	1	0	1			0	1	1	1	0	0

Bit(s)	Name	Description
29:24	IRQ1F_SEL	Interrupt source selector 6'h0~6'h3f: Please reference to interrupt source table
21:16	IRQ1E_SEL	Interrupt source selector 6'h0~6'h3f: Please reference to interrupt source table
13:8	IRQ1D_SEL	Interrupt source selector 6'h0~6'h3f: Please reference to interrupt source table
5:0	IRQ1C_SEL	Interrupt source selector 6'h0~6'h3f: Please reference to interrupt source table

151A8020 IRQ_SEL8 IRQ Selection 8 Register 23222120

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			IRQ23_SEL								IRQ22_SEL					
Type			RW								RW					
Reset			1	0	0	0	1	1			1	0	0	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			IRQ21_SEL								IRQ20_SEL					
Type			RW								RW					
Reset			1	0	0	0	0	1			1	0	0	0	0	0

Bit(s)	Name	Description
29:24	IRQ23_SEL	Interrupt source selector 6'h0~6'h3f: Please reference to interrupt source table
21:16	IRQ22_SEL	Interrupt source selector 6'h0~6'h3f: Please reference to interrupt source table
13:8	IRQ21_SEL	Interrupt source selector 6'h0~6'h3f: Please reference to interrupt source table
5:0	IRQ20_SEL	Interrupt source selector 6'h0~6'h3f: Please reference to interrupt source table

151A8024 IRQ_SEL9 IRQ Selection 9 Register 27262524

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name			IRQ27_SEL								IRQ26_SEL					
Type			RW								RW					
Reset			1	0	0	1	1	1			1	0	0	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			IRQ25_SEL								IRQ24_SEL					
Type			RW								RW					
Reset			1	0	0	1	0	1			1	0	0	1	0	0

Bit(s)	Name	Description
29:24	IRQ27_SEL	Interrupt source selector 6'h0~6'h3f: Please reference to interrupt source table
21:16	IRQ26_SEL	Interrupt source selector 6'h0~6'h3f: Please reference to interrupt source table
13:8	IRQ25_SEL	Interrupt source selector 6'h0~6'h3f: Please reference to interrupt source table
5:0	IRQ24_SEL	Interrupt source selector 6'h0~6'h3f: Please reference to interrupt source table

151A8028 **IRQ_SEL10** **IRQ Selection 10 Register** 2B2A2928

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			IRQ2B_SEL								IRQ2A_SEL					
Type			RW								RW					
Reset			1	0	1	0	1	1			1	0	1	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			IRQ29_SEL								IRQ28_SEL					
Type			RW								RW					
Reset			1	0	1	0	0	1			1	0	1	0	0	0

Bit(s)	Name	Description
29:24	IRQ2B_SEL	Interrupt source selector 6'h0~6'h3f: Please reference to interrupt source table
21:16	IRQ2A_SEL	Interrupt source selector 6'h0~6'h3f: Please reference to interrupt source table
13:8	IRQ29_SEL	Interrupt source selector 6'h0~6'h3f: Please reference to interrupt source table
5:0	IRQ28_SEL	Interrupt source selector 6'h0~6'h3f: Please reference to interrupt source table

Bit(s)	Name	Description
6'h0~6'h3f: Please reference to interrupt source table		

151A802C IRQ_SEL11 IRQ Selection 11 Register 2F2E2D2C

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	IRQ2F_SEL								IRQ2E_SEL							
Type	RW								RW							
Reset			1	0	1	1	1	1			1	0	1	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IRQ2D_SEL								IRQ2C_SEL							
Type	RW								RW							
Reset			1	0	1	1	0	1			1	0	1	1	0	0

Bit(s)	Name	Description
29:24	IRQ2F_SEL	Interrupt source selector 6'h0~6'h3f: Please reference to interrupt source table
21:16	IRQ2E_SEL	Interrupt source selector 6'h0~6'h3f: Please reference to interrupt source table
13:8	IRQ2D_SEL	Interrupt source selector 6'h0~6'h3f: Please reference to interrupt source table
5:0	IRQ2C_SEL	Interrupt source selector 6'h0~6'h3f: Please reference to interrupt source table

151A8030 IRQ_SEL12 IRQ Selection 12 Register 33323130

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	IRQ33_SEL								IRQ32_SEL							
Type	RW								RW							
Reset			1	1	0	0	1	1			1	1	0	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IRQ31_SEL								IRQ30_SEL							
Type	RW								RW							
Reset			1	1	0	0	0	1			1	1	0	0	0	0

Bit(s)	Name	Description
29:24	IRQ33_SEL	Interrupt source selector 6'h0~6'h3f: Please reference to interrupt source table
21:16	IRQ32_SEL	Interrupt source selector 6'h0~6'h3f: Please reference to interrupt source table
13:8	IRQ31_SEL	Interrupt source selector 6'h0~6'h3f: Please reference to interrupt source table
5:0	IRQ30_SEL	Interrupt source selector 6'h0~6'h3f: Please reference to interrupt source table

151A8034 **IRQ_SEL13** **IRQ Selection 13 Register** **37363534**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			IRQ37_SEL								IRQ36_SEL					
Type			RW								RW					
Reset			1	1	0	1	1	1			1	1	0	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			IRQ35_SEL								IRQ34_SEL					
Type			RW								RW					
Reset			1	1	0	1	0	1			1	1	0	1	0	0

Bit(s)	Name	Description
29:24	IRQ37_SEL	Interrupt source selector 6'h0~6'h3f: Please reference to interrupt source table
21:16	IRQ36_SEL	Interrupt source selector 6'h0~6'h3f: Please reference to interrupt source table
13:8	IRQ35_SEL	Interrupt source selector 6'h0~6'h3f: Please reference to interrupt source table
5:0	IRQ34_SEL	Interrupt source selector 6'h0~6'h3f: Please reference to interrupt source table

151A8038 **IRQ_SEL14** **IRQ Selection 14 Register** **3B3A3938**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			IRQ3B_SEL								IRQ3A_SEL					
Type			RW								RW					
Reset			1	1	1	0	1	1			1	1	1	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name			IRQ39_SEL								IRQ38_SEL					
Type			RW								RW					
Reset			1	1	1	0	0	1			1	1	1	0	0	0

Bit(s)	Name	Description
29:24	IRQ3B_SEL	Interrupt source selector 6'h0~6'h3f: Please reference to interrupt source table
21:16	IRQ3A_SEL	Interrupt source selector 6'h0~6'h3f: Please reference to interrupt source table
13:8	IRQ39_SEL	Interrupt source selector 6'h0~6'h3f: Please reference to interrupt source table
5:0	IRQ38_SEL	Interrupt source selector 6'h0~6'h3f: Please reference to interrupt source table

151A803C			IRQ_SEL15				IRQ Selection 15 Register								3F3E3D3C			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16		
Name			IRQ3F_SEL									IRQ3E_SEL						
Type			RW									RW						
Reset			1	1	1	1	1	1			1	1	1	1	1	0		
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
Name			IRQ3D_SEL									IRQ3C_SEL						
Type			RW									RW						
Reset			1	1	1	1	0	1			1	1	1	1	0	0		

Bit(s)	Name	Description
29:24	IRQ3F_SEL	Interrupt source selector 6'h0~6'h3f: Please reference to interrupt source table
21:16	IRQ3E_SEL	Interrupt source selector 6'h0~6'h3f: Please reference to interrupt source table
13:8	IRQ3D_SEL	Interrupt source selector 6'h0~6'h3f: Please reference to interrupt source table
5:0	IRQ3C_SEL	Interrupt source selector 6'h0~6'h3f: Please reference to interrupt source table

151A806C			FIQ_SEL								FIQ Selection Register						00000000		
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16			

Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											FIQ_SEL					
Type											RW					
Reset											0	0	0	0	0	0

Bit(s)	Name	Description
5:0	FIQ_SEL	FIQ source selector 6'h0~6'h3f: Please reference to interrupt source table

151A8070 IRQ_MASK IRQ Mask Register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	IRQ1F_MSK	IRQ1E_MSK	IRQ1D_MSK	IRQ1C_MSK	IRQ1B_MSK	IRQ1A_MSK	IRQ19_MSK	IRQ18_MSK	IRQ17_MSK	IRQ16_MSK	IRQ15_MSK	IRQ14_MSK	IRQ13_MSK	IRQ12_MSK	IRQ11_MSK	IRQ10_MSK
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IRQF_MSK	IRQE_MSK	IRQD_MSK	IRQC_MSK	IRQB_MSK	IRQA_MSK	IRQ9_MSK	IRQ8_MSK	IRQ7_MSK	IRQ6_MSK	IRQ5_MSK	IRQ4_MSK	IRQ3_MSK	IRQ2_MSK	IRQ1_MSK	IRQ0_MSK
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31	IRQ1F_MSK	Mask control for the associated interrupt source in the IRQ controller 0: Interrupt is enabled 1: Interrupt is disabled
30	IRQ1E_MSK	Mask control for the associated interrupt source in the IRQ controller 0: Interrupt is enabled 1: Interrupt is disabled
29	IRQ1D_MSK	Mask control for the associated interrupt source in the IRQ controller 0: Interrupt is enabled 1: Interrupt is disabled
28	IRQ1C_MSK	Mask control for the associated interrupt source in the IRQ controller 0: Interrupt is enabled 1: Interrupt is disabled

Bit(s)	Name	Description
27	IRQ1B_MSK	Mask control for the associated interrupt source in the IRQ controller 0: Interrupt is enabled 1: Interrupt is disabled
26	IRQ1A_MSK	Mask control for the associated interrupt source in the IRQ controller 0: Interrupt is enabled 1: Interrupt is disabled
25	IRQ19_MSK	Mask control for the associated interrupt source in the IRQ controller 0: Interrupt is enabled 1: Interrupt is disabled
24	IRQ18_MSK	Mask control for the associated interrupt source in the IRQ controller 0: Interrupt is enabled 1: Interrupt is disabled
23	IRQ17_MSK	Mask control for the associated interrupt source in the IRQ controller 0: Interrupt is enabled 1: Interrupt is disabled
22	IRQ16_MSK	Mask control for the associated interrupt source in the IRQ controller 0: Interrupt is enabled 1: Interrupt is disabled
21	IRQ15_MSK	Mask control for the associated interrupt source in the IRQ controller 0: Interrupt is enabled 1: Interrupt is disabled
20	IRQ14_MSK	Mask control for the associated interrupt source in the IRQ controller 0: Interrupt is enabled 1: Interrupt is disabled
19	IRQ13_MSK	Mask control for the associated interrupt source in the IRQ controller 0: Interrupt is enabled 1: Interrupt is disabled
18	IRQ12_MSK	Mask control for the associated interrupt source in the IRQ controller 0: Interrupt is enabled 1: Interrupt is disabled
17	IRQ11_MSK	Mask control for the associated interrupt source in the IRQ controller 0: Interrupt is enabled 1: Interrupt is disabled
16	IRQ10_MSK	Mask control for the associated interrupt source in the IRQ controller 0: Interrupt is enabled 1: Interrupt is disabled
15	IRQF_MSK	Mask control for the associated interrupt source in the IRQ controller 0: Interrupt is enabled 1: Interrupt is disabled
14	IRQE_MSK	Mask control for the associated interrupt source in the IRQ controller 0: Interrupt is enabled 1: Interrupt is disabled
13	IRQD_MSK	Mask control for the associated interrupt source in the IRQ controller 0: Interrupt is enabled 1: Interrupt is disabled
12	IRQC_MSK	Mask control for the associated interrupt source in the IRQ controller 0: Interrupt is enabled 1: Interrupt is disabled
11	IRQB_MSK	Mask control for the associated interrupt source in the IRQ controller 0: Interrupt is enabled 1: Interrupt is disabled
10	IRQA_MSK	Mask control for the associated interrupt source in the IRQ controller 0: Interrupt is enabled

Bit(s)	Name	Description
9	IRQ9_MSK	1: Interrupt is disabled Mask control for the associated interrupt source in the IRQ controller 0: Interrupt is enabled
8	IRQ8_MSK	1: Interrupt is disabled Mask control for the associated interrupt source in the IRQ controller 0: Interrupt is enabled
7	IRQ7_MSK	1: Interrupt is disabled Mask control for the associated interrupt source in the IRQ controller 0: Interrupt is enabled
6	IRQ6_MSK	1: Interrupt is disabled Mask control for the associated interrupt source in the IRQ controller 0: Interrupt is enabled
5	IRQ5_MSK	1: Interrupt is disabled Mask control for the associated interrupt source in the IRQ controller 0: Interrupt is enabled
4	IRQ4_MSK	1: Interrupt is disabled Mask control for the associated interrupt source in the IRQ controller 0: Interrupt is enabled
3	IRQ3_MSK	1: Interrupt is disabled Mask control for the associated interrupt source in the IRQ controller 0: Interrupt is enabled
2	IRQ2_MSK	1: Interrupt is disabled Mask control for the associated interrupt source in the IRQ controller 0: Interrupt is enabled
1	IRQ1_MSK	1: Interrupt is disabled Mask control for the associated interrupt source in the IRQ controller 0: Interrupt is enabled
0	IRQ0_MSK	1: Interrupt is disabled Mask control for the associated interrupt source in the IRQ controller 0: Interrupt is enabled

151A8074				IRQ_MASKM				IRQ Mask Register Middle								FFFFFFF			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16			
Name	IRQ3F_MSK	IRQ3E_MSK	IRQ3D_MSK	IRQ3C_MSK	IRQ3B_MSK	IRQ3A_MSK	IRQ39_MSK	IRQ38_MSK	IRQ37_MSK	IRQ36_MSK	IRQ35_MSK	IRQ34_MSK	IRQ33_MSK	IRQ32_MSK	IRQ31_MSK	IRQ30_MSK			
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW			
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1			
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0			
Name	IRQ2F_MSK	IRQ2E_MSK	IRQ2D_MSK	IRQ2C_MSK	IRQ2B_MSK	IRQ2A_MSK	IRQ29_MSK	IRQ28_MSK	IRQ27_MSK	IRQ26_MSK	IRQ25_MSK	IRQ24_MSK	IRQ23_MSK	IRQ22_MSK	IRQ21_MSK	IRQ20_MSK			
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW			
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1			

Bit(s)	Name	Description
31	IRQ3F_MSK	Mask control for the associated interrupt source in the IRQ controller 0: Interrupt is enabled 1: Interrupt is disabled
30	IRQ3E_MSK	Mask control for the associated interrupt source in the IRQ controller 0: Interrupt is enabled 1: Interrupt is disabled
29	IRQ3D_MSK	Mask control for the associated interrupt source in the IRQ controller 0: Interrupt is enabled 1: Interrupt is disabled
28	IRQ3C_MSK	Mask control for the associated interrupt source in the IRQ controller 0: Interrupt is enabled 1: Interrupt is disabled
27	IRQ3B_MSK	Mask control for the associated interrupt source in the IRQ controller 0: Interrupt is enabled 1: Interrupt is disabled
26	IRQ3A_MSK	Mask control for the associated interrupt source in the IRQ controller 0: Interrupt is enabled 1: Interrupt is disabled
25	IRQ39_MSK	Mask control for the associated interrupt source in the IRQ controller 0: Interrupt is enabled 1: Interrupt is disabled
24	IRQ38_MSK	Mask control for the associated interrupt source in the IRQ controller 0: Interrupt is enabled 1: Interrupt is disabled
23	IRQ37_MSK	Mask control for the associated interrupt source in the IRQ controller 0: Interrupt is enabled 1: Interrupt is disabled
22	IRQ36_MSK	Mask control for the associated interrupt source in the IRQ controller 0: Interrupt is enabled 1: Interrupt is disabled
21	IRQ35_MSK	Mask control for the associated interrupt source in the IRQ controller 0: Interrupt is enabled 1: Interrupt is disabled
20	IRQ34_MSK	Mask control for the associated interrupt source in the IRQ controller 0: Interrupt is enabled 1: Interrupt is disabled
19	IRQ33_MSK	Mask control for the associated interrupt source in the IRQ controller 0: Interrupt is enabled 1: Interrupt is disabled
18	IRQ32_MSK	Mask control for the associated interrupt source in the IRQ controller 0: Interrupt is enabled 1: Interrupt is disabled
17	IRQ31_MSK	Mask control for the associated interrupt source in the IRQ controller 0: Interrupt is enabled 1: Interrupt is disabled
16	IRQ30_MSK	Mask control for the associated interrupt source in the IRQ controller 0: Interrupt is enabled 1: Interrupt is disabled
15	IRQ2F_MSK	Mask control for the associated interrupt source in the IRQ controller 0: Interrupt is enabled 1: Interrupt is disabled
14	IRQ2E_MSK	Mask control for the associated interrupt source in the IRQ controller 0: Interrupt is enabled

Bit(s)	Name	Description
13	IRQ2D_MSK	1: Interrupt is disabled Mask control for the associated interrupt source in the IRQ controller 0: Interrupt is enabled
12	IRQ2C_MSK	1: Interrupt is disabled Mask control for the associated interrupt source in the IRQ controller 0: Interrupt is enabled
11	IRQ2B_MSK	1: Interrupt is disabled Mask control for the associated interrupt source in the IRQ controller 0: Interrupt is enabled
10	IRQ2A_MSK	1: Interrupt is disabled Mask control for the associated interrupt source in the IRQ controller 0: Interrupt is enabled
9	IRQ29_MSK	1: Interrupt is disabled Mask control for the associated interrupt source in the IRQ controller 0: Interrupt is enabled
8	IRQ28_MSK	1: Interrupt is disabled Mask control for the associated interrupt source in the IRQ controller 0: Interrupt is enabled
7	IRQ27_MSK	1: Interrupt is disabled Mask control for the associated interrupt source in the IRQ controller 0: Interrupt is enabled
6	IRQ26_MSK	1: Interrupt is disabled Mask control for the associated interrupt source in the IRQ controller 0: Interrupt is enabled
5	IRQ25_MSK	1: Interrupt is disabled Mask control for the associated interrupt source in the IRQ controller 0: Interrupt is enabled
4	IRQ24_MSK	1: Interrupt is disabled Mask control for the associated interrupt source in the IRQ controller 0: Interrupt is enabled
3	IRQ23_MSK	1: Interrupt is disabled Mask control for the associated interrupt source in the IRQ controller 0: Interrupt is enabled
2	IRQ22_MSK	1: Interrupt is disabled Mask control for the associated interrupt source in the IRQ controller 0: Interrupt is enabled
1	IRQ21_MSK	1: Interrupt is disabled Mask control for the associated interrupt source in the IRQ controller 0: Interrupt is enabled
0	IRQ20_MSK	1: Interrupt is disabled Mask control for the associated interrupt source in the IRQ controller 0: Interrupt is enabled

151A8080	IRQ_MASK_CLR				IRQ Mask Clear Register												00000000	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16		
Name	IRQ1F_MCLR	IRQ1E_MCLR	IRQ1D_MCLR	IRQ1C_MCLR	IRQ1B_MCLR	IRQ1A_MCLR	IRQ19_MCLR	IRQ18_MCLR	IRQ17_MCLR	IRQ16_MCLR	IRQ15_MCLR	IRQ14_MCLR	IRQ13_MCLR	IRQ12_MCLR	IRQ11_MCLR	IRQ10_MCLR		
Type	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO		

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IRQF_MCLR	IRQE_MCLR	IRQD_MCLR	IRQC_MCLR	IRQB_MCLR	IRQA_MCLR	IRQ9_MCLR	IRQ8_MCLR	IRQ7_MCLR	IRQ6_MCLR	IRQ5_MCLR	IRQ4_MCLR	IRQ3_MCLR	IRQ2_MCLR	IRQ1_MCLR	IRQ0_MCLR
Type	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	IRQ1F_MCLR	Clear corresponding bits in IRQ Mask Register. 0: No effect 1: Disable the corresponding MASK bit
30	IRQ1E_MCLR	Clear corresponding bits in IRQ Mask Register. 0: No effect 1: Disable the corresponding MASK bit
29	IRQ1D_MCLR	Clear corresponding bits in IRQ Mask Register. 0: No effect 1: Disable the corresponding MASK bit
28	IRQ1C_MCLR	Clear corresponding bits in IRQ Mask Register. 0: No effect 1: Disable the corresponding MASK bit
27	IRQ1B_MCLR	Clear corresponding bits in IRQ Mask Register. 0: No effect 1: Disable the corresponding MASK bit
26	IRQ1A_MCLR	Clear corresponding bits in IRQ Mask Register. 0: No effect 1: Disable the corresponding MASK bit
25	IRQ19_MCLR	Clear corresponding bits in IRQ Mask Register. 0: No effect 1: Disable the corresponding MASK bit
24	IRQ18_MCLR	Clear corresponding bits in IRQ Mask Register. 0: No effect 1: Disable the corresponding MASK bit
23	IRQ17_MCLR	Clear corresponding bits in IRQ Mask Register. 0: No effect 1: Disable the corresponding MASK bit
22	IRQ16_MCLR	Clear corresponding bits in IRQ Mask Register. 0: No effect 1: Disable the corresponding MASK bit
21	IRQ15_MCLR	Clear corresponding bits in IRQ Mask Register. 0: No effect 1: Disable the corresponding MASK bit
20	IRQ14_MCLR	Clear corresponding bits in IRQ Mask Register. 0: No effect 1: Disable the corresponding MASK bit
19	IRQ13_MCLR	Clear corresponding bits in IRQ Mask Register. 0: No effect 1: Disable the corresponding MASK bit
18	IRQ12_MCLR	Clear corresponding bits in IRQ Mask Register. 0: No effect 1: Disable the corresponding MASK bit

Bit(s)	Name	Description
17	IRQ11_MCLR	Clear corresponding bits in IRQ Mask Register. 0: No effect 1: Disable the corresponding MASK bit
16	IRQ10_MCLR	Clear corresponding bits in IRQ Mask Register. 0: No effect 1: Disable the corresponding MASK bit
15	IRQF_MCLR	Clear corresponding bits in IRQ Mask Register. 0: No effect 1: Disable the corresponding MASK bit
14	IRQE_MCLR	Clear corresponding bits in IRQ Mask Register. 0: No effect 1: Disable the corresponding MASK bit
13	IRQD_MCLR	Clear corresponding bits in IRQ Mask Register. 0: No effect 1: Disable the corresponding MASK bit
12	IRQC_MCLR	Clear corresponding bits in IRQ Mask Register. 0: No effect 1: Disable the corresponding MASK bit
11	IRQB_MCLR	Clear corresponding bits in IRQ Mask Register. 0: No effect 1: Disable the corresponding MASK bit
10	IRQA_MCLR	Clear corresponding bits in IRQ Mask Register. 0: No effect 1: Disable the corresponding MASK bit
9	IRQ9_MCLR	Clear corresponding bits in IRQ Mask Register. 0: No effect 1: Disable the corresponding MASK bit
8	IRQ8_MCLR	Clear corresponding bits in IRQ Mask Register. 0: No effect 1: Disable the corresponding MASK bit
7	IRQ7_MCLR	Clear corresponding bits in IRQ Mask Register. 0: No effect 1: Disable the corresponding MASK bit
6	IRQ6_MCLR	Clear corresponding bits in IRQ Mask Register. 0: No effect 1: Disable the corresponding MASK bit
5	IRQ5_MCLR	Clear corresponding bits in IRQ Mask Register. 0: No effect 1: Disable the corresponding MASK bit
4	IRQ4_MCLR	Clear corresponding bits in IRQ Mask Register. 0: No effect 1: Disable the corresponding MASK bit
3	IRQ3_MCLR	Clear corresponding bits in IRQ Mask Register. 0: No effect 1: Disable the corresponding MASK bit
2	IRQ2_MCLR	Clear corresponding bits in IRQ Mask Register. 0: No effect 1: Disable the corresponding MASK bit
1	IRQ1_MCLR	Clear corresponding bits in IRQ Mask Register. 0: No effect 1: Disable the corresponding MASK bit
0	IRQ0_MCLR	Clear corresponding bits in IRQ Mask Register. 0: No effect 1: Disable the corresponding MASK bit

Bit(s)	Name	Description
		1: Disable the corresponding MASK bit

151A8084 IRQ_MASK_CLRM IRQ Mask Clear Register Middle 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	IRQ3F_MCLR	IRQ3E_MCLR	IRQ3D_MCLR	IRQ3C_MCLR	IRQ3B_MCLR	IRQ3A_MCLR	IRQ39_MCLR	IRQ38_MCLR	IRQ37_MCLR	IRQ36_MCLR	IRQ35_MCLR	IRQ34_MCLR	IRQ33_MCLR	IRQ32_MCLR	IRQ31_MCLR	IRQ30_MCLR
Type	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IRQ2F_MCLR	IRQ2E_MCLR	IRQ2D_MCLR	IRQ2C_MCLR	IRQ2B_MCLR	IRQ2A_MCLR	IRQ29_MCLR	IRQ28_MCLR	IRQ27_MCLR	IRQ26_MCLR	IRQ25_MCLR	IRQ24_MCLR	IRQ23_MCLR	IRQ22_MCLR	IRQ21_MCLR	IRQ20_MCLR
Type	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	IRQ3F_MCLR	Clear corresponding bits in IRQ Mask Register. 0: No effect 1: Disable the corresponding MASK bit
30	IRQ3E_MCLR	Clear corresponding bits in IRQ Mask Register. 0: No effect 1: Disable the corresponding MASK bit
29	IRQ3D_MCLR	Clear corresponding bits in IRQ Mask Register. 0: No effect 1: Disable the corresponding MASK bit
28	IRQ3C_MCLR	Clear corresponding bits in IRQ Mask Register. 0: No effect 1: Disable the corresponding MASK bit
27	IRQ3B_MCLR	Clear corresponding bits in IRQ Mask Register. 0: No effect 1: Disable the corresponding MASK bit
26	IRQ3A_MCLR	Clear corresponding bits in IRQ Mask Register. 0: No effect 1: Disable the corresponding MASK bit
25	IRQ39_MCLR	Clear corresponding bits in IRQ Mask Register. 0: No effect 1: Disable the corresponding MASK bit
24	IRQ38_MCLR	Clear corresponding bits in IRQ Mask Register. 0: No effect 1: Disable the corresponding MASK bit
23	IRQ37_MCLR	Clear corresponding bits in IRQ Mask Register. 0: No effect 1: Disable the corresponding MASK bit
22	IRQ36_MCLR	Clear corresponding bits in IRQ Mask Register. 0: No effect

Bit(s)	Name	Description
21	IRQ35_MCLR	1: Disable the corresponding MASK bit Clear corresponding bits in IRQ Mask Register. 0: No effect
20	IRQ34_MCLR	1: Disable the corresponding MASK bit Clear corresponding bits in IRQ Mask Register. 0: No effect
19	IRQ33_MCLR	1: Disable the corresponding MASK bit Clear corresponding bits in IRQ Mask Register. 0: No effect
18	IRQ32_MCLR	1: Disable the corresponding MASK bit Clear corresponding bits in IRQ Mask Register. 0: No effect
17	IRQ31_MCLR	1: Disable the corresponding MASK bit Clear corresponding bits in IRQ Mask Register. 0: No effect
16	IRQ30_MCLR	1: Disable the corresponding MASK bit Clear corresponding bits in IRQ Mask Register. 0: No effect
15	IRQ2F_MCLR	1: Disable the corresponding MASK bit Clear corresponding bits in IRQ Mask Register. 0: No effect
14	IRQ2E_MCLR	1: Disable the corresponding MASK bit Clear corresponding bits in IRQ Mask Register. 0: No effect
13	IRQ2D_MCLR	1: Disable the corresponding MASK bit Clear corresponding bits in IRQ Mask Register. 0: No effect
12	IRQ2C_MCLR	1: Disable the corresponding MASK bit Clear corresponding bits in IRQ Mask Register. 0: No effect
11	IRQ2B_MCLR	1: Disable the corresponding MASK bit Clear corresponding bits in IRQ Mask Register. 0: No effect
10	IRQ2A_MCLR	1: Disable the corresponding MASK bit Clear corresponding bits in IRQ Mask Register. 0: No effect
9	IRQ29_MCLR	1: Disable the corresponding MASK bit Clear corresponding bits in IRQ Mask Register. 0: No effect
8	IRQ28_MCLR	1: Disable the corresponding MASK bit Clear corresponding bits in IRQ Mask Register. 0: No effect
7	IRQ27_MCLR	1: Disable the corresponding MASK bit Clear corresponding bits in IRQ Mask Register. 0: No effect
6	IRQ26_MCLR	1: Disable the corresponding MASK bit Clear corresponding bits in IRQ Mask Register. 0: No effect
5	IRQ25_MCLR	1: Disable the corresponding MASK bit Clear corresponding bits in IRQ Mask Register. 0: No effect
4	IRQ24_MCLR	1: Disable the corresponding MASK bit Clear corresponding bits in IRQ Mask Register.

Bit(s)	Name	Description
3	IRQ23_MCLR	0: No effect 1: Disable the corresponding MASK bit Clear corresponding bits in IRQ Mask Register.
2	IRQ22_MCLR	0: No effect 1: Disable the corresponding MASK bit Clear corresponding bits in IRQ Mask Register.
1	IRQ21_MCLR	0: No effect 1: Disable the corresponding MASK bit Clear corresponding bits in IRQ Mask Register.
0	IRQ20_MCLR	0: No effect 1: Disable the corresponding MASK bit Clear corresponding bits in IRQ Mask Register.

151A8090 IRQ_MASK_SET IRQ Mask Set Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	IRQ1F_MSET	IRQ1E_MSET	IRQ1D_MSET	IRQ1C_MSET	IRQ1B_MSET	IRQ1A_MSET	IRQ19_MSET	IRQ18_MSET	IRQ17_MSET	IRQ16_MSET	IRQ15_MSET	IRQ14_MSET	IRQ13_MSET	IRQ12_MSET	IRQ11_MSET	IRQ10_MSET
Type	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IRQF_MSET	IRQE_MSET	IRQD_MSET	IRQC_MSET	IRQB_MSET	IRQA_MSET	IRQ9_MSET	IRQ8_MSET	IRQ7_MSET	IRQ6_MSET	IRQ5_MSET	IRQ4_MSET	IRQ3_MSET	IRQ2_MSET	IRQ1_MSET	IRQ0_MSET
Type	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	IRQ1F_MSET	Set corresponding bits in IRQ Mask Register. 0: No effect 1: Enable corresponding MASK bit
30	IRQ1E_MSET	Set corresponding bits in IRQ Mask Register. 0: No effect 1: Enable corresponding MASK bit
29	IRQ1D_MSET	Set corresponding bits in IRQ Mask Register. 0: No effect 1: Enable corresponding MASK bit
28	IRQ1C_MSET	Set corresponding bits in IRQ Mask Register. 0: No effect 1: Enable corresponding MASK bit
27	IRQ1B_MSET	Set corresponding bits in IRQ Mask Register. 0: No effect 1: Enable corresponding MASK bit
26	IRQ1A_MSET	Set corresponding bits in IRQ Mask Register. 0: No effect 1: Enable corresponding MASK bit

Bit(s)	Name	Description
25	IRQ19_MSET	0: No effect 1: Enable corresponding MASK bit Set corresponding bits in IRQ Mask Register.
24	IRQ18_MSET	0: No effect 1: Enable corresponding MASK bit Set corresponding bits in IRQ Mask Register.
23	IRQ17_MSET	0: No effect 1: Enable corresponding MASK bit Set corresponding bits in IRQ Mask Register.
22	IRQ16_MSET	0: No effect 1: Enable corresponding MASK bit Set corresponding bits in IRQ Mask Register.
21	IRQ15_MSET	0: No effect 1: Enable corresponding MASK bit Set corresponding bits in IRQ Mask Register.
20	IRQ14_MSET	0: No effect 1: Enable corresponding MASK bit Set corresponding bits in IRQ Mask Register.
19	IRQ13_MSET	0: No effect 1: Enable corresponding MASK bit Set corresponding bits in IRQ Mask Register.
18	IRQ12_MSET	0: No effect 1: Enable corresponding MASK bit Set corresponding bits in IRQ Mask Register.
17	IRQ11_MSET	0: No effect 1: Enable corresponding MASK bit Set corresponding bits in IRQ Mask Register.
16	IRQ10_MSET	0: No effect 1: Enable corresponding MASK bit Set corresponding bits in IRQ Mask Register.
15	IRQF_MSET	0: No effect 1: Enable corresponding MASK bit Set corresponding bits in IRQ Mask Register.
14	IRQE_MSET	0: No effect 1: Enable corresponding MASK bit Set corresponding bits in IRQ Mask Register.
13	IRQD_MSET	0: No effect 1: Enable corresponding MASK bit Set corresponding bits in IRQ Mask Register.
12	IRQC_MSET	0: No effect 1: Enable corresponding MASK bit Set corresponding bits in IRQ Mask Register.
11	IRQB_MSET	0: No effect 1: Enable corresponding MASK bit Set corresponding bits in IRQ Mask Register.
10	IRQA_MSET	0: No effect 1: Enable corresponding MASK bit Set corresponding bits in IRQ Mask Register.
9	IRQ9_MSET	0: No effect 1: Enable corresponding MASK bit Set corresponding bits in IRQ Mask Register.

Bit(s)	Name	Description
8	IRQ8_MSET	Set corresponding bits in IRQ Mask Register. 0: No effect 1: Enable corresponding MASK bit
7	IRQ7_MSET	Set corresponding bits in IRQ Mask Register. 0: No effect 1: Enable corresponding MASK bit
6	IRQ6_MSET	Set corresponding bits in IRQ Mask Register. 0: No effect 1: Enable corresponding MASK bit
5	IRQ5_MSET	Set corresponding bits in IRQ Mask Register. 0: No effect 1: Enable corresponding MASK bit
4	IRQ4_MSET	Set corresponding bits in IRQ Mask Register. 0: No effect 1: Enable corresponding MASK bit
3	IRQ3_MSET	Set corresponding bits in IRQ Mask Register. 0: No effect 1: Enable corresponding MASK bit
2	IRQ2_MSET	Set corresponding bits in IRQ Mask Register. 0: No effect 1: Enable corresponding MASK bit
1	IRQ1_MSET	Set corresponding bits in IRQ Mask Register. 0: No effect 1: Enable corresponding MASK bit
0	IRQ0_MSET	Set corresponding bits in IRQ Mask Register. 0: No effect 1: Enable corresponding MASK bit

151A8094 IRQ_MASK_SETM IRQ Mask Set Register Middle 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	IRQ3F_MSET	IRQ3E_MSET	IRQ3D_MSET	IRQ3C_MSET	IRQ3B_MSET	IRQ3A_MSET	IRQ39_MSET	IRQ38_MSET	IRQ37_MSET	IRQ36_MSET	IRQ35_MSET	IRQ34_MSET	IRQ33_MSET	IRQ32_MSET	IRQ31_MSET	IRQ30_MSET
Type	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IRQ2F_MSET	IRQ2E_MSET	IRQ2D_MSET	IRQ2C_MSET	IRQ2B_MSET	IRQ2A_MSET	IRQ29_MSET	IRQ28_MSET	IRQ27_MSET	IRQ26_MSET	IRQ25_MSET	IRQ24_MSET	IRQ23_MSET	IRQ22_MSET	IRQ21_MSET	IRQ20_MSET
Type	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	IRQ3F_MSET	Set corresponding bits in IRQ Mask Register. 0: No effect 1: Enable corresponding MASK bit

Bit(s)	Name	Description
30	IRQ3E_MSET	Set corresponding bits in IRQ Mask Register. 0: No effect 1: Enable corresponding MASK bit
29	IRQ3D_MSET	Set corresponding bits in IRQ Mask Register. 0: No effect 1: Enable corresponding MASK bit
28	IRQ3C_MSET	Set corresponding bits in IRQ Mask Register. 0: No effect 1: Enable corresponding MASK bit
27	IRQ3B_MSET	Set corresponding bits in IRQ Mask Register. 0: No effect 1: Enable corresponding MASK bit
26	IRQ3A_MSET	Set corresponding bits in IRQ Mask Register. 0: No effect 1: Enable corresponding MASK bit
25	IRQ39_MSET	Set corresponding bits in IRQ Mask Register. 0: No effect 1: Enable corresponding MASK bit
24	IRQ38_MSET	Set corresponding bits in IRQ Mask Register. 0: No effect 1: Enable corresponding MASK bit
23	IRQ37_MSET	Set corresponding bits in IRQ Mask Register. 0: No effect 1: Enable corresponding MASK bit
22	IRQ36_MSET	Set corresponding bits in IRQ Mask Register. 0: No effect 1: Enable corresponding MASK bit
21	IRQ35_MSET	Set corresponding bits in IRQ Mask Register. 0: No effect 1: Enable corresponding MASK bit
20	IRQ34_MSET	Set corresponding bits in IRQ Mask Register. 0: No effect 1: Enable corresponding MASK bit
19	IRQ33_MSET	Set corresponding bits in IRQ Mask Register. 0: No effect 1: Enable corresponding MASK bit
18	IRQ32_MSET	Set corresponding bits in IRQ Mask Register. 0: No effect 1: Enable corresponding MASK bit
17	IRQ31_MSET	Set corresponding bits in IRQ Mask Register. 0: No effect 1: Enable corresponding MASK bit
16	IRQ30_MSET	Set corresponding bits in IRQ Mask Register. 0: No effect 1: Enable corresponding MASK bit
15	IRQ2F_MSET	Set corresponding bits in IRQ Mask Register. 0: No effect 1: Enable corresponding MASK bit
14	IRQ2E_MSET	Set corresponding bits in IRQ Mask Register. 0: No effect 1: Enable corresponding MASK bit
13	IRQ2D_MSET	Set corresponding bits in IRQ Mask Register. 0: No effect 1: Enable corresponding MASK bit

Bit(s)	Name	Description
12	IRQ2C_MSET	1: Enable corresponding MASK bit Set corresponding bits in IRQ Mask Register. 0: No effect
11	IRQ2B_MSET	1: Enable corresponding MASK bit Set corresponding bits in IRQ Mask Register. 0: No effect
10	IRQ2A_MSET	1: Enable corresponding MASK bit Set corresponding bits in IRQ Mask Register. 0: No effect
9	IRQ29_MSET	1: Enable corresponding MASK bit Set corresponding bits in IRQ Mask Register. 0: No effect
8	IRQ28_MSET	1: Enable corresponding MASK bit Set corresponding bits in IRQ Mask Register. 0: No effect
7	IRQ27_MSET	1: Enable corresponding MASK bit Set corresponding bits in IRQ Mask Register. 0: No effect
6	IRQ26_MSET	1: Enable corresponding MASK bit Set corresponding bits in IRQ Mask Register. 0: No effect
5	IRQ25_MSET	1: Enable corresponding MASK bit Set corresponding bits in IRQ Mask Register. 0: No effect
4	IRQ24_MSET	1: Enable corresponding MASK bit Set corresponding bits in IRQ Mask Register. 0: No effect
3	IRQ23_MSET	1: Enable corresponding MASK bit Set corresponding bits in IRQ Mask Register. 0: No effect
2	IRQ22_MSET	1: Enable corresponding MASK bit Set corresponding bits in IRQ Mask Register. 0: No effect
1	IRQ21_MSET	1: Enable corresponding MASK bit Set corresponding bits in IRQ Mask Register. 0: No effect
0	IRQ20_MSET	1: Enable corresponding MASK bit Set corresponding bits in IRQ Mask Register. 0: No effect 1: Enable corresponding MASK bit

151A80A0	IRQ_EOI			IRQ End of Interrupt Register												00000000	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
Name	IRQ1F_EOI	IRQ1E_EOI	IRQ1D_EOI	IRQ1C_EOI	IRQ1B_EOI	IRQ1A_EOI	IRQ19_EOI	IRQ18_EOI	IRQ17_EOI	IRQ16_EOI	IRQ15_EOI	IRQ14_EOI	IRQ13_EOI	IRQ12_EOI	IRQ11_EOI	IRQ10_EOI	
Type	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IRQF_EOI	IRQE_EOI	IRQD_EOI	IRQC_EOI	IRQB_EOI	IRQA_EOI	IRQ9_EOI	IRQ8_EOI	IRQ7_EOI	IRQ6_EOI	IRQ5_EOI	IRQ4_EOI	IRQ3_EOI	IRQ2_EOI	IRQ1_EOI	IRQ0_EOI
Type	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	IRQ1F_EOI	End of Interrupt command for the associated interrupt line. 0: No service is currently in progress or pending 1: Interrupt request is in-service
30	IRQ1E_EOI	End of Interrupt command for the associated interrupt line. 0: No service is currently in progress or pending 1: Interrupt request is in-service
29	IRQ1D_EOI	End of Interrupt command for the associated interrupt line. 0: No service is currently in progress or pending 1: Interrupt request is in-service
28	IRQ1C_EOI	End of Interrupt command for the associated interrupt line. 0: No service is currently in progress or pending 1: Interrupt request is in-service
27	IRQ1B_EOI	End of Interrupt command for the associated interrupt line. 0: No service is currently in progress or pending 1: Interrupt request is in-service
26	IRQ1A_EOI	End of Interrupt command for the associated interrupt line. 0: No service is currently in progress or pending 1: Interrupt request is in-service
25	IRQ19_EOI	End of Interrupt command for the associated interrupt line. 0: No service is currently in progress or pending 1: Interrupt request is in-service
24	IRQ18_EOI	End of Interrupt command for the associated interrupt line. 0: No service is currently in progress or pending 1: Interrupt request is in-service
23	IRQ17_EOI	End of Interrupt command for the associated interrupt line. 0: No service is currently in progress or pending 1: Interrupt request is in-service
22	IRQ16_EOI	End of Interrupt command for the associated interrupt line. 0: No service is currently in progress or pending 1: Interrupt request is in-service
21	IRQ15_EOI	End of Interrupt command for the associated interrupt line. 0: No service is currently in progress or pending 1: Interrupt request is in-service
20	IRQ14_EOI	End of Interrupt command for the associated interrupt line. 0: No service is currently in progress or pending 1: Interrupt request is in-service
19	IRQ13_EOI	End of Interrupt command for the associated interrupt line. 0: No service is currently in progress or pending 1: Interrupt request is in-service
18	IRQ12_EOI	End of Interrupt command for the associated interrupt line. 0: No service is currently in progress or pending 1: Interrupt request is in-service
17	IRQ11_EOI	End of Interrupt command for the associated interrupt line. 0: No service is currently in progress or pending

Bit(s)	Name	Description
16	IRQ10_EOI	1: Interrupt request is in-service End of Interrupt command for the associated interrupt line. 0: No service is currently in progress or pending
15	IRQF_EOI	1: Interrupt request is in-service End of Interrupt command for the associated interrupt line. 0: No service is currently in progress or pending
14	IRQE_EOI	1: Interrupt request is in-service End of Interrupt command for the associated interrupt line. 0: No service is currently in progress or pending
13	IRQD_EOI	1: Interrupt request is in-service End of Interrupt command for the associated interrupt line. 0: No service is currently in progress or pending
12	IRQC_EOI	1: Interrupt request is in-service End of Interrupt command for the associated interrupt line. 0: No service is currently in progress or pending
11	IRQB_EOI	1: Interrupt request is in-service End of Interrupt command for the associated interrupt line. 0: No service is currently in progress or pending
10	IRQA_EOI	1: Interrupt request is in-service End of Interrupt command for the associated interrupt line. 0: No service is currently in progress or pending
9	IRQ9_EOI	1: Interrupt request is in-service End of Interrupt command for the associated interrupt line. 0: No service is currently in progress or pending
8	IRQ8_EOI	1: Interrupt request is in-service End of Interrupt command for the associated interrupt line. 0: No service is currently in progress or pending
7	IRQ7_EOI	1: Interrupt request is in-service End of Interrupt command for the associated interrupt line. 0: No service is currently in progress or pending
6	IRQ6_EOI	1: Interrupt request is in-service End of Interrupt command for the associated interrupt line. 0: No service is currently in progress or pending
5	IRQ5_EOI	1: Interrupt request is in-service End of Interrupt command for the associated interrupt line. 0: No service is currently in progress or pending
4	IRQ4_EOI	1: Interrupt request is in-service End of Interrupt command for the associated interrupt line. 0: No service is currently in progress or pending
3	IRQ3_EOI	1: Interrupt request is in-service End of Interrupt command for the associated interrupt line. 0: No service is currently in progress or pending
2	IRQ2_EOI	1: Interrupt request is in-service End of Interrupt command for the associated interrupt line. 0: No service is currently in progress or pending
1	IRQ1_EOI	1: Interrupt request is in-service End of Interrupt command for the associated interrupt line. 0: No service is currently in progress or pending
0	IRQ0_EOI	1: Interrupt request is in-service End of Interrupt command for the associated interrupt line. 0: No service is currently in progress or pending

151A80A4 IRQ_EOIM IRQ End of Interrupt Register Middle 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	IRQ3F_EOI	IRQ3E_EOI	IRQ3D_EOI	IRQ3C_EOI	IRQ3B_EOI	IRQ3A_EOI	IRQ39_EOI	IRQ38_EOI	IRQ37_EOI	IRQ36_EOI	IRQ35_EOI	IRQ34_EOI	IRQ33_EOI	IRQ32_EOI	IRQ31_EOI	IRQ30_EOI
Type	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IRQ2F_EOI	IRQ2E_EOI	IRQ2D_EOI	IRQ2C_EOI	IRQ2B_EOI	IRQ2A_EOI	IRQ29_EOI	IRQ28_EOI	IRQ27_EOI	IRQ26_EOI	IRQ25_EOI	IRQ24_EOI	IRQ23_EOI	IRQ22_EOI	IRQ21_EOI	IRQ20_EOI
Type	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	IRQ3F_EOI	End of Interrupt command for the associated interrupt line. 0: No service is currently in progress or pending 1: Interrupt request is in-service
30	IRQ3E_EOI	End of Interrupt command for the associated interrupt line. 0: No service is currently in progress or pending 1: Interrupt request is in-service
29	IRQ3D_EOI	End of Interrupt command for the associated interrupt line. 0: No service is currently in progress or pending 1: Interrupt request is in-service
28	IRQ3C_EOI	End of Interrupt command for the associated interrupt line. 0: No service is currently in progress or pending 1: Interrupt request is in-service
27	IRQ3B_EOI	End of Interrupt command for the associated interrupt line. 0: No service is currently in progress or pending 1: Interrupt request is in-service
26	IRQ3A_EOI	End of Interrupt command for the associated interrupt line. 0: No service is currently in progress or pending 1: Interrupt request is in-service
25	IRQ39_EOI	End of Interrupt command for the associated interrupt line. 0: No service is currently in progress or pending 1: Interrupt request is in-service
24	IRQ38_EOI	End of Interrupt command for the associated interrupt line. 0: No service is currently in progress or pending 1: Interrupt request is in-service
23	IRQ37_EOI	End of Interrupt command for the associated interrupt line. 0: No service is currently in progress or pending 1: Interrupt request is in-service
22	IRQ36_EOI	End of Interrupt command for the associated interrupt line. 0: No service is currently in progress or pending 1: Interrupt request is in-service
21	IRQ35_EOI	End of Interrupt command for the associated interrupt line. 0: No service is currently in progress or pending 1: Interrupt request is in-service

Bit(s)	Name	Description
20	IRQ34_EOI	End of Interrupt command for the associated interrupt line. 0: No service is currently in progress or pending 1: Interrupt request is in-service
19	IRQ33_EOI	End of Interrupt command for the associated interrupt line. 0: No service is currently in progress or pending 1: Interrupt request is in-service
18	IRQ32_EOI	End of Interrupt command for the associated interrupt line. 0: No service is currently in progress or pending 1: Interrupt request is in-service
17	IRQ31_EOI	End of Interrupt command for the associated interrupt line. 0: No service is currently in progress or pending 1: Interrupt request is in-service
16	IRQ30_EOI	End of Interrupt command for the associated interrupt line. 0: No service is currently in progress or pending 1: Interrupt request is in-service
15	IRQ2F_EOI	End of Interrupt command for the associated interrupt line. 0: No service is currently in progress or pending 1: Interrupt request is in-service
14	IRQ2E_EOI	End of Interrupt command for the associated interrupt line. 0: No service is currently in progress or pending 1: Interrupt request is in-service
13	IRQ2D_EOI	End of Interrupt command for the associated interrupt line. 0: No service is currently in progress or pending 1: Interrupt request is in-service
12	IRQ2C_EOI	End of Interrupt command for the associated interrupt line. 0: No service is currently in progress or pending 1: Interrupt request is in-service
11	IRQ2B_EOI	End of Interrupt command for the associated interrupt line. 0: No service is currently in progress or pending 1: Interrupt request is in-service
10	IRQ2A_EOI	End of Interrupt command for the associated interrupt line. 0: No service is currently in progress or pending 1: Interrupt request is in-service
9	IRQ29_EOI	End of Interrupt command for the associated interrupt line. 0: No service is currently in progress or pending 1: Interrupt request is in-service
8	IRQ28_EOI	End of Interrupt command for the associated interrupt line. 0: No service is currently in progress or pending 1: Interrupt request is in-service
7	IRQ27_EOI	End of Interrupt command for the associated interrupt line. 0: No service is currently in progress or pending 1: Interrupt request is in-service
6	IRQ26_EOI	End of Interrupt command for the associated interrupt line. 0: No service is currently in progress or pending 1: Interrupt request is in-service
5	IRQ25_EOI	End of Interrupt command for the associated interrupt line. 0: No service is currently in progress or pending 1: Interrupt request is in-service
4	IRQ24_EOI	End of Interrupt command for the associated interrupt line. 0: No service is currently in progress or pending 1: Interrupt request is in-service
3	IRQ23_EOI	End of Interrupt command for the associated interrupt line. 0: No service is currently in progress or pending

Bit(s)	Name	Description
2	IRQ22_EOI	1: Interrupt request is in-service End of Interrupt command for the associated interrupt line. 0: No service is currently in progress or pending
1	IRQ21_EOI	1: Interrupt request is in-service End of Interrupt command for the associated interrupt line. 0: No service is currently in progress or pending
0	IRQ20_EOI	1: Interrupt request is in-service End of Interrupt command for the associated interrupt line. 0: No service is currently in progress or pending 1: Interrupt request is in-service

151A80B0 IRQ_SENS IRQ Sensitive Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	IRQ1F_SENS	IRQ1E_SENS	IRQ1D_SENS	IRQ1C_SENS	IRQ1B_SENS	IRQ1A_SENS	IRQ19_SENS	IRQ18_SENS	IRQ17_SENS	IRQ16_SENS	IRQ15_SENS	IRQ14_SENS	IRQ13_SENS	IRQ12_SENS	IRQ11_SENS	IRQ10_SENS
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IRQF_SENS	IRQE_SENS	IRQD_SENS	IRQC_SENS	IRQB_SENS	IRQA_SENS	IRQ9_SENS	IRQ8_SENS	IRQ7_SENS	IRQ6_SENS	IRQ5_SENS	IRQ4_SENS	IRQ3_SENS	IRQ2_SENS	IRQ1_SENS	IRQ0_SENS
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	IRQ1F_SENS	Sensitivity type of the associated Interrupt Source 0: Edge sensitivity with active LOW 1: Level sensitivity with active LOW
30	IRQ1E_SENS	Sensitivity type of the associated Interrupt Source 0: Edge sensitivity with active LOW 1: Level sensitivity with active LOW
29	IRQ1D_SENS	Sensitivity type of the associated Interrupt Source 0: Edge sensitivity with active LOW 1: Level sensitivity with active LOW
28	IRQ1C_SENS	Sensitivity type of the associated Interrupt Source 0: Edge sensitivity with active LOW 1: Level sensitivity with active LOW
27	IRQ1B_SENS	Sensitivity type of the associated Interrupt Source 0: Edge sensitivity with active LOW 1: Level sensitivity with active LOW
26	IRQ1A_SENS	Sensitivity type of the associated Interrupt Source 0: Edge sensitivity with active LOW 1: Level sensitivity with active LOW
25	IRQ19_SENS	Sensitivity type of the associated Interrupt Source 0: Edge sensitivity with active LOW

Bit(s)	Name	Description
24	IRQ18_SENS	1: Level sensitivity with active LOW Sensitivity type of the associated Interrupt Source 0: Edge sensitivity with active LOW
23	IRQ17_SENS	1: Level sensitivity with active LOW Sensitivity type of the associated Interrupt Source 0: Edge sensitivity with active LOW
22	IRQ16_SENS	1: Level sensitivity with active LOW Sensitivity type of the associated Interrupt Source 0: Edge sensitivity with active LOW
21	IRQ15_SENS	1: Level sensitivity with active LOW Sensitivity type of the associated Interrupt Source 0: Edge sensitivity with active LOW
20	IRQ14_SENS	1: Level sensitivity with active LOW Sensitivity type of the associated Interrupt Source 0: Edge sensitivity with active LOW
19	IRQ13_SENS	1: Level sensitivity with active LOW Sensitivity type of the associated Interrupt Source 0: Edge sensitivity with active LOW
18	IRQ12_SENS	1: Level sensitivity with active LOW Sensitivity type of the associated Interrupt Source 0: Edge sensitivity with active LOW
17	IRQ11_SENS	1: Level sensitivity with active LOW Sensitivity type of the associated Interrupt Source 0: Edge sensitivity with active LOW
16	IRQ10_SENS	1: Level sensitivity with active LOW Sensitivity type of the associated Interrupt Source 0: Edge sensitivity with active LOW
15	IRQF_SENS	1: Level sensitivity with active LOW Sensitivity type of the associated Interrupt Source 0: Edge sensitivity with active LOW
14	IRQE_SENS	1: Level sensitivity with active LOW Sensitivity type of the associated Interrupt Source 0: Edge sensitivity with active LOW
13	IRQD_SENS	1: Level sensitivity with active LOW Sensitivity type of the associated Interrupt Source 0: Edge sensitivity with active LOW
12	IRQC_SENS	1: Level sensitivity with active LOW Sensitivity type of the associated Interrupt Source 0: Edge sensitivity with active LOW
11	IRQB_SENS	1: Level sensitivity with active LOW Sensitivity type of the associated Interrupt Source 0: Edge sensitivity with active LOW
10	IRQA_SENS	1: Level sensitivity with active LOW Sensitivity type of the associated Interrupt Source 0: Edge sensitivity with active LOW
9	IRQ9_SENS	1: Level sensitivity with active LOW Sensitivity type of the associated Interrupt Source 0: Edge sensitivity with active LOW
8	IRQ8_SENS	1: Level sensitivity with active LOW Sensitivity type of the associated Interrupt Source 0: Edge sensitivity with active LOW
7	IRQ7_SENS	1: Level sensitivity with active LOW Sensitivity type of the associated Interrupt Source

Bit(s)	Name	Description
6	IRQ6_SENS	0: Edge sensitivity with active LOW 1: Level sensitivity with active LOW Sensitivity type of the associated Interrupt Source
5	IRQ5_SENS	0: Edge sensitivity with active LOW 1: Level sensitivity with active LOW Sensitivity type of the associated Interrupt Source
4	IRQ4_SENS	0: Edge sensitivity with active LOW 1: Level sensitivity with active LOW Sensitivity type of the associated Interrupt Source
3	IRQ3_SENS	0: Edge sensitivity with active LOW 1: Level sensitivity with active LOW Sensitivity type of the associated Interrupt Source
2	IRQ2_SENS	0: Edge sensitivity with active LOW 1: Level sensitivity with active LOW Sensitivity type of the associated Interrupt Source
1	IRQ1_SENS	0: Edge sensitivity with active LOW 1: Level sensitivity with active LOW Sensitivity type of the associated Interrupt Source
0	IRQ0_SENS	0: Edge sensitivity with active LOW 1: Level sensitivity with active LOW Sensitivity type of the associated Interrupt Source

151A80B4 IRQ_SENSM IRQ Sensitive Register Middle 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	IRQ3F_SENS	IRQ3E_SENS	IRQ3D_SENS	IRQ3C_SENS	IRQ3B_SENS	IRQ3A_SENS	IRQ39_SENS	IRQ38_SENS	IRQ37_SENS	IRQ36_SENS	IRQ35_SENS	IRQ34_SENS	IRQ33_SENS	IRQ32_SENS	IRQ31_SENS	IRQ30_SENS
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IRQ2F_SENS	IRQ2E_SENS	IRQ2D_SENS	IRQ2C_SENS	IRQ2B_SENS	IRQ2A_SENS	IRQ29_SENS	IRQ28_SENS	IRQ27_SENS	IRQ26_SENS	IRQ25_SENS	IRQ24_SENS	IRQ23_SENS	IRQ22_SENS	IRQ21_SENS	IRQ20_SENS
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	IRQ3F_SENS	Sensitivity type of the associated Interrupt Source 0: Edge sensitivity with active LOW 1: Level sensitivity with active LOW
30	IRQ3E_SENS	Sensitivity type of the associated Interrupt Source 0: Edge sensitivity with active LOW 1: Level sensitivity with active LOW
29	IRQ3D_SENS	Sensitivity type of the associated Interrupt Source

Bit(s)	Name	Description
28	IRQ3C_SENS	0: Edge sensitivity with active LOW 1: Level sensitivity with active LOW Sensitivity type of the associated Interrupt Source
27	IRQ3B_SENS	0: Edge sensitivity with active LOW 1: Level sensitivity with active LOW Sensitivity type of the associated Interrupt Source
26	IRQ3A_SENS	0: Edge sensitivity with active LOW 1: Level sensitivity with active LOW Sensitivity type of the associated Interrupt Source
25	IRQ39_SENS	0: Edge sensitivity with active LOW 1: Level sensitivity with active LOW Sensitivity type of the associated Interrupt Source
24	IRQ38_SENS	0: Edge sensitivity with active LOW 1: Level sensitivity with active LOW Sensitivity type of the associated Interrupt Source
23	IRQ37_SENS	0: Edge sensitivity with active LOW 1: Level sensitivity with active LOW Sensitivity type of the associated Interrupt Source
22	IRQ36_SENS	0: Edge sensitivity with active LOW 1: Level sensitivity with active LOW Sensitivity type of the associated Interrupt Source
21	IRQ35_SENS	0: Edge sensitivity with active LOW 1: Level sensitivity with active LOW Sensitivity type of the associated Interrupt Source
20	IRQ34_SENS	0: Edge sensitivity with active LOW 1: Level sensitivity with active LOW Sensitivity type of the associated Interrupt Source
19	IRQ33_SENS	0: Edge sensitivity with active LOW 1: Level sensitivity with active LOW Sensitivity type of the associated Interrupt Source
18	IRQ32_SENS	0: Edge sensitivity with active LOW 1: Level sensitivity with active LOW Sensitivity type of the associated Interrupt Source
17	IRQ31_SENS	0: Edge sensitivity with active LOW 1: Level sensitivity with active LOW Sensitivity type of the associated Interrupt Source
16	IRQ30_SENS	0: Edge sensitivity with active LOW 1: Level sensitivity with active LOW Sensitivity type of the associated Interrupt Source
15	IRQ2F_SENS	0: Edge sensitivity with active LOW 1: Level sensitivity with active LOW Sensitivity type of the associated Interrupt Source
14	IRQ2E_SENS	0: Edge sensitivity with active LOW 1: Level sensitivity with active LOW Sensitivity type of the associated Interrupt Source
13	IRQ2D_SENS	0: Edge sensitivity with active LOW 1: Level sensitivity with active LOW Sensitivity type of the associated Interrupt Source
12	IRQ2C_SENS	0: Edge sensitivity with active LOW 1: Level sensitivity with active LOW Sensitivity type of the associated Interrupt Source

Bit(s)	Name	Description
11	IRQ2B_SENS	Sensitivity type of the associated Interrupt Source 0: Edge sensitivity with active LOW 1: Level sensitivity with active LOW
10	IRQ2A_SENS	Sensitivity type of the associated Interrupt Source 0: Edge sensitivity with active LOW 1: Level sensitivity with active LOW
9	IRQ29_SENS	Sensitivity type of the associated Interrupt Source 0: Edge sensitivity with active LOW 1: Level sensitivity with active LOW
8	IRQ28_SENS	Sensitivity type of the associated Interrupt Source 0: Edge sensitivity with active LOW 1: Level sensitivity with active LOW
7	IRQ27_SENS	Sensitivity type of the associated Interrupt Source 0: Edge sensitivity with active LOW 1: Level sensitivity with active LOW
6	IRQ26_SENS	Sensitivity type of the associated Interrupt Source 0: Edge sensitivity with active LOW 1: Level sensitivity with active LOW
5	IRQ25_SENS	Sensitivity type of the associated Interrupt Source 0: Edge sensitivity with active LOW 1: Level sensitivity with active LOW
4	IRQ24_SENS	Sensitivity type of the associated Interrupt Source 0: Edge sensitivity with active LOW 1: Level sensitivity with active LOW
3	IRQ23_SENS	Sensitivity type of the associated Interrupt Source 0: Edge sensitivity with active LOW 1: Level sensitivity with active LOW
2	IRQ22_SENS	Sensitivity type of the associated Interrupt Source 0: Edge sensitivity with active LOW 1: Level sensitivity with active LOW
1	IRQ21_SENS	Sensitivity type of the associated Interrupt Source 0: Edge sensitivity with active LOW 1: Level sensitivity with active LOW
0	IRQ20_SENS	Sensitivity type of the associated Interrupt Source 0: Edge sensitivity with active LOW 1: Level sensitivity with active LOW

151A80C0		IRQ_SOFT			IRQ Software Interrupt Register												00000000	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16		
Name	IRQ1F_SOFT	IRQ1E_SOFT	IRQ1D_SOFT	IRQ1C_SOFT	IRQ1B_SOFT	IRQ1A_SOFT	IRQ19_SOFT	IRQ18_SOFT	IRQ17_SOFT	IRQ16_SOFT	IRQ15_SOFT	IRQ14_SOFT	IRQ13_SOFT	IRQ12_SOFT	IRQ11_SOFT	IRQ10_SOFT		
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
Name	IRQF_S_OFT	IRQE_S_OFT	IRQD_S_OFT	IRQC_S_OFT	IRQB_S_OFT	IRQA_S_OFT	IRQ9_S_OFT	IRQ8_S_OFT	IRQ7_S_OFT	IRQ6_S_OFT	IRQ5_S_OFT	IRQ4_S_OFT	IRQ3_S_OFT	IRQ2_S_OFT	IRQ1_S_OFT	IRQ0_S_OFT		

Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	IRQ1F_SOFT	Software Interrupt
30	IRQ1E_SOFT	Software Interrupt
29	IRQ1D_SOFT	Software Interrupt
28	IRQ1C_SOFT	Software Interrupt
27	IRQ1B_SOFT	Software Interrupt
26	IRQ1A_SOFT	Software Interrupt
25	IRQ19_SOFT	Software Interrupt
24	IRQ18_SOFT	Software Interrupt
23	IRQ17_SOFT	Software Interrupt
22	IRQ16_SOFT	Software Interrupt
21	IRQ15_SOFT	Software Interrupt
20	IRQ14_SOFT	Software Interrupt
19	IRQ13_SOFT	Software Interrupt
18	IRQ12_SOFT	Software Interrupt
17	IRQ11_SOFT	Software Interrupt
16	IRQ10_SOFT	Software Interrupt
15	IRQF_SOFT	Software Interrupt
14	IRQE_SOFT	Software Interrupt
13	IRQD_SOFT	Software Interrupt
12	IRQC_SOFT	Software Interrupt
11	IRQB_SOFT	Software Interrupt
10	IRQA_SOFT	Software Interrupt
9	IRQ9_SOFT	Software Interrupt
8	IRQ8_SOFT	Software Interrupt
7	IRQ7_SOFT	Software Interrupt
6	IRQ6_SOFT	Software Interrupt
5	IRQ5_SOFT	Software Interrupt
4	IRQ4_SOFT	Software Interrupt
3	IRQ3_SOFT	Software Interrupt
2	IRQ2_SOFT	Software Interrupt
1	IRQ1_SOFT	Software Interrupt
0	IRQ0_SOFT	Software Interrupt

151A80C4	IRQ_SOFTM			IRQ Software Interrupt Register Middle												00000000	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
Name	IRQ3F_SOFT	IRQ3E_SOFT	IRQ3D_SOFT	IRQ3C_SOFT	IRQ3B_SOFT	IRQ3A_SOFT	IRQ39_SOFT	IRQ38_SOFT	IRQ37_SOFT	IRQ36_SOFT	IRQ35_SOFT	IRQ34_SOFT	IRQ33_SOFT	IRQ32_SOFT	IRQ31_SOFT	IRQ30_SOFT	
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	

Name	IRQ2F_SOFT	IRQ2E_SOFT	IRQ2D_SOFT	IRQ2C_SOFT	IRQ2B_SOFT	IRQ2A_SOFT	IRQ29_SOFT	IRQ28_SOFT	IRQ27_SOFT	IRQ26_SOFT	IRQ25_SOFT	IRQ24_SOFT	IRQ23_SOFT	IRQ22_SOFT	IRQ21_SOFT	IRQ20_SOFT
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	IRQ3F_SOFT	Software Interrupt
30	IRQ3E_SOFT	Software Interrupt
29	IRQ3D_SOFT	Software Interrupt
28	IRQ3C_SOFT	Software Interrupt
27	IRQ3B_SOFT	Software Interrupt
26	IRQ3A_SOFT	Software Interrupt
25	IRQ39_SOFT	Software Interrupt
24	IRQ38_SOFT	Software Interrupt
23	IRQ37_SOFT	Software Interrupt
22	IRQ36_SOFT	Software Interrupt
21	IRQ35_SOFT	Software Interrupt
20	IRQ34_SOFT	Software Interrupt
19	IRQ33_SOFT	Software Interrupt
18	IRQ32_SOFT	Software Interrupt
17	IRQ31_SOFT	Software Interrupt
16	IRQ30_SOFT	Software Interrupt
15	IRQ2F_SOFT	Software Interrupt
14	IRQ2E_SOFT	Software Interrupt
13	IRQ2D_SOFT	Software Interrupt
12	IRQ2C_SOFT	Software Interrupt
11	IRQ2B_SOFT	Software Interrupt
10	IRQ2A_SOFT	Software Interrupt
9	IRQ29_SOFT	Software Interrupt
8	IRQ28_SOFT	Software Interrupt
7	IRQ27_SOFT	Software Interrupt
6	IRQ26_SOFT	Software Interrupt
5	IRQ25_SOFT	Software Interrupt
4	IRQ24_SOFT	Software Interrupt
3	IRQ23_SOFT	Software Interrupt
2	IRQ22_SOFT	Software Interrupt
1	IRQ21_SOFT	Software Interrupt
0	IRQ20_SOFT	Software Interrupt

151A80D0				FIQ_CON												FIQ Control Register												00000001			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16															
Name																															
Type																															
Reset																															

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															FIQ_SE NS	FIQ_M ASK
Type															RW	RW
Reset															0	1

Bit(s)	Name	Description
1	FIQ_SENS	Sensitivity type of the FIQ Interrupt Source 0: Edge sensitivity with active LOW 1: Level sensitivity with active LOW
0	FIQ_MASK	Mask control for the FIQ Interrupt Source 0: Interrupt is enabled 1: Interrupt is disabled

151A80D4 **FIQ_EOI** **FIQ End of Interrupt Register** 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																FIQ_EO I
Type																WO
Reset																0

Bit(s)	Name	Description
0	FIQ_EOI	End of Interrupt command 0: No interrupt request is generated 1: Interrupt request is in-service

151A80D8 **IRQ_STA2** **Binary Coded Value of IRQ_STATUS** 00000100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																

Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								NOIRQ			IRQ_STA2					
Type								RS			RC					
Reset								1			0	0	0	0	0	0

Bit(s)	Name	Description
8	NOIRQ	Indicating if there is an IRQ or not. If there is no IRQ, this bit is HIGH
5:0	IRQ_STA2	Binary coded value of IRQ_STA

151A80DC IRQ_EOI2 Binary Coded Value of IRQ_EOI 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											IRQ_EOI2					
Type											WO					
Reset											0	0	0	0	0	0

Bit(s)	Name	Description
5:0	IRQ_EOI2	Binary coded value of IRQ_EOI

151A80E0 IRQ_ASTA Binary Value of IRQ Source Status 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	IRQ1F_ASTA	IRQ1E_ASTA	IRQ1D_ASTA	IRQ1C_ASTA	IRQ1B_ASTA	IRQ1A_ASTA	IRQ19_ASTA	IRQ18_ASTA	IRQ17_ASTA	IRQ16_ASTA	IRQ15_ASTA	IRQ14_ASTA	IRQ13_ASTA	IRQ12_ASTA	IRQ11_ASTA	IRQ10_ASTA
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	IRQF_A STA	IRQE_A STA	IRQD_A ASTA	IRQC_A STA	IRQB_A STA	IRQA_A ASTA	IRQ9_A STA	IRQ8_A STA	IRQ7_A STA	IRQ6_A STA	IRQ5_A STA	IRQ4_A STA	IRQ3_A STA	IRQ2_A STA	IRQ1_A STA	IRQ0_A STA
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	IRQ1F_ASTA	Status of interrupt source 0: no interrupt. 1: interrupt occurs
30	IRQ1E_ASTA	Status of interrupt source 0: no interrupt. 1: interrupt occurs
29	IRQ1D_ASTA	Status of interrupt source 0: no interrupt. 1: interrupt occurs
28	IRQ1C_ASTA	Status of interrupt source 0: no interrupt. 1: interrupt occurs
27	IRQ1B_ASTA	Status of interrupt source 0: no interrupt. 1: interrupt occurs
26	IRQ1A_ASTA	Status of interrupt source 0: no interrupt. 1: interrupt occurs
25	IRQ19_ASTA	Status of interrupt source 0: no interrupt. 1: interrupt occurs
24	IRQ18_ASTA	Status of interrupt source 0: no interrupt. 1: interrupt occurs
23	IRQ17_ASTA	Status of interrupt source 0: no interrupt. 1: interrupt occurs
22	IRQ16_ASTA	Status of interrupt source 0: no interrupt. 1: interrupt occurs
21	IRQ15_ASTA	Status of interrupt source 0: no interrupt. 1: interrupt occurs
20	IRQ14_ASTA	Status of interrupt source 0: no interrupt. 1: interrupt occurs
19	IRQ13_ASTA	Status of interrupt source 0: no interrupt. 1: interrupt occurs
18	IRQ12_ASTA	Status of interrupt source 0: no interrupt. 1: interrupt occurs
17	IRQ11_ASTA	Status of interrupt source 0: no interrupt. 1: interrupt occurs

Bit(s)	Name	Description
16	IRQ10_ASTA	Status of interrupt source 0: no interrupt. 1: interrupt occurs
15	IRQF_ASTA	Status of interrupt source 0: no interrupt. 1: interrupt occurs
14	IRQE_ASTA	Status of interrupt source 0: no interrupt. 1: interrupt occurs
13	IRQD_ASTA	Status of interrupt source 0: no interrupt. 1: interrupt occurs
12	IRQC_ASTA	Status of interrupt source 0: no interrupt. 1: interrupt occurs
11	IRQB_ASTA	Status of interrupt source 0: no interrupt. 1: interrupt occurs
10	IRQA_ASTA	Status of interrupt source 0: no interrupt. 1: interrupt occurs
9	IRQ9_ASTA	Status of interrupt source 0: no interrupt. 1: interrupt occurs
8	IRQ8_ASTA	Status of interrupt source 0: no interrupt. 1: interrupt occurs
7	IRQ7_ASTA	Status of interrupt source 0: no interrupt. 1: interrupt occurs
6	IRQ6_ASTA	Status of interrupt source 0: no interrupt. 1: interrupt occurs
5	IRQ5_ASTA	Status of interrupt source 0: no interrupt. 1: interrupt occurs
4	IRQ4_ASTA	Status of interrupt source 0: no interrupt. 1: interrupt occurs
3	IRQ3_ASTA	Status of interrupt source 0: no interrupt. 1: interrupt occurs
2	IRQ2_ASTA	Status of interrupt source 0: no interrupt. 1: interrupt occurs
1	IRQ1_ASTA	Status of interrupt source 0: no interrupt. 1: interrupt occurs
0	IRQ0_ASTA	Status of interrupt source 0: no interrupt. 1: interrupt occurs

151A80E4 IRQ_ASTAM Binary Value of IRQ Source Status Middle 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	IRQ3F_ASTA	IRQ3E_ASTA	IRQ3D_ASTA	IRQ3C_ASTA	IRQ3B_ASTA	IRQ3A_ASTA	IRQ39_ASTA	IRQ38_ASTA	IRQ37_ASTA	IRQ36_ASTA	IRQ35_ASTA	IRQ34_ASTA	IRQ33_ASTA	IRQ32_ASTA	IRQ31_ASTA	IRQ30_ASTA
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IRQ2F_ASTA	IRQ2E_ASTA	IRQ2D_ASTA	IRQ2C_ASTA	IRQ2B_ASTA	IRQ2A_ASTA	IRQ29_ASTA	IRQ28_ASTA	IRQ27_ASTA	IRQ26_ASTA	IRQ25_ASTA	IRQ24_ASTA	IRQ23_ASTA	IRQ22_ASTA	IRQ21_ASTA	IRQ20_ASTA
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	IRQ3F_ASTA	Status of interrupt source 0: no interrupt. 1: interrupt occurs
30	IRQ3E_ASTA	Status of interrupt source 0: no interrupt. 1: interrupt occurs
29	IRQ3D_ASTA	Status of interrupt source 0: no interrupt. 1: interrupt occurs
28	IRQ3C_ASTA	Status of interrupt source 0: no interrupt. 1: interrupt occurs
27	IRQ3B_ASTA	Status of interrupt source 0: no interrupt. 1: interrupt occurs
26	IRQ3A_ASTA	Status of interrupt source 0: no interrupt. 1: interrupt occurs
25	IRQ39_ASTA	Status of interrupt source 0: no interrupt. 1: interrupt occurs
24	IRQ38_ASTA	Status of interrupt source 0: no interrupt. 1: interrupt occurs
23	IRQ37_ASTA	Status of interrupt source 0: no interrupt. 1: interrupt occurs
22	IRQ36_ASTA	Status of interrupt source 0: no interrupt. 1: interrupt occurs
21	IRQ35_ASTA	Status of interrupt source 0: no interrupt. 1: interrupt occurs
20	IRQ34_ASTA	Status of interrupt source

Bit(s)	Name	Description
19	IRQ33_ASTA	0: no interrupt. 1: interrupt occurs Status of interrupt source
18	IRQ32_ASTA	0: no interrupt. 1: interrupt occurs Status of interrupt source
17	IRQ31_ASTA	0: no interrupt. 1: interrupt occurs Status of interrupt source
16	IRQ30_ASTA	0: no interrupt. 1: interrupt occurs Status of interrupt source
15	IRQ2F_ASTA	0: no interrupt. 1: interrupt occurs Status of interrupt source
14	IRQ2E_ASTA	0: no interrupt. 1: interrupt occurs Status of interrupt source
13	IRQ2D_ASTA	0: no interrupt. 1: interrupt occurs Status of interrupt source
12	IRQ2C_ASTA	0: no interrupt. 1: interrupt occurs Status of interrupt source
11	IRQ2B_ASTA	0: no interrupt. 1: interrupt occurs Status of interrupt source
10	IRQ2A_ASTA	0: no interrupt. 1: interrupt occurs Status of interrupt source
9	IRQ29_ASTA	0: no interrupt. 1: interrupt occurs Status of interrupt source
8	IRQ28_ASTA	0: no interrupt. 1: interrupt occurs Status of interrupt source
7	IRQ27_ASTA	0: no interrupt. 1: interrupt occurs Status of interrupt source
6	IRQ26_ASTA	0: no interrupt. 1: interrupt occurs Status of interrupt source
5	IRQ25_ASTA	0: no interrupt. 1: interrupt occurs Status of interrupt source
4	IRQ24_ASTA	0: no interrupt. 1: interrupt occurs Status of interrupt source
3	IRQ23_ASTA	0: no interrupt. 1: interrupt occurs Status of interrupt source

Bit(s)	Name	Description
2	IRQ22_ASTA	Status of interrupt source 0: no interrupt. 1: interrupt occurs
1	IRQ21_ASTA	Status of interrupt source 0: no interrupt. 1: interrupt occurs
0	IRQ20_ASTA	Status of interrupt source 0: no interrupt. 1: interrupt occurs

151A80F0 **IRQ_EEVT** **Binary Value of EINT Event** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																EINT_EVENT
Type																RO
Reset																0

Bit(s)	Name	Description
0	EINT_EVENT	EINT event status 0: no EINT event. 1: EINT event occurs.

151A8100 **EINT_STA** **EINT Status Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													EINT13_STA	EINT12_STA	EINT11_STA	EINT10_STA
Type													RO	RO	RO	RO
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINTF_STA	EINTE_STA	EINTD_STA	EINTC_STA	EINTB_STA	EINTA_STA	EINT9_STA	EINT8_STA	EINT7_STA	EINT6_STA	EINT5_STA	EINT4_STA	EINT3_STA	EINT2_STA	EINT1_STA	EINT0_STA

Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
19	EINT13_STA	Interrupt Status 0: No interrupt request is generated 1: Interrupt request is pending
18	EINT12_STA	Interrupt Status 0: No interrupt request is generated 1: Interrupt request is pending
17	EINT11_STA	Interrupt Status 0: No interrupt request is generated 1: Interrupt request is pending
16	EINT10_STA	Interrupt Status 0: No interrupt request is generated 1: Interrupt request is pending
15	EINTF_STA	Interrupt Status 0: No interrupt request is generated 1: Interrupt request is pending
14	EINTE_STA	Interrupt Status 0: No interrupt request is generated 1: Interrupt request is pending
13	EINTD_STA	Interrupt Status 0: No interrupt request is generated 1: Interrupt request is pending
12	EINTC_STA	Interrupt Status 0: No interrupt request is generated 1: Interrupt request is pending
11	EINTB_STA	Interrupt Status 0: No interrupt request is generated 1: Interrupt request is pending
10	EINTA_STA	Interrupt Status 0: No interrupt request is generated 1: Interrupt request is pending
9	EINT9_STA	Interrupt Status 0: No interrupt request is generated 1: Interrupt request is pending
8	EINT8_STA	Interrupt Status 0: No interrupt request is generated 1: Interrupt request is pending
7	EINT7_STA	Interrupt Status 0: No interrupt request is generated 1: Interrupt request is pending
6	EINT6_STA	Interrupt Status 0: No interrupt request is generated 1: Interrupt request is pending
5	EINT5_STA	Interrupt Status 0: No interrupt request is generated 1: Interrupt request is pending
4	EINT4_STA	Interrupt Status 0: No interrupt request is generated 1: Interrupt request is pending

Bit(s)	Name	Description
3	EINT3_STA	Interrupt Status 0: No interrupt request is generated 1: Interrupt request is pending
2	EINT2_STA	Interrupt Status 0: No interrupt request is generated 1: Interrupt request is pending
1	EINT1_STA	Interrupt Status 0: No interrupt request is generated 1: Interrupt request is pending
0	EINT0_STA	Interrupt Status 0: No interrupt request is generated 1: Interrupt request is pending

151A8104		EINT_MASK				EINT Mask Register								000FFFFF			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
Name													EINT13_MASK	EINT12_MASK	EINT11_MASK	EINT10_MASK	
Type													RW	RW	RW	RW	
Reset													1	1	1	1	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Name	EINTF_MASK	EINTE_MASK	EINTD_MASK	EINTC_MASK	EINTB_MASK	EINTA_MASK	EINT9_MASK	EINT8_MASK	EINT7_MASK	EINT6_MASK	EINT5_MASK	EINT4_MASK	EINT3_MASK	EINT2_MASK	EINT1_MASK	EINT0_MASK	
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	

Bit(s)	Name	Description
19	EINT13_MASK	Mask control for the associated interrupt source in the IRQ controller 0: Interrupt is enabled 1: Interrupt is disabled
18	EINT12_MASK	Mask control for the associated interrupt source in the IRQ controller 0: Interrupt is enabled 1: Interrupt is disabled
17	EINT11_MASK	Mask control for the associated interrupt source in the IRQ controller 0: Interrupt is enabled 1: Interrupt is disabled
16	EINT10_MASK	Mask control for the associated interrupt source in the IRQ controller 0: Interrupt is enabled 1: Interrupt is disabled
15	EINTF_MASK	Mask control for the associated interrupt source in the IRQ controller 0: Interrupt is enabled 1: Interrupt is disabled
14	EINTE_MASK	Mask control for the associated interrupt source in the IRQ controller 0: Interrupt is enabled 1: Interrupt is disabled

Bit(s)	Name	Description
13	EINTD_MASK	1: Interrupt is disabled Mask control for the associated interrupt source in the IRQ controller 0: Interrupt is enabled
12	EINTC_MASK	1: Interrupt is disabled Mask control for the associated interrupt source in the IRQ controller 0: Interrupt is enabled
11	EINTB_MASK	1: Interrupt is disabled Mask control for the associated interrupt source in the IRQ controller 0: Interrupt is enabled
10	EINTA_MASK	1: Interrupt is disabled Mask control for the associated interrupt source in the IRQ controller 0: Interrupt is enabled
9	EINT9_MASK	1: Interrupt is disabled Mask control for the associated interrupt source in the IRQ controller 0: Interrupt is enabled
8	EINT8_MASK	1: Interrupt is disabled Mask control for the associated interrupt source in the IRQ controller 0: Interrupt is enabled
7	EINT7_MASK	1: Interrupt is disabled Mask control for the associated interrupt source in the IRQ controller 0: Interrupt is enabled
6	EINT6_MASK	1: Interrupt is disabled Mask control for the associated interrupt source in the IRQ controller 0: Interrupt is enabled
5	EINT5_MASK	1: Interrupt is disabled Mask control for the associated interrupt source in the IRQ controller 0: Interrupt is enabled
4	EINT4_MASK	1: Interrupt is disabled Mask control for the associated interrupt source in the IRQ controller 0: Interrupt is enabled
3	EINT3_MASK	1: Interrupt is disabled Mask control for the associated interrupt source in the IRQ controller 0: Interrupt is enabled
2	EINT2_MASK	1: Interrupt is disabled Mask control for the associated interrupt source in the IRQ controller 0: Interrupt is enabled
1	EINT1_MASK	1: Interrupt is disabled Mask control for the associated interrupt source in the IRQ controller 0: Interrupt is enabled
0	EINT0_MASK	1: Interrupt is disabled Mask control for the associated interrupt source in the IRQ controller 0: Interrupt is enabled

151A8108	EINT_MASK_CLR				EINT Mask Clear Register								00000000			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													EINT13_MCLR	EINT12_MCLR	EINT11_MCLR	EINT10_MCLR

Type													WO	WO	WO	WO
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINTF_MCLR	EINTE_MCLR	EINTD_MCLR	EINTC_MCLR	EINTB_MCLR	EINTA_MCLR	EINT9_MCLR	EINT8_MCLR	EINT7_MCLR	EINT6_MCLR	EINT5_MCLR	EINT4_MCLR	EINT3_MCLR	EINT2_MCLR	EINT1_MCLR	EINT0_MCLR
Type	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
19	EINT13_MCLR	Disable mask for the associated external interrupt source 0: No effect. 1: Disable the corresponding MASK bit.
18	EINT12_MCLR	Disable mask for the associated external interrupt source 0: No effect. 1: Disable the corresponding MASK bit.
17	EINT11_MCLR	Disable mask for the associated external interrupt source 0: No effect. 1: Disable the corresponding MASK bit.
16	EINT10_MCLR	Disable mask for the associated external interrupt source 0: No effect. 1: Disable the corresponding MASK bit.
15	EINTF_MCLR	Disable mask for the associated external interrupt source 0: No effect. 1: Disable the corresponding MASK bit.
14	EINTE_MCLR	Disable mask for the associated external interrupt source 0: No effect. 1: Disable the corresponding MASK bit.
13	EINTD_MCLR	Disable mask for the associated external interrupt source 0: No effect. 1: Disable the corresponding MASK bit.
12	EINTC_MCLR	Disable mask for the associated external interrupt source 0: No effect. 1: Disable the corresponding MASK bit.
11	EINTB_MCLR	Disable mask for the associated external interrupt source 0: No effect. 1: Disable the corresponding MASK bit.
10	EINTA_MCLR	Disable mask for the associated external interrupt source 0: No effect. 1: Disable the corresponding MASK bit.
9	EINT9_MCLR	Disable mask for the associated external interrupt source 0: No effect. 1: Disable the corresponding MASK bit.
8	EINT8_MCLR	Disable mask for the associated external interrupt source 0: No effect. 1: Disable the corresponding MASK bit.
7	EINT7_MCLR	Disable mask for the associated external interrupt source 0: No effect. 1: Disable the corresponding MASK bit.
6	EINT6_MCLR	Disable mask for the associated external interrupt source

Bit(s)	Name	Description
5	EINT5_MCLR	0: No effect. 1: Disable the corresponding MASK bit. Disable mask for the associated external interrupt source
4	EINT4_MCLR	0: No effect. 1: Disable the corresponding MASK bit. Disable mask for the associated external interrupt source
3	EINT3_MCLR	0: No effect. 1: Disable the corresponding MASK bit. Disable mask for the associated external interrupt source
2	EINT2_MCLR	0: No effect. 1: Disable the corresponding MASK bit. Disable mask for the associated external interrupt source
1	EINT1_MCLR	0: No effect. 1: Disable the corresponding MASK bit. Disable mask for the associated external interrupt source
0	EINT0_MCLR	0: No effect. 1: Disable the corresponding MASK bit. Disable mask for the associated external interrupt source

151A810C EINT_MASK_SET EINT Mask Set Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													EINT13_MSET	EINT12_MSET	EINT11_MSET	EINT10_MSET
Type													WO	WO	WO	WO
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINTF_MSET	EINTE_MSET	EINTD_MSET	EINTC_MSET	EINTB_MSET	EINTA_MSET	EINT9_MSET	EINT8_MSET	EINT7_MSET	EINT6_MSET	EINT5_MSET	EINT4_MSET	EINT3_MSET	EINT2_MSET	EINT1_MSET	EINT0_MSET
Type	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
19	EINT13_MSET	Enable mask for the associated external interrupt source. 0: No effect. 1: Enable corresponding MASK bit.
18	EINT12_MSET	Enable mask for the associated external interrupt source. 0: No effect. 1: Enable corresponding MASK bit.
17	EINT11_MSET	Enable mask for the associated external interrupt source. 0: No effect. 1: Enable corresponding MASK bit.

Bit(s)	Name	Description
16	EINT10_MSET	Enable mask for the associated external interrupt source. 0: No effect. 1: Enable corresponding MASK bit.
15	EINTF_MSET	Enable mask for the associated external interrupt source. 0: No effect. 1: Enable corresponding MASK bit.
14	EINTE_MSET	Enable mask for the associated external interrupt source. 0: No effect. 1: Enable corresponding MASK bit.
13	EINTD_MSET	Enable mask for the associated external interrupt source. 0: No effect. 1: Enable corresponding MASK bit.
12	EINTC_MSET	Enable mask for the associated external interrupt source. 0: No effect. 1: Enable corresponding MASK bit.
11	EINTB_MSET	Enable mask for the associated external interrupt source. 0: No effect. 1: Enable corresponding MASK bit.
10	EINTA_MSET	Enable mask for the associated external interrupt source. 0: No effect. 1: Enable corresponding MASK bit.
9	EINT9_MSET	Enable mask for the associated external interrupt source. 0: No effect. 1: Enable corresponding MASK bit.
8	EINT8_MSET	Enable mask for the associated external interrupt source. 0: No effect. 1: Enable corresponding MASK bit.
7	EINT7_MSET	Enable mask for the associated external interrupt source. 0: No effect. 1: Enable corresponding MASK bit.
6	EINT6_MSET	Enable mask for the associated external interrupt source. 0: No effect. 1: Enable corresponding MASK bit.
5	EINT5_MSET	Enable mask for the associated external interrupt source. 0: No effect. 1: Enable corresponding MASK bit.
4	EINT4_MSET	Enable mask for the associated external interrupt source. 0: No effect. 1: Enable corresponding MASK bit.
3	EINT3_MSET	Enable mask for the associated external interrupt source. 0: No effect. 1: Enable corresponding MASK bit.
2	EINT2_MSET	Enable mask for the associated external interrupt source. 0: No effect. 1: Enable corresponding MASK bit.
1	EINT1_MSET	Enable mask for the associated external interrupt source. 0: No effect. 1: Enable corresponding MASK bit.
0	EINT0_MSET	Enable mask for the associated external interrupt source. 0: No effect. 1: Enable corresponding MASK bit.

151A8110 EINT_INTACK EINT Interrupt Acknowledge Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													EINT13_ACK	EINT12_ACK	EINT11_ACK	EINT10_ACK
Type													WO	WO	WO	WO
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINTF_ACK	EINTE_ACK	EINTD_ACK	EINTC_ACK	EINTB_ACK	EINTA_ACK	EINT9_ACK	EINT8_ACK	EINT7_ACK	EINT6_ACK	EINT5_ACK	EINT4_ACK	EINT3_ACK	EINT2_ACK	EINT1_ACK	EINT0_ACK
Type	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
19	EINT13_ACK	Interrupt acknowledgement 0: No effect. 1: Interrupt Request is acknowledged.
18	EINT12_ACK	Interrupt acknowledgement 0: No effect. 1: Interrupt Request is acknowledged.
17	EINT11_ACK	Interrupt acknowledgement 0: No effect. 1: Interrupt Request is acknowledged.
16	EINT10_ACK	Interrupt acknowledgement 0: No effect. 1: Interrupt Request is acknowledged.
15	EINTF_ACK	Interrupt acknowledgement 0: No effect. 1: Interrupt Request is acknowledged.
14	EINTE_ACK	Interrupt acknowledgement 0: No effect. 1: Interrupt Request is acknowledged.
13	EINTD_ACK	Interrupt acknowledgement 0: No effect. 1: Interrupt Request is acknowledged.
12	EINTC_ACK	Interrupt acknowledgement 0: No effect. 1: Interrupt Request is acknowledged.
11	EINTB_ACK	Interrupt acknowledgement 0: No effect. 1: Interrupt Request is acknowledged.
10	EINTA_ACK	Interrupt acknowledgement 0: No effect. 1: Interrupt Request is acknowledged.
9	EINT9_ACK	Interrupt acknowledgement 0: No effect. 1: Interrupt Request is acknowledged.
8	EINT8_ACK	Interrupt acknowledgement 0: No effect. 1: Interrupt Request is acknowledged.

Bit(s)	Name	Description
7	EINT7_ACK	0: No effect. 1: Interrupt Request is acknowledged. Interrupt acknowledgement
6	EINT6_ACK	0: No effect. 1: Interrupt Request is acknowledged. Interrupt acknowledgement
5	EINT5_ACK	0: No effect. 1: Interrupt Request is acknowledged. Interrupt acknowledgement
4	EINT4_ACK	0: No effect. 1: Interrupt Request is acknowledged. Interrupt acknowledgement
3	EINT3_ACK	0: No effect. 1: Interrupt Request is acknowledged. Interrupt acknowledgement
2	EINT2_ACK	0: No effect. 1: Interrupt Request is acknowledged. Interrupt acknowledgement
1	EINT1_ACK	0: No effect. 1: Interrupt Request is acknowledged. Interrupt acknowledgement
0	EINT0_ACK	0: No effect. 1: Interrupt Request is acknowledged. Interrupt acknowledgement

151A8114	EINT_SENS				EINT Sensitive Register								000FFFFF			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													EINT13_SENS	EINT12_SENS	EINT11_SENS	EINT10_SENS
Type													RW	RW	RW	RW
Reset													1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINTF_SENS	EINTE_SENS	EINTD_SENS	EINTC_SENS	EINTB_SENS	EINTA_SENS	EINT9_SENS	EINT8_SENS	EINT7_SENS	EINT6_SENS	EINT5_SENS	EINT4_SENS	EINT3_SENS	EINT2_SENS	EINT1_SENS	EINT0_SENS
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
19	EINT13_SENS	Sensitive type of the associated external interrupt source 0: Edge sensitivity. 1: Level sensitivity.

Bit(s)	Name	Description
18	EINT12_SENS	Sensitive type of the associated external interrupt source 0: Edge sensitivity. 1: Level sensitivity.
17	EINT11_SENS	Sensitive type of the associated external interrupt source 0: Edge sensitivity. 1: Level sensitivity.
16	EINT10_SENS	Sensitive type of the associated external interrupt source 0: Edge sensitivity. 1: Level sensitivity.
15	EINTF_SENS	Sensitive type of the associated external interrupt source 0: Edge sensitivity. 1: Level sensitivity.
14	EINTE_SENS	Sensitive type of the associated external interrupt source 0: Edge sensitivity. 1: Level sensitivity.
13	EINTD_SENS	Sensitive type of the associated external interrupt source 0: Edge sensitivity. 1: Level sensitivity.
12	EINTC_SENS	Sensitive type of the associated external interrupt source 0: Edge sensitivity. 1: Level sensitivity.
11	EINTB_SENS	Sensitive type of the associated external interrupt source 0: Edge sensitivity. 1: Level sensitivity.
10	EINTA_SENS	Sensitive type of the associated external interrupt source 0: Edge sensitivity. 1: Level sensitivity.
9	EINT9_SENS	Sensitive type of the associated external interrupt source 0: Edge sensitivity. 1: Level sensitivity.
8	EINT8_SENS	Sensitive type of the associated external interrupt source 0: Edge sensitivity. 1: Level sensitivity.
7	EINT7_SENS	Sensitive type of the associated external interrupt source 0: Edge sensitivity. 1: Level sensitivity.
6	EINT6_SENS	Sensitive type of the associated external interrupt source 0: Edge sensitivity. 1: Level sensitivity.
5	EINT5_SENS	Sensitive type of the associated external interrupt source 0: Edge sensitivity. 1: Level sensitivity.
4	EINT4_SENS	Sensitive type of the associated external interrupt source 0: Edge sensitivity. 1: Level sensitivity.
3	EINT3_SENS	Sensitive type of the associated external interrupt source 0: Edge sensitivity. 1: Level sensitivity.
2	EINT2_SENS	Sensitive type of the associated external interrupt source 0: Edge sensitivity. 1: Level sensitivity.
1	EINT1_SENS	Sensitive type of the associated external interrupt source 0: Edge sensitivity.

Bit(s)	Name	Description
0	EINT0_SENS	1: Level sensitivity. Sensitive type of the associated external interrupt source 0: Edge sensitivity. 1: Level sensitivity.

151A8118 EINT_SOFT EINT Software Interrupt Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													EINT13_SOFT	EINT12_SOFT	EINT11_SOFT	EINT10_SOFT
Type													RW	RW	RW	RW
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINTF_SOFT	EINTE_SOFT	EINTD_SOFT	EINTC_SOFT	EINTB_SOFT	EINTA_SOFT	EINT9_SOFT	EINT8_SOFT	EINT7_SOFT	EINT6_SOFT	EINT5_SOFT	EINT4_SOFT	EINT3_SOFT	EINT2_SOFT	EINT1_SOFT	EINT0_SOFT
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
19	EINT13_SOFT	Software Interrupt
18	EINT12_SOFT	Software Interrupt
17	EINT11_SOFT	Software Interrupt
16	EINT10_SOFT	Software Interrupt
15	EINTF_SOFT	Software Interrupt
14	EINTE_SOFT	Software Interrupt
13	EINTD_SOFT	Software Interrupt
12	EINTC_SOFT	Software Interrupt
11	EINTB_SOFT	Software Interrupt
10	EINTA_SOFT	Software Interrupt
9	EINT9_SOFT	Software Interrupt
8	EINT8_SOFT	Software Interrupt
7	EINT7_SOFT	Software Interrupt
6	EINT6_SOFT	Software Interrupt
5	EINT5_SOFT	Software Interrupt
4	EINT4_SOFT	Software Interrupt
3	EINT3_SOFT	Software Interrupt
2	EINT2_SOFT	Software Interrupt
1	EINT1_SOFT	Software Interrupt
0	EINT0_SOFT	Software Interrupt

151A8120 EINT0_CON EINT 0 De-bounce Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT0_EN	EINT0_PRESCALER				EINT0_POL	EINT0_CNT									
Type	RW	RW				RW	RW									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	EINT0_EN	De-bounce control circuit 0: Disable 1: Enable
14:12	EINT0_PRESCALER	Determine the clock cycle period for debounce count. 3'b000: 32768Hz, max 3'b001: 16384Hz 3'b010: 8192Hz 3'b011: 4096Hz 3'b100: 2048Hz, max 3'b101: 1024Hz 3'b110: 512Hz 3'b111: 256Hz, max
11	EINT0_POL	Activation type of the EINT source 0: Negative polarity 1: Positive polarity
10:0	EINT0_CNT	De-bounce duration in terms of numbers of 32768Hz clock cycles. The cycle length is determined by PRESCALER

151A8130 EINT1_CON EINT 1 De-bounce Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT1_EN	EINT1_PRESCALER				EINT1_POL	EINT1_CNT									
Type	RW	RW				RW	RW									

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	EINT1_EN	De-bounce control circuit 0: Disable 1: Enable
14:12	EINT1_PRESCALER	Determine the clock cycle period for debounce count. 3'b000: 32768Hz, max 3'b001: 16384Hz 3'b010: 8192Hz 3'b011: 4096Hz 3'b100: 2048Hz, max 3'b101: 1024Hz 3'b110: 512Hz 3'b111: 256Hz, max
11	EINT1_POL	Activation type of the EINT source 0: Negative polarity 1: Positive polarity
10:0	EINT1_CNT	De-bounce duration in terms of numbers of 32768Hz clock cycles. The cycle length is determined by PRESCALER

151A8140		EINT2_CON				EINT 2 De-bounce Control Register											00000000	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16		
Name																		
Type																		
Reset																		
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
Name	EINT2_EN	EINT2_PRESCALER			EINT2_POL	EINT2_CNT												
Type	RW	RW			RW	RW												
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

Bit(s)	Name	Description
15	EINT2_EN	De-bounce control circuit 0: Disable 1: Enable
14:12	EINT2_PRESCALER	Determine the clock cycle period for debounce count. 3'b000: 32768Hz, max 3'b001: 16384Hz 3'b010: 8192Hz 3'b011: 4096Hz 3'b100: 2048Hz, max 3'b101: 1024Hz

Bit(s)	Name	Description
11	EINT2_POL	3'b110: 512Hz 3'b111: 256Hz, max Activation type of the EINT source 0: Negative polarity 1: Positive polarity
10:0	EINT2_CNT	De-bounce duration in terms of numbers of 32768Hz clock cycles. The cycle length is determined by PRESCALER

151A8150		<u>EINT3_CON</u>				EINT 3 De-bounce Control Register											00000000	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16		
Name																		
Type																		
Reset																		
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
Name	EINT3_EN	EINT3_PRESCALER				EINT3_POL	EINT3_CNT											
Type	RW	RW				RW	RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

Bit(s)	Name	Description
15	EINT3_EN	De-bounce control circuit 0: Disable 1: Enable
14:12	EINT3_PRESCALER	Determine the clock cycle period for debounce count. 3'b000: 32768Hz, max 3'b001: 16384Hz 3'b010: 8192Hz 3'b011: 4096Hz 3'b100: 2048Hz, max 3'b101: 1024Hz 3'b110: 512Hz 3'b111: 256Hz, max
11	EINT3_POL	Activation type of the EINT source 0: Negative polarity 1: Positive polarity
10:0	EINT3_CNT	De-bounce duration in terms of numbers of 32768Hz clock cycles. The cycle length is determined by PRESCALER

151A8160		<u>EINT4_CON</u>		EINT 4 De-bounce Control Register										00000000		
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT4_EN	EINT4_PRESCALER				EINT4_POL	EINT4_CNT									
Type	RW	RW				RW	RW									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	EINT4_EN	De-bounce control circuit 0: Disable 1: Enable
14:12	EINT4_PRESCALER	Determine the clock cycle period for debounce count. 3'b000: 32768Hz, max 3'b001: 16384Hz 3'b010: 8192Hz 3'b011: 4096Hz 3'b100: 2048Hz, max 3'b101: 1024Hz 3'b110: 512Hz 3'b111: 256Hz, max
11	EINT4_POL	Activation type of the EINT source 0: Negative polarity 1: Positive polarity
10:0	EINT4_CNT	De-bounce duration in terms of numbers of 32768Hz clock cycles. The cycle length is determined by PRESCALER

151A8170 EINT5_CON EINT 5 De-bounce Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT5_EN	EINT5_PRESCALER				EINT5_POL	EINT5_CNT									
Type	RW	RW				RW	RW									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	EINT5_EN	De-bounce control circuit 0: Disable 1: Enable
14:12	EINT5_PRESCALER	Determine the clock cycle period for debounce count. 3'b000: 32768Hz, max 3'b001: 16384Hz 3'b010: 8192Hz 3'b011: 4096Hz 3'b100: 2048Hz, max 3'b101: 1024Hz 3'b110: 512Hz 3'b111: 256Hz, max
11	EINT5_POL	Activation type of the EINT source 0: Negative polarity 1: Positive polarity
10:0	EINT5_CNT	De-bounce duration in terms of numbers of 32768Hz clock cycles. The cycle length is determined by PRESCALER

151A8180		EINT6_CON				EINT 6 De-bounce Control Register											00000000	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16		
Name																		
Type																		
Reset																		
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
Name	EINT6_EN	EINT6_PRESCALER			EINT6_POL	EINT6_CNT												
Type	RW	RW			RW	RW												
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

Bit(s)	Name	Description
15	EINT6_EN	De-bounce control circuit 0: Disable 1: Enable
14:12	EINT6_PRESCALER	Determine the clock cycle period for debounce count. 3'b000: 32768Hz, max 3'b001: 16384Hz 3'b010: 8192Hz 3'b011: 4096Hz 3'b100: 2048Hz, max 3'b101: 1024Hz 3'b110: 512Hz 3'b111: 256Hz, max

Bit(s)	Name	Description
11	EINT6_POL	Activation type of the EINT source 0: Negative polarity 1: Positive polarity
10:0	EINT6_CNT	De-bounce duration in terms of numbers of 32768Hz clock cycles. The cycle length is determined by PRESCALER

151A8190 EINT7_CON EINT 7 De-bounce Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT7_EN	EINT7_PRESCALER				EINT7_POL	EINT7_CNT									
Type	RW	RW				RW	RW									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	EINT7_EN	De-bounce control circuit 0: Disable 1: Enable
14:12	EINT7_PRESCALER	Determine the clock cycle period for debounce count. 3'b000: 32768Hz, max 3'b001: 16384Hz 3'b010: 8192Hz 3'b011: 4096Hz 3'b100: 2048Hz, max 3'b101: 1024Hz 3'b110: 512Hz 3'b111: 256Hz, max
11	EINT7_POL	Activation type of the EINT source 0: Negative polarity 1: Positive polarity
10:0	EINT7_CNT	De-bounce duration in terms of numbers of 32768Hz clock cycles. The cycle length is determined by PRESCALER

151A81A0 EINT8_CON EINT 8 De-bounce Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																

Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT8_EN	EINT8_PRESCALER				EINT8_POL	EINT8_CNT									
Type	RW	RW				RW	RW									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	EINT8_EN	De-bounce control circuit 0: Disable 1: Enable
14:12	EINT8_PRESCALER	Determine the clock cycle period for debounce count. 3'b000: 32768Hz, max 3'b001: 16384Hz 3'b010: 8192Hz 3'b011: 4096Hz 3'b100: 2048Hz, max 3'b101: 1024Hz 3'b110: 512Hz 3'b111: 256Hz, max
11	EINT8_POL	Activation type of the EINT source 0: Negative polarity 1: Positive polarity
10:0	EINT8_CNT	De-bounce duration in terms of numbers of 32768Hz clock cycles. The cycle length is determined by PRESCALER

151A81B0 EINT9 CON EINT 9 De-bounce Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT9_EN	EINT9_PRESCALER				EINT9_POL	EINT9_CNT									
Type	RW	RW				RW	RW									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	EINT9_EN	De-bounce control circuit 0: Disable 1: Enable
14:12	EINT9_PRESCALER	Determine the clock cycle period for debounce count. 3'b000: 32768Hz, max 3'b001: 16384Hz 3'b010: 8192Hz 3'b011: 4096Hz 3'b100: 2048Hz, max 3'b101: 1024Hz 3'b110: 512Hz 3'b111: 256Hz, max
11	EINT9_POL	Activation type of the EINT source 0: Negative polarity 1: Positive polarity
10:0	EINT9_CNT	De-bounce duration in terms of numbers of 32768Hz clock cycles. The cycle length is determined by PRESCALER

151A81C0		EINTA_CON				EINTA De-bounce Control Register											00000000	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16		
Name																		
Type																		
Reset																		
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
Name	EINTA_EN	EINTA_PRESCALER				EINTA_POL	EINTA_CNT											
Type	RW	RW				RW	RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

Bit(s)	Name	Description
15	EINTA_EN	De-bounce control circuit 0: Disable 1: Enable
14:12	EINTA_PRESCALER	Determine the clock cycle period for debounce count. 3'b000: 32768Hz, max 3'b001: 16384Hz 3'b010: 8192Hz 3'b011: 4096Hz 3'b100: 2048Hz, max 3'b101: 1024Hz 3'b110: 512Hz 3'b111: 256Hz, max
11	EINTA_POL	Activation type of the EINT source

Bit(s)	Name	Description
10:0	EINTA_CNT	0: Negative polarity 1: Positive polarity De-bounce duration in terms of numbers of 32768Hz clock cycles. The cycle length is determined by PRESCALER

151A81D0 EINTB_CON EINT B De-bounce Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINTB_EN	EINTB_PRESCALER				EINTB_POL	EINTB_CNT									
Type	RW	RW				RW	RW									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	EINTB_EN	De-bounce control circuit 0: Disable 1: Enable
14:12	EINTB_PRESCALER	Determine the clock cycle period for debounce count. 3'b000: 32768Hz, max 3'b001: 16384Hz 3'b010: 8192Hz 3'b011: 4096Hz 3'b100: 2048Hz, max 3'b101: 1024Hz 3'b110: 512Hz 3'b111: 256Hz, max
11	EINTB_POL	Activation type of the EINT source 0: Negative polarity 1: Positive polarity
10:0	EINTB_CNT	De-bounce duration in terms of numbers of 32768Hz clock cycles. The cycle length is determined by PRESCALER

151A81E0 EINTC_CON EINT C De-bounce Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																

Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINTC_EN	EINTC_PRESCALER			EINTC_POL	EINTC_CNT										
Type	RW	RW			RW	RW										
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	EINTC_EN	De-bounce control circuit 0: Disable 1: Enable
14:12	EINTC_PRESCALER	Determine the clock cycle period for debounce count. 3'b000: 32768Hz, max 3'b001: 16384Hz 3'b010: 8192Hz 3'b011: 4096Hz 3'b100: 2048Hz, max 3'b101: 1024Hz 3'b110: 512Hz 3'b111: 256Hz, max
11	EINTC_POL	Activation type of the EINT source 0: Negative polarity 1: Positive polarity
10:0	EINTC_CNT	De-bounce duration in terms of numbers of 32768Hz clock cycles. The cycle length is determined by PRESCALER

151A81F0	EINTD_CON				EINT D De-bounce Control Register												00000000	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16		
Name																		
Type																		
Reset																		
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
Name	EINTD_EN	EINTD_PRESCALER			EINTD_POL	EINTD_CNT												
Type	RW	RW			RW	RW												
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

Bit(s)	Name	Description
15	EINTD_EN	De-bounce control circuit 0: Disable 1: Enable
14:12	EINTD_PRESCALER	Determine the clock cycle period for debounce count. 3'b000: 32768Hz, max 3'b001: 16384Hz 3'b010: 8192Hz 3'b011: 4096Hz 3'b100: 2048Hz, max 3'b101: 1024Hz 3'b110: 512Hz 3'b111: 256Hz, max
11	EINTD_POL	Activation type of the EINT source 0: Negative polarity 1: Positive polarity
10:0	EINTD_CNT	De-bounce duration in terms of numbers of 32768Hz clock cycles. The cycle length is determined by PRESCALER

151A8200 **EINTE_CON** EINT E De-bounce Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINTE_EN	EINTE_PRESCALER				EINTE_POL	EINTE_CNT									
Type	RW	RW				RW	RW									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	EINTE_EN	De-bounce control circuit 0: Disable 1: Enable
14:12	EINTE_PRESCALER	Determine the clock cycle period for debounce count. 3'b000: 32768Hz, max 3'b001: 16384Hz 3'b010: 8192Hz 3'b011: 4096Hz 3'b100: 2048Hz, max 3'b101: 1024Hz 3'b110: 512Hz 3'b111: 256Hz, max
11	EINTE_POL	Activation type of the EINT source

Bit(s)	Name	Description
10:0	EINTE_CNT	0: Negative polarity 1: Positive polarity De-bounce duration in terms of numbers of 32768Hz clock cycles. The cycle length is determined by PRESCALER

151A8210 EINTF_CON EINT F De-bounce Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINTF_EN	EINTF_PRESCALER				EINTF_POL	EINTF_CNT									
Type	RW	RW				RW	RW									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	EINTF_EN	De-bounce control circuit 0: Disable 1: Enable
14:12	EINTF_PRESCALER	Determine the clock cycle period for debounce count. 3'b000: 32768Hz, max 3'b001: 16384Hz 3'b010: 8192Hz 3'b011: 4096Hz 3'b100: 2048Hz, max 3'b101: 1024Hz 3'b110: 512Hz 3'b111: 256Hz, max
11	EINTF_POL	Activation type of the EINT source 0: Negative polarity 1: Positive polarity
10:0	EINTF_CNT	De-bounce duration in terms of numbers of 32768Hz clock cycles. The cycle length is determined by PRESCALER

151A8220 EINT10_CON EINT 10 De-bounce Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																

Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT10_EN	EINT10_PRESCALER			EINT10_POL	EINT10_CNT										
Type	RW	RW			RW	RW										
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	EINT10_EN	De-bounce control circuit 0: Disable 1: Enable
14:12	EINT10_PRESCALER	Determine the clock cycle period for debounce count. 3'b000: 32768Hz, max 3'b001: 16384Hz 3'b010: 8192Hz 3'b011: 4096Hz 3'b100: 2048Hz, max 3'b101: 1024Hz 3'b110: 512Hz 3'b111: 256Hz, max
11	EINT10_POL	Activation type of the EINT source 0: Negative polarity 1: Positive polarity
10:0	EINT10_CNT	De-bounce duration in terms of numbers of 32768Hz clock cycles. The cycle length is determined by PRESCALER

151A8230 EINT11 CON EINT 11 De-bounce Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT11_EN	EINT11_PRESCALER			EINT11_POL	EINT11_CNT										
Type	RW	RW			RW	RW										
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	EINT11_EN	De-bounce control circuit 0: Disable 1: Enable
14:12	EINT11_PRESCALER	Determine the clock cycle period for debounce count. 3'b000: 32768Hz, max 3'b001: 16384Hz 3'b010: 8192Hz 3'b011: 4096Hz 3'b100: 2048Hz, max 3'b101: 1024Hz 3'b110: 512Hz 3'b111: 256Hz, max
11	EINT11_POL	Activation type of the EINT source 0: Negative polarity 1: Positive polarity
10:0	EINT11_CNT	De-bounce duration in terms of numbers of 32768Hz clock cycles. The cycle length is determined by PRESCALER

151A8240 **EINT12_CON** EINT 12 De-bounce Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT12_EN	EINT12_PRESCALER				EINT12_POL	EINT12_CNT									
Type	RW	RW				RW	RW									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	EINT12_EN	De-bounce control circuit 0: Disable 1: Enable
14:12	EINT12_PRESCALER	Determine the clock cycle period for debounce count. 3'b000: 32768Hz, max 3'b001: 16384Hz 3'b010: 8192Hz 3'b011: 4096Hz 3'b100: 2048Hz, max 3'b101: 1024Hz 3'b110: 512Hz 3'b111: 256Hz, max
11	EINT12_POL	Activation type of the EINT source

Bit(s)	Name	Description
10:0	EINT12_CNT	0: Negative polarity 1: Positive polarity De-bounce duration in terms of numbers of 32768Hz clock cycles. The cycle length is determined by PRESCALER

151A8250 EINT13_CON EINT 13 De-bounce Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT13_EN	EINT13_PRESCALER				EINT13_POL	EINT13_CNT									
Type	RW	RW				RW	RW									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	EINT13_EN	De-bounce control circuit 0: Disable 1: Enable
14:12	EINT13_PRESCALER	Determine the clock cycle period for debounce count. 3'b000: 32768Hz, max 3'b001: 16384Hz 3'b010: 8192Hz 3'b011: 4096Hz 3'b100: 2048Hz, max 3'b101: 1024Hz 3'b110: 512Hz 3'b111: 256Hz, max
11	EINT13_POL	Activation type of the EINT source 0: Negative polarity 1: Positive polarity
10:0	EINT13_CNT	De-bounce duration in terms of numbers of 32768Hz clock cycles. The cycle length is determined by PRESCALER

151A8400 IRQ_SRC monitor IRQ source 0~31 for debug 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	IRQ_SRC															

Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IRQ_SRC															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	IRQ_SRC	monitor IRQ source 0~31 for debug

151A8404 IRQ_SRCM monitor IRQ source 32~63 for debug 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													IRQ_SRCM			
Type													RU			
Reset													0	0	0	0

Bit(s)	Name	Description
3:0	IRQ_SRCM	monitor IRQ source 32~63 for debug

151A8408 EINT_SRC monitor EINT source for debug 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																EINT_SRC
Type																RU
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	EINT_SRC															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16:0	EINT_SRC	monitor EINT source for debug

151A9000 GPT_ISR GPT Interrupt Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															GPT1_I NT	GPT0_I NT
Type															W1C	W1C
Reset															0	0

Bit(s)	Name	Description
1	GPT1_INT	Timer 1 interrupt. Firmware writes 1 to clear this bit, write 0 is meaningless.
0	GPT0_INT	Timer 0 interrupt. Firmware writes 1 to clear this bit, write 0 is meaningless.

151A9004 GPT_IER GPT Interrupt Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															GPT1_I NT_EN	GPT0_I NT_EN

Type																		RW	RW
Reset																		0	0

Bit(s)	Name	Description
1	GPT1_INT_EN	Timer 1 interrupt enable 0: Disable interrupt 1: Enable interrupt
0	GPT0_INT_EN	Timer 0 interrupt enable 0: Disable interrupt 1: Enable interrupt

151A9010 GPT0_CTRL GPT0 Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													RESTART	SPEED	MODE	EN
Type													WO	RW	RW	RW
Reset													0	0	0	0

Bit(s)	Name	Description
3	RESTART	This register will be auto-clear after restart the counter 0: No any change 1: Restart counter
2	SPEED	This register controls the unit of counter. 0: unit of 32 x 32.768/32KHz cycle 1: unit of 1 x 32.768KHz cycle
1	MODE	This register controls the timer to count repeatedly (in a loop) or just one-shot. SW needs to set this register when GPT0_CTRL[0] = 0. 0: One-shot mode is selected. 1: Auto-repeat mode is selected.
0	EN	This register controls timer to start counting or to stop. 0: timer is disabled. 1: timer is enabled

151A9014 GPT0_ICNT

GPT0 Initial Counter Register

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CNT	Initial counting value, in unit of 32 x 32.768/32KHz (or 1 x 32.768KHz) cycle. The unit depends on the value of GPT0_CTRL[2]. The timer runs on 32.768KHz and counts down from this value whenever enabled. When timer counts down to zero, an interrupt is generated. SW needs to set this register when GPT0_CTRL[0] = 0.

151A9020 GPT1_CTRL GPT1 Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													RESTART	SPEED	MODE	EN
Type													WO	RW	RW	RW
Reset													0	0	0	0

Bit(s)	Name	Description
3	RESTART	This register will be auto-clear after restart the counter 0: No any change 1: Restart counter
2	SPEED	This register controls the unit of counter. 0: unit of 32 x 32.768/32KHz cycle 1: unit of 1 x 32.768KHz cycle
1	MODE	This register controls the timer to count repeatedly (in a loop) or just one-shot. SW needs to set this register when GPT1_CTRL[0] = 0.

Bit(s)	Name	Description
0	EN	0: One-shot mode is selected. 1: Auto-repeat mode is selected. This register controls timer to start counting or to stop. 0: timer is disabled. 1: timer is enabled

151A9024 **GPT1_ICNT** GPT1 Initial Counter Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CNT	Initial counting value, in unit of 32 x 32.768/32KHz (or 1 x 32.768KHz) cycle. The unit depends on the value of GPT1_CTRL[2]. The timer runs on 32.768KHz and counts down from this value whenever enabled. When timer counts down to zero, an interrupt is generated. SW needs to set this register when GPT1_CTRL[0] = 0.

151A9030 **GPT2_CTRL** GPT2 Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															SPEED	EN
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	SPEED	This register controls the unit of counter. 0: unit of 32.768/32KHz cycle 1: unit of 1 x 32.768KHz cycle
0	EN	This register controls timer to start counting or to stop. 0: timer is disabled. 1: timer is enabled

151A9034 GPT2_CNT GPT2 Counter Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CNT															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CNT															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CNT	Initial / Counting value, in unit of 32 x 32.768/32KHz cycle. This counter counts from initial value after enable. When GPT2_CTRL[0] (ie. gpt2_en) is 0, this register is used to for counter initial value setting. Its type is R/W. When GPT2_CTRL[0] (ie. gpt2_en) is 1, this register is used to for current counting value reading. Once the gpt2_en is turned on, the current counting value can be read out after 3T 32kHz clock.

151A9040 GPT0_CNT GPT0 Counter Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CNT															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CNT															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CNT	Current counter value, in unit of 32 x 32.768/32KHz cycle (or 1 x 32.768KHz cycle). Once the gpt0_en is turned on, the current counting value can be read out after 3T 32kHz clock.

151A9044 GPT1_CNT GPT1 Counter Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CNT															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CNT															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CNT	Current counter value, in unit of 32 x 32.768/32KHz cycle (or 1 x 32.768KHz cycle). Once the gpt1_en is turned on, the current counting value can be read out after 3T 32kHz clock.

151A9050 GPT3_CTRL GPT3 Control Register 00190000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											OSC_CNT_1US					
Type											RW					
Reset											0	1	1	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPT3_I CLR											GPT3_I NT_EN				GPT3_EN
Type	RW											RW				RW
Reset	0											0				0

Bit(s)	Name	Description
21:16	OSC_CNT_1US	The interval of tick of GPT3 [for 7615].

Bit(s)	Name	Description
15	GPT3_ICLR	When osc_ck is 26MHz, OSC_CNT_1US = 26-1=25. GPT3 interrupt clear. [6630 E2] 0: interrupt clear is disabled 1: interrupt clear is enable
4	GPT3_INT_EN	Enable interrupt of GPT3. 0: GPT3 interrupt is disabled. 1: GPT3 interrupt is enabled.
0	GPT3_EN	Enable of GPT3. 0: GPT3 is disabled. 1: GPT3 is enabled, it will +1 for each 1us tick [6630 E2]

151A9054 GPT3_INIT GPT3 Initial Value 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPT3_INIT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPT3_INIT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	GPT3_INIT	Initial value of GPT3. When GPT3 is disabled, this value will be automatically loaded into GPT3 counter.

151A9058 GPT3_CNT GPT3 Counter Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPT3_CNT															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPT3_CNT															
Type	RU															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	GPT3_CNT	Current counter value of GPT3 When GPT3 is enabled (GPT3_EN=1), the counter will be increased by every 1us tick. This is a free-run counter[6630 E2]

151A905C GPT3_EXPIRE GPT3 Expire Value 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPT3_EXPIRE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPT3_EXPIRE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	GPT3_EXPIRE	Expire value of GPT3. When GPT3 counts to GPT3_EXPIRE, GPT3_int_b will be set to low.

151A9060 GPT4_CTRL GPT4 Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										GPT4_DIV						GPT4_EN
Type										RW						RW
Reset										0	0	0	0	0	0	0

Bit(s)	Name	Description
6:1	GPT4_DIV	This register indicates the frequency of counter = OSC_FREQ/(GPT4_DIV+1). When 1us counter is required, GPT4_DIV = OSC_FREQ-1. GPT4_DIV can't be set to the value < 3, to preevent from
0	GPT4_EN	This register controls counter to start counting or to stop. 0: counter is disabled. 1: counter is enabled

151A9064 GPT4_INIT GPT4 Initial Value 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPT4_INIT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPT4_INIT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	GPT4_INIT	Initial value of GPT4. When GPT4 is disabled, this value will be automatically loaded into GPT4 counter.

151A9068 GPT4_CNT GPT4 Counter Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPT4_CNT															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPT4_CNT															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	GPT4_CNT	Current counter value of GPT4 when GPT4 is enabled (GPT4_EN=1)

151A9070 GPT_DBGSEL GPT debug selection register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									GPT_DBGSEL							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	GPT_DBGSEL	GPT debug selection for debug probe signal

151AA030 WDT_MODE Watchdog Timer Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MODE_KEY												IRQ			ENAB E
Type	WO												RW			RW
Reset	0	0	0	0	0	0	0	0					0			0

Bit(s)	Name	Description
15:8	MODE_KEY	Write access is allowed if MODE_KEY=0x22
3	IRQ	Issue an interrupt instead of a Watchdog Timer reset. For debug purposes, RGU issues an interrupt to the MCU instead of resetting the system. 0 Disable.

Bit(s)	Name	Description
0	ENABLE	1 Enable. Enables the Watchdog Timer. Default watchdog timer is disabled. 0: Disables the Watchdog Timer. 1: Enables the Watchdog Timer.

151AA034 WDT_TIMEOUT Watchdog Time-Out Interval Register 0000FFE0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TIMEOUT											TO_KEY				
Type	RW											WO				
Reset	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0

Bit(s)	Name	Description
15:5	TIMEOUT	The counter is restarted with {TIMEOUT [10:0], 11_1111_1111b}. Thus the Watchdog Timer time-out period is a multiple of $1024 * T32k = 32ms * (TIMEOUT + 1)$ if T32K is ideal. Software needs to use the timeout value for this calculation in order to closely reflect the actual time-out period.
4:0	TO_KEY	Write access is allowed if TO_KEY=08h

151AA038 WDT_RESTART Watchdog Timer Restart Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RESTART_KEY															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESTART_KEY															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RESTART_KEY	Restart the counter if RESTART_KEY=1971h. Only when counter is restarted, the WDT_TIMEOUT and WDT_RST_DT are loaded into the counter

151AA03C WDT_STA Watchdog Timer Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HW_STA	SW_STA														
Type	RU	RU														
Reset	0	0														

Bit(s)	Name	Description
15	HW_STA	Indicates the cause of the watchdog reset. 0: Reset not due to Watchdog Timer. 1: Reset because the Watchdog Timer time-out period expired.
14	SW_STA	Indicates if the watchdog was triggered by software. 0: Reset not due to software-triggered Watchdog Timer. 1: Reset due to software-triggered Watchdog Timer.

151AA040 WDT_RST_DT Watchdog Reset Duration Register 00000FFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RST_DURATION											
Type					RW											
Reset					1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
11:0	RST_DURATION	This register indicates the reset duration when Watchdog Timer times out. However, if the WDT_MODE register IRQ bit is set to 1, an interrupt is issued instead of a reset.

151AA044 WDT_SWRST Watchdog Timer Software Reset Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SWRST_KEY															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	SWRST_KEY	Software-triggered Watchdog Timer reset. If the register content matches the SWRST_KEY, a watchdog reset is issued. However, if the WDT_MODE register IRQ bit is set to 1, an interrupt is issued instead of a reset. SWRST_Key = 1209h

151AA050 WDT_IRQEN_B Watchdog Timer IRQ Enable Register 00000002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															IRQEN_B_1	IRQEN_B_0
Type															RW	RW
Reset															1	0

Bit(s)	Name	Description
1	IRQEN_B_1	active low interrupt enable to AP side, 1: disable, 0: enable
0	IRQEN_B_0	active low interrupt enable to CONN_MCU_CIRQ, 1: disable, 0: enable

151AB000		BT_WR_DATA				UART BT TX Write Data Register											00000000	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16		
Name																		
Type																		
Reset																		
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
Name	BT_WR_DATA																	
Type	RW																	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

Bit(s)	Name	Description
15:0	BT_WR_DATA	BT TX data register. If BT_TX_BSY is low, ARM can write data into this data register. If BT_TX_BSY is high, ARM cannot write data into this register and BT_TX_OVF will hold high. Write Command is asserted to send the output data through the "TXD" pin.

151AB004	WF_WR_DATA					UART WF TX Write Data Register											00000000	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16		
Name																		
Type																		
Reset																		
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
Name	WF_WR_DATA																	
Type	RW																	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

Bit(s)	Name	Description
15:0	WF_WR_DATA	WiFi TX data register. If WF_TX_BSY is low, ARM can write data into this data register. If WF_TX_BSY is high, ARM cannot write data into this register and WF_TX_OVF will hold high. Write Command is asserted to send the output data through the "TXD" pin.

151AB008 STA Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													WF_TX_OVF	BT_TX_OVF	WF_TX_BSY	BT_TX_BSY
Type													RU	RU	RU	RU
Reset													0	0	0	0

Bit(s)	Name	Description
3	WF_TX_OVF	WiFi TX data overflow flag. If WF_TX_BSY is high and ARM write WF_WR_DATA again, this flag would hold high and only cleared by software reset. SW can clear it by write 1 to CTRL1[0].
2	BT_TX_OVF	BT TX data overflow flag. If BT_TX_BSY is high and ARM write BT_WR_DATA again, this flag would hold high and only cleared by software reset. SW can clear it by write 1 to CTRL1[0].
1	WF_TX_BSY	When ARM set the WF_WR_DATA, this flag will set to "1". Data will not transmit until BT_TX_BSY is low. This flag will be low when WF_WR_DATA transmit finished. SW can abort Tx by write 1 to CTRL1[0]. This is for debug purpose.
0	BT_TX_BSY	When ARM set the BT_WR_DATA, this flag will set to "1". Data will not transmit until WF_TX_BSY is low. This flag will be low when BT_WR_DATA transmit finished. SW can abort Tx by write 1 to CTRL1[0]. This is for debug purpose.

151AB00C CTRL1 UART Control 1 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											BAUD_RATE					TXCLR
Type											RW					WO
Reset											0	0				0

Bit(s)	Name	Description
5:4	BAUD_RATE	UART serial port baud rate select. "00" : 115200bps "01" : 230400bps "10" : 460800bps "11" : 921600bps
0	TXCLR	Write this bit "1" to clear TX registers.

151AB010 **BCDF_BASE0** **Baud Rate Divider 0** **000000E1**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							BCDF_BASE0									
Type							RW									
Reset							0	0	1	1	1	0	0	0	0	1

Bit(s)	Name	Description
9:0	BCDF_BASE0	BCDF_BASE0 = TCXO/115200. De-sense UART will support baud from 115200 to 921600. They are 115200, 230400, 460800, and 921600. These baud rates are multiples of 115200. Processor can set baud rate selection register BCDF_RATE[1:0] to obtain what you want. Example: The TCXO=26M, BCDF_BASE0 default is 26M/115200= 0xE1. If you need different Baud Rate, please set 0x800A000C[5:4] = 0 and BCDF_BASE0 = TCXO/Baud Rate. Example: If you need Baud Rate = 3.25M, the BCDF_BASE0 = 26M/3.25M = 0x8.

151AB014 **ADJUST** **Baud Rate Adjust** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									ADJUST							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	ADJUST	Baud rate counter adjustment. The baud rate counter will be BCD register bitwise plus 1.

151AF000 HANG_DET_CTL Hang Detection Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	INT_STS		INT_EN													
Type	W1C		RW													
Reset	0	0	0	0												
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RST_CYC_CNT	HANG_DET_EN
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
31:30	INT_STS	INT status write 1 to clear bit[30] for INT_EN[28] bit[31] for INT_EN[29] 1: INT pending 0: INT not pending
29:28	INT_EN	NMI Interrupt enable bit[28] for PC hang INT enable bit[29] for PC hit INT enable 1: enable

Bit(s)	Name	Description
1	RST_CYC_CNT	0: disable Reset hang cycle counter write 1 to reset, then write 0 to release reset
0	HANG_DET_EN	CPU hang detection enable 1: enable 0: disable

151AF004 HANG_CYC_THRE Hang cycle threshold 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	HANG_CYC_THRE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HANG_CYC_THRE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	HANG_CYC_THRE	Hang cycle threshold If checked PC remains the same for the specified cycle number, it is detected as CPU hang, and INT is issued if enabled.

151AF008 PC_CHK_BITMAP PC check bitmap FFFFFFFC0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PC_CHK_BITMAP															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PC_CHK_BITMAP															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	PC_CHK_BITMAP	Program Counter Check Bitmap Don't check LSB parts to mimic locality. When the check part of PC remains the same, it is thought that PC resides in a loop. 1: check 0: don't check

151AF00C IGN_ADDR_CFG Ignored Address Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									IGN_EN							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	IGN_EN	Ignore enable Bit N is enable bit for ignore address CR N 1: ignore address CR N 0: don't ignore address CR N

151AF010 IGN_ADDR_0 Ignored Address 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	IGN_ADDR_0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IGN_ADDR_0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	IGN_ADDR_0	Ignore address 0

151AF014 **IGN_ADDR_1** **Ignore Address 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	IGN_ADDR_1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IGN_ADDR_1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	IGN_ADDR_1	Ignore address 1

151AF018 **IGN_ADDR_2** **Ignore Address 2** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	IGN_ADDR_2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IGN_ADDR_2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	IGN_ADDR_2	Ignore address 2

151AF01C **IGN_ADDR_3** **Ignore Address 3** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	IGN_ADDR_3															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IGN_ADDR_3															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	IGN_ADDR_3	Ignore address 3

151AF020 IGN_ADDR_4 Ignore Address 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	IGN_ADDR_4															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IGN_ADDR_4															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	IGN_ADDR_4	Ignore address 4

151AF024 IGN_ADDR_5 Ignore Address 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	IGN_ADDR_5															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	IGN_ADDR_5															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	IGN_ADDR_5	Ignore address 5

151AF028 IGN_ADDR_6 Ignore Address 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	IGN_ADDR_6															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IGN_ADDR_6															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	IGN_ADDR_6	Ignore address 6

151AF02C IGN_ADDR_7 Ignore Address 7 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	IGN_ADDR_7															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IGN_ADDR_7															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	IGN_ADDR_7	Ignore address 7

151AF030 **RO_CHK_PC** **current checked PC** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RO_CHK_PC															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RO_CHK_PC															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_CHK_PC	current checked PC

151AF034 **RO_CYC_CNT** **current cycle counter** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RO_CYC_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RO_CYC_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_CYC_CNT	current cycle counter (of current checked PC)

151AF038 **PC_MON_CTL** **PC monitor control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	RST_PC_MON_STS															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PC_MON_EN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	RST_PC_MON_STS	Reset PC monitor status write 1, and then write 0 to reset PC_MON_STS
15:0	PC_MON_EN	PC monitor enable bit[0] is corresponding to MON_PC_CFG0 bit[1] is corresponding to MON_PC_CFG1, etc. 1: enable 0: disable

151AF03C PC_MON_STS PC monitor status 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RO_PC_MON_STS															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RO_PC_MON_STS	Latched PC_MON_STS when INT is triggered If INT is enabled, for SW to find which monitor address is hit 1: monitor enable, and corresponding PC was hit 0: monitor disable, or corresponding PC was not hit

151AF040 MON_PC_CFG0 Monitor PC config 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MON_ADDR_0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MON_ADDR_0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MON_ADDR_0	monitor address

151AF044 MON_PC_CFG1 Monitor PC config 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MON_ADDR_1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MON_ADDR_1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MON_ADDR_1	monitor address

151AF048 MON_PC_CFG2 Monitor PC config 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MON_ADDR_2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MON_ADDR_2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MON_ADDR_2	monitior address

151AF04C MON_PC_CFG3 Monitor PC config 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MON_ADDR_3															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MON_ADDR_3															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MON_ADDR_3	monitior address

151AF050 MON_PC_CFG4 Monitor PC config 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MON_ADDR_4															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MON_ADDR_4															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MON_ADDR_4	montior address

151AF054 MON_PC_CFG5 Monitor PC config 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MON_ADDR_5															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MON_ADDR_5															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MON_ADDR_5	montior address

151AF058 MON_PC_CFG6 Monitor PC config 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MON_ADDR_6															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MON_ADDR_6															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MON_ADDR_6	montior address

151AF05C MON_PC_CFG7 Monitor PC config 7 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	MON_ADDR_7															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MON_ADDR_7															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MON_ADDR_7	monitor address

151AF060 MON_PC_CFG8 Monitor PC config 8 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MON_ADDR_8															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MON_ADDR_8															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MON_ADDR_8	monitor address

151AF064 MON_PC_CFG9 Monitor PC config 9 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MON_ADDR_9															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	MON_ADDR_9															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MON_ADDR_9	monitior address

151AF068 MON_PC_CFG10 Monitor PC config 10 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MON_ADDR_10															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MON_ADDR_10															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MON_ADDR_10	monitior address

151AF06C MON_PC_CFG11 Monitor PC config 11 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MON_ADDR_11															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MON_ADDR_11															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MON_ADDR_11	montior address

151AF070 MON_PC_CFG12 Monitor PC config 12 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MON_ADDR_12															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MON_ADDR_12															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MON_ADDR_12	montior address

151AF074 MON_PC_CFG13 Monitor PC config 13 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MON_ADDR_13															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MON_ADDR_13															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MON_ADDR_13	montior address

151AF078 MON_PC_CFG14 Monitor PC config 14 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	MON_ADDR_14															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MON_ADDR_14															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MON_ADDR_14	monitior address

151AF07C MON_PC_CFG15 Monitor PC config 15 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MON_ADDR_15															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MON_ADDR_15															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MON_ADDR_15	monitior address

151AF080 SW_DBG_CTL SW DEBUG CONTROL 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SW_DBG_CTL															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	SW_DBG_CTL															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SW_DBG_CTL	SW debug index

151AF090 MCU_DBG_IF_CMD MCU_DBG_IF_CMD 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MCU_DBG_IF_CMD															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MCU_DBG_IF_CMD															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MCU_DBG_IF_CMD	MCU_DBG_IF_CMD

151AF094 MCU_DBG_IF_ARG0 MCU_DBG_IF_ARG0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MCU_DBG_IF_ARG0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MCU_DBG_IF_ARG0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MCU_DBG_IF_ARG0	MCU_DBG_IF_ARG0

151AF098 MCU_DBG_IF_ARG1 MCU_DBG_IF_ARG1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MCU_DBG_IF_ARG1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MCU_DBG_IF_ARG1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MCU_DBG_IF_ARG1	MCU_DBG_IF_ARG1

151AF09C MCU_DBG_IF_CTL MCU_DBG_IF_CTL 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																MCU_DBG_IF_SW_IRQ
Type																RW
Reset																0

Bit(s)	Name	Description
0	MCU_DBG_IF_SW_IRQ	MCU_DBG_IF_SW_IRQ 1'b0: Not issue interrupt 1'b1: Issue interrupt

Bit(s)	Name	Description

151AF100	DBG_PC_LOG_CTL				DBG_PC_LOG_CTL								001E06FC			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DBG_PC_LOG_THRESHOLD								DBG_PC_LOG_SEL						DBG_PC_LOG_SEL_SRC	DBG_PC_LOG_EN
Type	RW								RW						RW	RW
Reset	0	0	0	0	0	1	1	0	1	1	1	1	1	1	0	0

Bit(s)	Name	Description
15:8	DBG_PC_LOG_THRESHOLD	DBG_PC_LOG_THRESHOLD
7:2	DBG_PC_LOG_SEL	DBG_PC_LOG_SEL
1	DBG_PC_LOG_SEL_SRC	DBG_PC_LOG_SEL_SRC
		1'b0 : mux selection source from AP/HIF
		1'b1 : mux selection source from MCUSYS
0	DBG_PC_LOG_EN	DBG_PC_LOG_EN

151AF104	DBG_PC_LOG_0				DBG_PC_LOG_0								00000000			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RO_DBG_PC_LOG_0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RO_DBG_PC_LOG_0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_DBG_PC_LOG_0	DBG_PC_LOG_0 (source pc 1)

151AF108 **DBG_PC_LOG_1** **DBG_PC_LOG_1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RO_DBG_PC_LOG_1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RO_DBG_PC_LOG_1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_DBG_PC_LOG_1	DBG_PC_LOG_1 (destination pc 1)

151AF10C **DBG_PC_LOG_2** **DBG_PC_LOG_2** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RO_DBG_PC_LOG_2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RO_DBG_PC_LOG_2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_DBG_PC_LOG_2	DBG_PC_LOG_2 (source pc 2)

151AF110 **DBG_PC_LOG_3** **DBG_PC_LOG_3** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	RO_DBG_PC_LOG_3															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RO_DBG_PC_LOG_3															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_DBG_PC_LOG_3	DBG_PC_LOG_3 (destination pc 2)

151AF114 DBG_PC_LOG_4 DBG_PC_LOG_4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RO_DBG_PC_LOG_4															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RO_DBG_PC_LOG_4															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_DBG_PC_LOG_4	DBG_PC_LOG_4 (source pc 3)

151AF118 DBG_PC_LOG_5 DBG_PC_LOG_5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RO_DBG_PC_LOG_5															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	RO_DBG_PC_LOG_5															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_DBG_PC_LOG_5	DBG_PC_LOG_5 (destination pc 3)

151AF11C DBG_PC_LOG_6 DBG_PC_LOG_6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RO_DBG_PC_LOG_6															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RO_DBG_PC_LOG_6															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_DBG_PC_LOG_6	DBG_PC_LOG_6 (source pc 4)

151AF120 DBG_PC_LOG_7 DBG_PC_LOG_7 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RO_DBG_PC_LOG_7															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RO_DBG_PC_LOG_7															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_DBG_PC_LOG_7	DBG_PC_LOG_7 (destination pc 4)

151AF124 **DBG_PC_LOG_8** **DBG_PC_LOG_8** 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RO_DBG_PC_LOG_8															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RO_DBG_PC_LOG_8															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_DBG_PC_LOG_8	DBG_PC_LOG_8 (source pc 5)

151AF128 **DBG_PC_LOG_9** **DBG_PC_LOG_9** 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RO_DBG_PC_LOG_9															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RO_DBG_PC_LOG_9															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_DBG_PC_LOG_9	DBG_PC_LOG_9 (destination pc 5)

151AF12C **DBG_PC_LOG_10** **DBG_PC_LOG_10** 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	RO_DBG_PC_LOG_10															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RO_DBG_PC_LOG_10															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_DBG_PC_LOG_10	DBG_PC_LOG_10 (source pc 6)

151AF130 DBG_PC_LOG_11 DBG_PC_LOG_11 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RO_DBG_PC_LOG_11															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RO_DBG_PC_LOG_11															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_DBG_PC_LOG_11	DBG_PC_LOG_11 (destination pc 6)

151AF134 DBG_PC_LOG_12 DBG_PC_LOG_12 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RO_DBG_PC_LOG_12															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	RO_DBG_PC_LOG_12															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_DBG_PC_LOG_12	DBG_PC_LOG_12 (source pc 7)

151AF138 DBG_PC_LOG_13 DBG_PC_LOG_13 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RO_DBG_PC_LOG_13															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RO_DBG_PC_LOG_13															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_DBG_PC_LOG_13	DBG_PC_LOG_13 (destination pc 7)

151AF13C DBG_PC_LOG_14 DBG_PC_LOG_14 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RO_DBG_PC_LOG_14															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RO_DBG_PC_LOG_14															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_DBG_PC_LOG_14	DBG_PC_LOG_14 (source pc 8)

151AF140 **DBG_PC_LOG_15** **DBG_PC_LOG_15** 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RO_DBG_PC_LOG_15															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RO_DBG_PC_LOG_15															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_DBG_PC_LOG_15	DBG_PC_LOG_15 (destination pc 8)

151AF144 **DBG_PC_LOG_16** **DBG_PC_LOG_16** 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RO_DBG_PC_LOG_16															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RO_DBG_PC_LOG_16															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_DBG_PC_LOG_16	DBG_PC_LOG_16 (source pc 9)

151AF148 **DBG_PC_LOG_17** **DBG_PC_LOG_17** 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	RO_DBG_PC_LOG_17															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RO_DBG_PC_LOG_17															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_DBG_PC_LOG_17	DBG_PC_LOG_17 (destination pc 9)

151AF14C DBG_PC_LOG_18 DBG_PC_LOG_18 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RO_DBG_PC_LOG_18															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RO_DBG_PC_LOG_18															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_DBG_PC_LOG_18	DBG_PC_LOG_18 (source pc 10)

151AF150 DBG_PC_LOG_19 DBG_PC_LOG_19 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RO_DBG_PC_LOG_19															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	RO_DBG_PC_LOG_19															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_DBG_PC_LOG_19	DBG_PC_LOG_19 (destination pc 10)

151AF154 DBG_PC_LOG_20 DBG_PC_LOG_20 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RO_DBG_PC_LOG_20															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RO_DBG_PC_LOG_20															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_DBG_PC_LOG_20	DBG_PC_LOG_20 (source pc 11)

151AF158 DBG_PC_LOG_21 DBG_PC_LOG_21 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RO_DBG_PC_LOG_21															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RO_DBG_PC_LOG_21															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_DBG_PC_LOG_21	DBG_PC_LOG_21 (destination pc 11)

151AF15C DBG_PC_LOG_22 DBG_PC_LOG_22 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RO_DBG_PC_LOG_22															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RO_DBG_PC_LOG_22															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_DBG_PC_LOG_22	DBG_PC_LOG_22 (source pc 12)

151AF160 DBG_PC_LOG_23 DBG_PC_LOG_23 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RO_DBG_PC_LOG_23															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RO_DBG_PC_LOG_23															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_DBG_PC_LOG_23	DBG_PC_LOG_23 (destination pc 12)

151AF164 DBG_PC_LOG_24 DBG_PC_LOG_24 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	RO_DBG_PC_LOG_24															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RO_DBG_PC_LOG_24															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_DBG_PC_LOG_24	DBG_PC_LOG_24 (source pc 13)

151AF168 DBG_PC_LOG_25 DBG_PC_LOG_25 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RO_DBG_PC_LOG_25															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RO_DBG_PC_LOG_25															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_DBG_PC_LOG_25	DBG_PC_LOG_25 (destination pc 13)

151AF16C DBG_PC_LOG_26 DBG_PC_LOG_26 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RO_DBG_PC_LOG_26															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	RO_DBG_PC_LOG_26															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_DBG_PC_LOG_26	DBG_PC_LOG_26 (source pc 14)

151AF170 DBG_PC_LOG_27 DBG_PC_LOG_27 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RO_DBG_PC_LOG_27															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RO_DBG_PC_LOG_27															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_DBG_PC_LOG_27	DBG_PC_LOG_27 (destination pc 14)

151AF174 DBG_PC_LOG_28 DBG_PC_LOG_28 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RO_DBG_PC_LOG_28															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RO_DBG_PC_LOG_28															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_DBG_PC_LOG_28	DBG_PC_LOG_28 (source pc 15)

151AF178 **DBG_PC_LOG_29** **DBG_PC_LOG_29** 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RO_DBG_PC_LOG_29															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RO_DBG_PC_LOG_29															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_DBG_PC_LOG_29	DBG_PC_LOG_29 (destination pc 15)

151AF17C **DBG_PC_LOG_30** **DBG_PC_LOG_30** 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RO_DBG_PC_LOG_30															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RO_DBG_PC_LOG_30															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_DBG_PC_LOG_30	DBG_PC_LOG_30 (source pc 16)

151AF180 **DBG_PC_LOG_31** **DBG_PC_LOG_31** 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	RO_DBG_PC_LOG_31															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RO_DBG_PC_LOG_31															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_DBG_PC_LOG_31	DBG_PC_LOG_31 (destination pc 16)

151AF200	DBG_GPR_LOG_CTL					DBG_GPR_LOG_CTL							03DE01FC			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						DBG_GPR_SEL										
Type						RW										
Reset						0	1	1	1	1	0					
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DBG_GPR_LOG_THRESHOLD								DBG_GPR_LOG_SEL						DBG_GPR_LOG_SEL_SRC	DBG_GPR_LOG_EN
Type	RW								RW						RW	RW
Reset	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0

Bit(s)	Name	Description
26:21	DBG_GPR_SEL	DBG_GPR_SEL 6'd0~6'd5 : a0~a5 6'd6~6'd14 : s0~s8 6'd15 : ta 6'd16~6'd25 : t0~t9 6'd26~6'd27 : p0~p1 6'd28 : fp 6'd29 : gp 6'd30 : lp 6'd31 : sp
15:8	DBG_GPR_LOG_THRESHOLD	DBG_GPR_LOG_THRESHOLD
7:2	DBG_GPR_LOG_SEL	DBG_GPR_LOG_SEL
1	DBG_GPR_LOG_SEL_SRC	DBG_GPR_LOG_SEL_SRC

Bit(s)	Name	Description
		1'b0 : mux selection source from AP/HIF 1'b1 : mux selection source from MCUSYS
0	DBG_GPR_LOG_EN	DBG_GPR_LOG_EN

151AF204 DBG_GPR_LOG_0 DBG_GPR_LOG_0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RO_DBG_GPR_LOG_0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RO_DBG_GPR_LOG_0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_DBG_GPR_LOG_0	DBG_GPR_LOG_0 (source gpr 1)

151AF208 DBG_GPR_LOG_1 DBG_GPR_LOG_1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RO_DBG_GPR_LOG_1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RO_DBG_GPR_LOG_1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_DBG_GPR_LOG_1	DBG_GPR_LOG_1 (destination gpr 1)

151AF20C DBG_GPR_LOG_2 DBG_GPR_LOG_2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RO_DBG_GPR_LOG_2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RO_DBG_GPR_LOG_2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_DBG_GPR_LOG_2	DBG_GPR_LOG_2 (source gpr 2)

151AF210 DBG_GPR_LOG_3 DBG_GPR_LOG_3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RO_DBG_GPR_LOG_3															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RO_DBG_GPR_LOG_3															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_DBG_GPR_LOG_3	DBG_GPR_LOG_3 (destination gpr 2)

151AF214 DBG_GPR_LOG_4 DBG_GPR_LOG_4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RO_DBG_GPR_LOG_4															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RO_DBG_GPR_LOG_4															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_DBG_GPR_LOG_4	DBG_GPR_LOG_4 (source gpr 3)

151AF218 DBG GPR LOG 5 DBG_GPR_LOG_5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RO_DBG_GPR_LOG_5															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RO_DBG_GPR_LOG_5															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_DBG_GPR_LOG_5	DBG_GPR_LOG_5 (destination gpr 3)

151AF21C DBG GPR LOG 6 DBG_GPR_LOG_6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RO_DBG_GPR_LOG_6															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RO_DBG_GPR_LOG_6															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_DBG_GPR_LOG_6	DBG_GPR_LOG_6 (source gpr 4)

151AF220 **DBG GPR LOG 7** **DBG_GPR_LOG_7** 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RO_DBG_GPR_LOG_7															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RO_DBG_GPR_LOG_7															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_DBG_GPR_LOG_7	DBG_GPR_LOG_7 (destination gpr 4)

151AF224 **DBG GPR LOG 8** **DBG_GPR_LOG_8** 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RO_DBG_GPR_LOG_8															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RO_DBG_GPR_LOG_8															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_DBG_GPR_LOG_8	DBG_GPR_LOG_8 (source gpr 5)

151AF228 **DBG GPR LOG 9** **DBG_GPR_LOG_9** 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	RO_DBG_GPR_LOG_9															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RO_DBG_GPR_LOG_9															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_DBG_GPR_LOG_9	DBG_GPR_LOG_9 (destination gpr 5)

151AF22C DBG_GPR_LOG_10 DBG_GPR_LOG_10 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RO_DBG_GPR_LOG_10															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RO_DBG_GPR_LOG_10															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_DBG_GPR_LOG_10	DBG_GPR_LOG_10 (source gpr 6)

151AF230 DBG_GPR_LOG_11 DBG_GPR_LOG_11 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RO_DBG_GPR_LOG_11															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	RO_DBG_GPR_LOG_11															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_DBG_GPR_LOG_11	DBG_GPR_LOG_11 (destination gpr 6)

151AF234 DBG_GPR_LOG_12 DBG_GPR_LOG_12 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RO_DBG_GPR_LOG_12															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RO_DBG_GPR_LOG_12															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_DBG_GPR_LOG_12	DBG_GPR_LOG_12 (source gpr 7)

151AF238 DBG_GPR_LOG_13 DBG_GPR_LOG_13 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RO_DBG_GPR_LOG_13															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RO_DBG_GPR_LOG_13															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_DBG_GPR_LOG_13	DBG_GPR_LOG_13 (destination gpr 7)

151AF23C DBG GPR LOG 14 DBG_GPR_LOG_14 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RO_DBG_GPR_LOG_14															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RO_DBG_GPR_LOG_14															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_DBG_GPR_LOG_14	DBG_GPR_LOG_14 (source gpr 8)

151AF240 DBG GPR LOG 15 DBG_GPR_LOG_15 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RO_DBG_GPR_LOG_15															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RO_DBG_GPR_LOG_15															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_DBG_GPR_LOG_15	DBG_GPR_LOG_15 (destination gpr 8)

151AF244 DBG GPR LOG 16 DBG_GPR_LOG_16 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	RO_DBG_GPR_LOG_16															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RO_DBG_GPR_LOG_16															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_DBG_GPR_LOG_16	DBG_GPR_LOG_16 (source gpr 9)

151AF248 DBG_GPR_LOG_17 DBG_GPR_LOG_17 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RO_DBG_GPR_LOG_17															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RO_DBG_GPR_LOG_17															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_DBG_GPR_LOG_17	DBG_GPR_LOG_17 (destination gpr 9)

151AF24C DBG_GPR_LOG_18 DBG_GPR_LOG_18 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RO_DBG_GPR_LOG_18															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	RO_DBG_GPR_LOG_18															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_DBG_GPR_LOG_18	DBG_GPR_LOG_18 (source gpr 10)

151AF250 DBG_GPR_LOG_19 DBG_GPR_LOG_19 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RO_DBG_GPR_LOG_19															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RO_DBG_GPR_LOG_19															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_DBG_GPR_LOG_19	DBG_GPR_LOG_19 (destination gpr 10)

151AF254 DBG_GPR_LOG_20 DBG_GPR_LOG_20 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RO_DBG_GPR_LOG_20															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RO_DBG_GPR_LOG_20															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_DBG_GPR_LOG_20	DBG_GPR_LOG_20 (source gpr 11)

151AF258 **DBG GPR LOG 21** **DBG_GPR_LOG_21** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RO_DBG_GPR_LOG_21															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RO_DBG_GPR_LOG_21															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_DBG_GPR_LOG_21	DBG_GPR_LOG_21 (destination gpr 11)

151AF25C **DBG GPR LOG 22** **DBG_GPR_LOG_22** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RO_DBG_GPR_LOG_22															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RO_DBG_GPR_LOG_22															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_DBG_GPR_LOG_22	DBG_GPR_LOG_22 (source gpr 12)

151AF260 **DBG GPR LOG 23** **DBG_GPR_LOG_23** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	RO_DBG_GPR_LOG_23															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RO_DBG_GPR_LOG_23															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_DBG_GPR_LOG_23	DBG_GPR_LOG_23 (destination gpr 12)

151AF264 DBG_GPR_LOG_24 DBG_GPR_LOG_24 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RO_DBG_GPR_LOG_24															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RO_DBG_GPR_LOG_24															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_DBG_GPR_LOG_24	DBG_GPR_LOG_24 (source gpr 13)

151AF268 DBG_GPR_LOG_25 DBG_GPR_LOG_25 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RO_DBG_GPR_LOG_25															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	RO_DBG_GPR_LOG_25															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_DBG_GPR_LOG_25	DBG_GPR_LOG_25 (destination gpr 13)

151AF26C DBG_GPR_LOG_26 DBG_GPR_LOG_26 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RO_DBG_GPR_LOG_26															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RO_DBG_GPR_LOG_26															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_DBG_GPR_LOG_26	DBG_GPR_LOG_26 (source gpr 14)

151AF270 DBG_GPR_LOG_27 DBG_GPR_LOG_27 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RO_DBG_GPR_LOG_27															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RO_DBG_GPR_LOG_27															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_DBG_GPR_LOG_27	DBG_GPR_LOG_27 (destination gpr 14)

151AF274 **DBG GPR LOG 28** **DBG_GPR_LOG_28** 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RO_DBG_GPR_LOG_28															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RO_DBG_GPR_LOG_28															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_DBG_GPR_LOG_28	DBG_GPR_LOG_28 (source gpr 15)

151AF278 **DBG GPR LOG 29** **DBG_GPR_LOG_29** 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RO_DBG_GPR_LOG_29															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RO_DBG_GPR_LOG_29															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_DBG_GPR_LOG_29	DBG_GPR_LOG_29 (destination gpr 15)

151AF27C **DBG GPR LOG 30** **DBG_GPR_LOG_30** 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	RO_DBG_GPR_LOG_30															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RO_DBG_GPR_LOG_30															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_DBG_GPR_LOG_30	DBG_GPR_LOG_30 (source gpr 16)

151AF280 DBG_GPR_LOG_31 DBG_GPR_LOG_31 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RO_DBG_GPR_LOG_31															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RO_DBG_GPR_LOG_31															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RO_DBG_GPR_LOG_31	DBG_GPR_LOG_31 (destination gpr 16)

6.5 Programming Guide

6.5.1 ADMA Programming Guide

6.5.1.1 ADMA Descriptor Format

The format of TX and RX DMAD are shown in following two figures respectively. The lengths of both descriptors are fixed to 8 DWs.

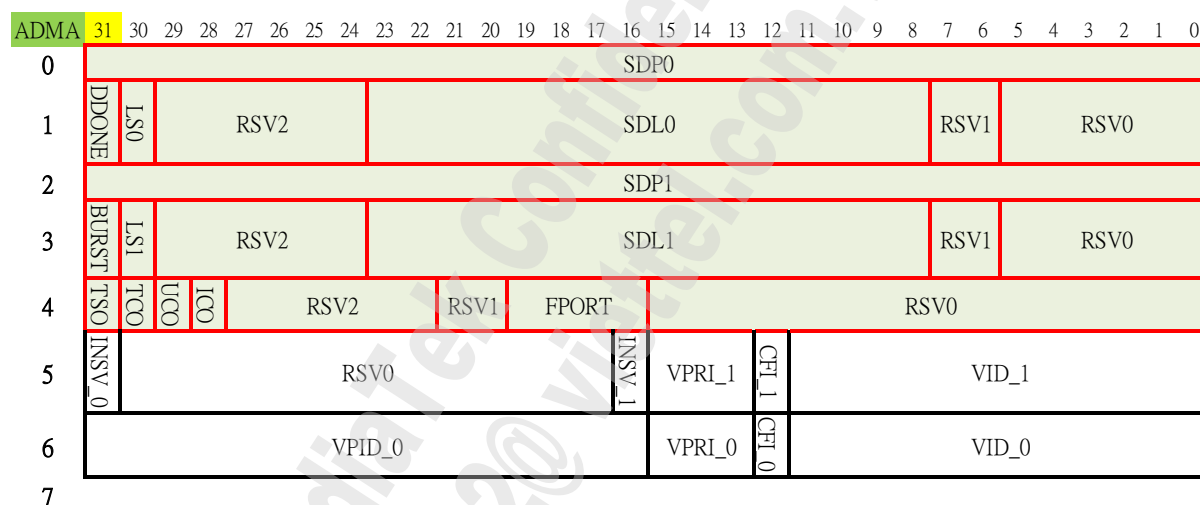


Figure 6-3: ADMA Tx DMA Descriptor format (TX DMAD)

Owing to ADMA supports TX gathering, a single TX packet may be divided into several segments, located in several discontinuous regions in the system memory. A TX DMAD may contain up to two segments, while the end of packet is indicated by *Last Segment (LS0/LS1)* bit. *SDP0/SDP1* stands for *Segment Data Pointer* of segment 0 or 1, which points to the start address of the segment to be sent. *SDL0/SDL1* is the *Segment Data Length*, which defines the length of the segment. Another feature that ADMA supports is *Burst*, which allows a TX ring to occupy the TX channel and consecutively send out an arbitrary number of packets. *DDONE* bit is for coherence checking, which means *DMA DONE*.

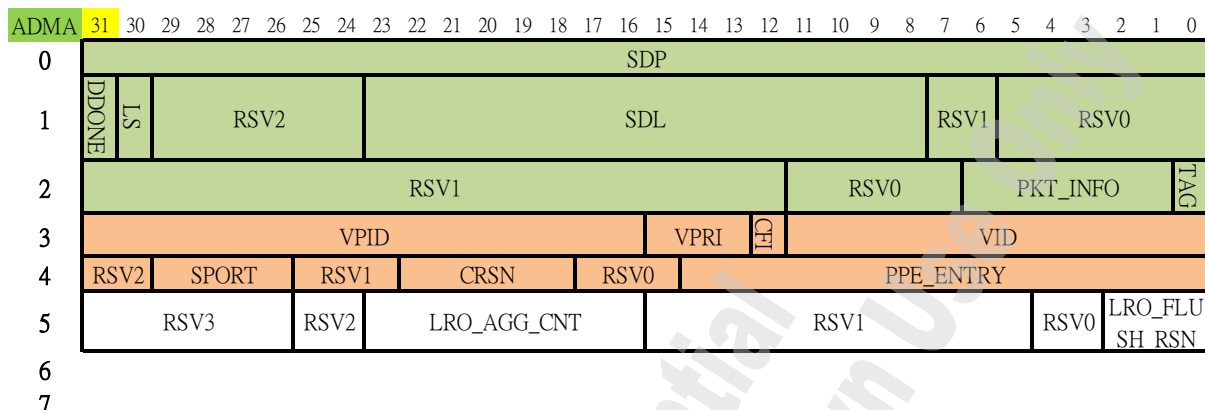


Figure 6-4: ADMA Rx DMA Descriptor format (RX DMAD)

RX DMAD, on the other hand, can only contain one segment. *SDPo*, *SDLo*, *LSO*, and *DDONE* are the same as the ones in TX DMAD and are thus not further explained. It is worth noticing that RX DMAD does not have the *Burst* bit, since the arrival of RX packets are uncontrollable and therefore the bit has no use.

6.5.1.2 Ring Structure

Several descriptors are chained into a descriptor ring, and ADMA may have several rings. There are 4 TX ring and 4 RX ring. By using two indexes for each ring, which are the DMA index and the CPU index, the number of descriptors that needs to be processed is indicated. Figure 1-4 shows an example of a TX descriptor ring being used. In this example, the ring is composed of 8 TX descriptors, abbreviated to *TXD0* through *TXD7*. The DMA TX index and the CPU TX index are abbreviated to *DTX_IDX* and *CTX_IDX*, respectively.

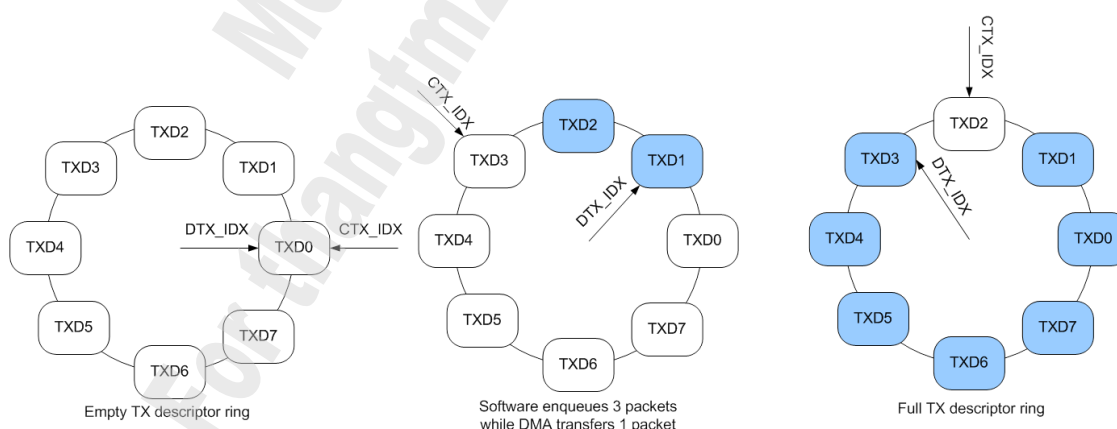


Figure 6-5: DMA descriptor ring

First, after the ring is initialized, both indexes will be pointing at TXDo, indicating an empty ring, as in the left figure. Then when CPU is about to send packets, it will fill in the TX descriptor and increase CTX_IDX by one. As CTX_IDX and DTX_IDX are pointing at different descriptor, DMA knows that there is a packet to be sent. After DMA sends out the packet, DMA will increase DTX_IDX by one. The middle figure shows a case that CPU has prepared three packets to be sent (assuming each packet consumes one descriptor only), while the DMA has already sent out the first one, leaving two remaining packets. The right figure shows the case of the ring being full, in which DTX_IDX advances CTX_IDX by one.

6.5.1.3 Tx Operating Flow

The operating flow of packet transmitting is listed below and the schematic diagram is shown in following figure.

- (a) [CPU] Write the packet into system memory.
- (b) [CPU] Write the packet information into TX DMAD.
- (c) [CPU] Increase CTX_IDX by 1.
- (d) [DMA] Read TX DMAD as $CTX\_IDX \neq DTX\_IDX$.
if (DDONE) Issue an interrupt (TX coherent error).
else Request for and start the data transfer.
- (e) [DMA] Write 1 to DDONE in TX DMAD.
- (f) [DMA] Increase DTX_IDX by 1 and issue an interrupt of transmitting done (TX_DONE_INT).

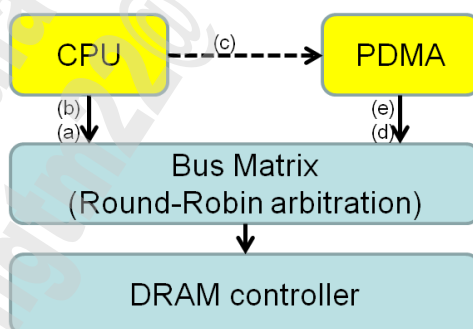


Figure 6-6: Operating flow of DMA TX.

6.5.1.4 Rx Operating Flow

The operating flow of packet receiving is listed below and the schematic diagram is shown in following figure.

- (a) [DMA] Read RX DMAD as packet being received and RX ring not being full
if (DDONE) Issue an interrupt (RX coherent error).
else Request for and start the data transfer.

- (b) [DMA] Write the packet into system memory, update RX DMAD, increase *DRX_IDX* by 1, and issue an interrupt of receiving done (*RX_DONE_INT*).
- (c) [CPU] Read *DRX_IDX* as the interrupt is asserted.
- (d) [CPU] Read out the RX DMAD and the corresponding packet.
- (e) [CPU] Update RX DMAD to return it back to DMA.
- (f) [CPU] Increase *CRX_IDX* by 1.

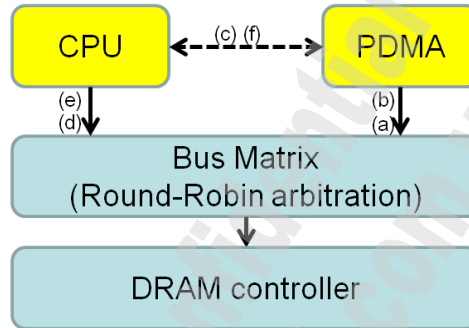


Figure 6-7: Operating flow of DMA RX.

6.5.1.5 Descriptor Ring Initialization

TX/RX ring #0 for example.

Programming Sequence	Memo
Reset DMA TX/RX descriptor ring #0 index	
*ADMA_RST_IDX. RST_DRX_IDXo = 0x1;	
*ADMA_RST_IDX. RST_DTX_IDXo = 0x1;	
*ADMA_RST_IDX. RST_DRX_IDXo = 0x0;	
*ADMA_RST_IDX. RST_DTX_IDXo = 0x0;	
Initialize the TX descriptor	
Software fills the fields of descriptor, and keeps “DDONE” bit = 1	
*ADMA_TX_BASE_PTR_o = TX Ring #0 Base Pointer;	//8-DW aligned address
*ADMA_TX_MAX_CNT_o = TX Ring #0 Maximum Count;	//The maximum number of TXD count in TX Ring #0
*ADMA_TX_CTX_IDX_o = TX Ring #0 CPU pointer;	//Point to the next TXD CPU wants to use
Initialize the RX Ring #0 descriptor	
Software fills the fields of descriptor, and keeps “DDONE” bit = 1	
*ADMA_RX_BASE_PTR_o = RX Ring #0 Base Pointer;	//8-DW aligned address

* ADMA_RX_MAX_CNT_o = RX Ring #0 Maximum Count;	//The maximum number of RXD count in RX Ring #0
* ADMA_RX_CRX_IDX_o = RX Ring #0 CPU pointer;	//Point to the next RXD CPU wants to use
Enable TX/RX Interrupt	
* ADMA_INT_STATUS = 0xFFFFFFFF Check *INT_STATUS, it should be 0x0	// Write 1 Clear the interrupt status register // Read back and make sure interrupt status is clear
*INT_MASK=0x000F000F	//Enable Tx and Rx DMA done interrupt as example (This step can be skip if using polling mode)
Enable TX/RX DMA	
*ADMA_GLO_CFG. RX_2B_OFFSET= 0x0; *ADMA_GLO_CFG. CSR_CLKGATE_BYP = 0x1; *ADMA_GLO_CFG. BYTE_SWAP = 0x0; *ADMA_GLO_CFG. BIG_ENDIAN = 0x0; *ADMA_GLO_CFG. TX_WB_DDONE = 0x1; *ADMA_GLO_CFG. RX_DMA_EN = 0x1; *ADMA_GLO_CFG. TX_DMA_EN = 0x1;	

6.5.1.6 Issue a Data Moving Request

TX/RX ring #0 for example.

Programming Sequence	Memo
Specify RX descriptor	
Write data destination address into DMAD “SDPo” field	
Write data moving length into DMAD “SDLo” field	
Write DMAD “LSO” = 1 (If this is the last segment descriptor)	// Last segment of this transaction
Write DMAD “DDONE” = 0	// DDONE is updated last
Read back RX descriptor	
Check the content of RX descriptor	// This step is optional but can prevent coherent issue (make sure descriptor is updated before kick Off Rx)
Kick Off RX Request	
If (ADMA_RX_CRX_IDX_o == (ADMA_RX_MAX_CNT_o - 1)) *ADMA_RX_CRX_IDX_o = 0; else *ADMA_RX_CRX_IDX_o = ADMA_RX_CRX_IDX_o + 1;	Increase CRX index
Specify TX descriptor	

Write data source address into DMAD “SDPo” field	// update SDP1 if needed
Write other DMAD field	// update other Tx info field if needed
Write data moving length into DMAD “SDL0” field	// update SDL1 if needed
Write “LSO” = 1 (If this is the last segment descriptor)	//
Write “DDONE” = 0	// DDONE is updated last
Read back TX descriptor	
Check the content of TX descriptor	// This step is optional but can prevent coherent issue (make sure descriptor is updated before kick Off Tx)
Kick Off TX Request	
If (ADMA_TX_CTX_IDX_o == (ADMA_TX_MAX_CNT_o - 1)) * ADMA_TX_CTX_IDX_o = 0; else * ADMA_TX_CTX_IDX_o = ADMA_TX_CTX_IDX_o + 1;	Increase CTX index

[Caution]

RX flow

- CPU must confirm that RX descriptor “DDONE”=1, before retrieve the corresponding recycled descriptor/buffer.
- CPU should finish whole data moving information field in RX descriptor, before set “DDONE” = 0 in last step.

TX flow

- CPU should finish whole data moving information field in TX descriptor, before set “DDONE” = 0 in last step.
- CPU must confirm that TX descriptor “DDONE”=1, before retrieve the corresponding recycled descriptor/buffer.

6.5.2 QDMA Programming Guide

6.5.2.1 QDMA Descriptor Format

The format of TX and RX descriptor are shown in following two figures respectively. The lengths of both descriptors are fixed to 8 DWs.

QDMA BASE	SDP	32	Segment Data Pointer
	SDL	16	Segment Data Length
	LS	1	Last Segment
	DDONE	1	Indicate DMA has transfer the segment pointed by this TX desc. and change the owner to CPU
	NDP	32	Next Descriptor Pointer, NDP[1:0] must be 0
	BURST	1	when set, the scheduler can not hand-over to other TS queues. Should go on to transmit the next packet
	SWC	1	Desc. From SW forward chain
	PQID	8	QDMA TX Physical Queue ID
CPU PATH	FPORT	4	Force forwarding PSE port
	TSO	1	TCP segmentation offload enable
	TCO	1	TCP checksum offload enable
	UCO	1	UDP checksum offload enable
	ICO	1	IP checksum offload enable
	VQIDO	1	VQID offload enable
	VQID	10	QDMA TX Virtual Queue ID (VQIDO=0)
	IPOFST	7	IP header offset, SDP+IPOFST=pointer to IP header(VQIDO=1)
	PROT	3	Protocol identification for HW calculating VQ ID (VQIDO=1), (0:L2 bridge /1:IPv4 NAT /2:IPv4 NAPT /3:IPv6 3T /4:IPv6 5T)
	VID_0	12	1'st(outer) VLAN ID Index
	CFI_0	1	1'st(outer) VLAN Canonical Format Indicator
	VPRI_0	3	1'st(outer) VLAN priority tag to be inserted
	VPID_0	16	1'st(outer) VALN Protocol ID
	INSV_0	1	1'st(outer) VLAN Insertion, it can support TX special tag for external switch
	VID_1	12	2'nd(inner) VLAN ID Index
	CFI_1	1	2'nd(inner) VLAN Canonical Format Indicator
	VPRI_1	3	2'nd(inner) VLAN priority tag to be inserted

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SDP																															
NDP																															
DONE	LS	RSV2					SDL															RSV1		RSV0							
		SWC	RSV5					PQID					RSV3		RSV2		FPORT			RSV1		RSV0									
	URST		TCO	UCO	ICO	RSV3	QID0	RSV2	VQID					RSV1		IPOFST					RSV0		PROT								
		RSV0							ISV1	VPRI_1		PRI_1	VID_1																		
VPID_0					VPRI_0		PRI_0	VID_0																							

Figure 6-8: QDMA Tx descriptor format

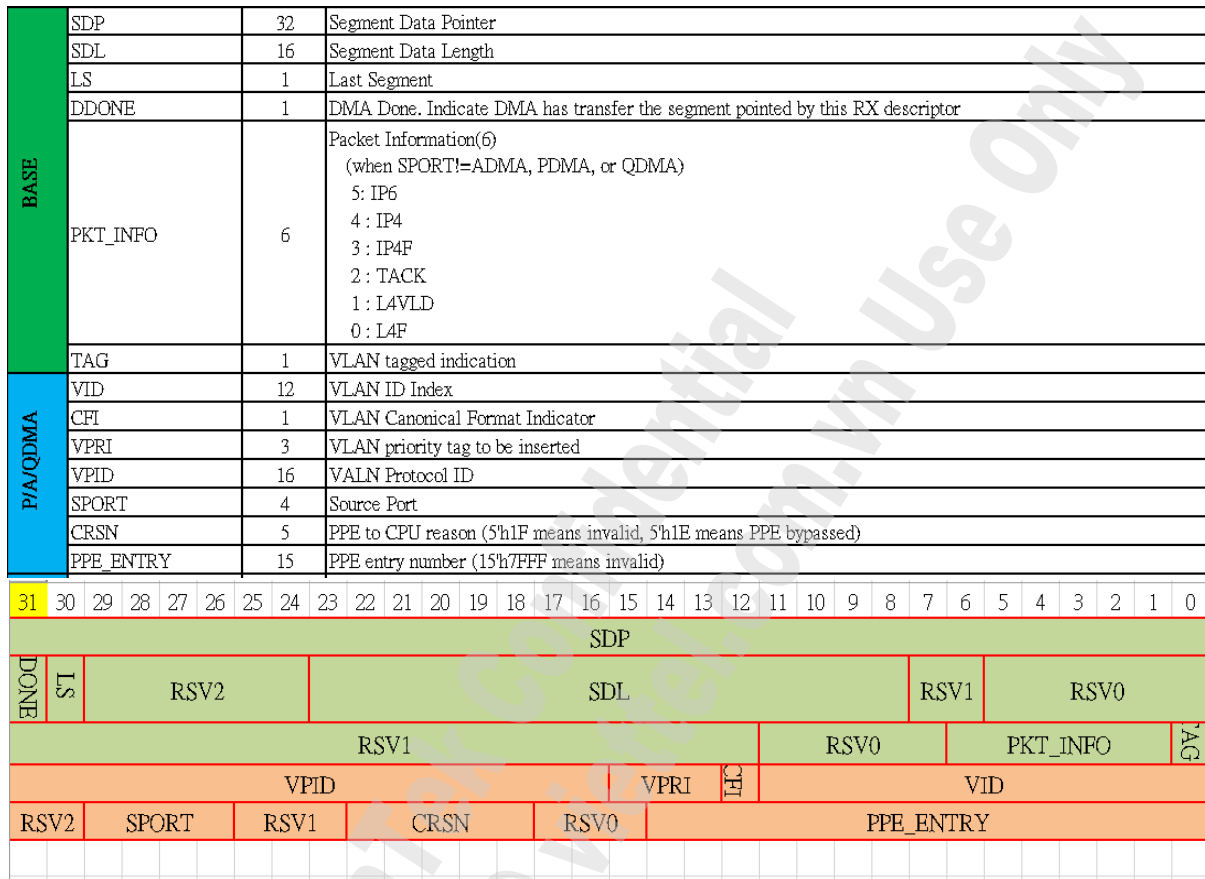


Figure 6-9: QDMA Rx descriptor format

6.5.2.2 Rx Descriptor Ring Initialization

RX ring #0 for example.

Programming Sequence	Memo
Reset QDMA RX descriptor ring #0 index	
Offset 0x4608 *QDMA_RST_IDX. RST_DRX_IDXo = 0x1;	
Offset 0x4608 *QDMA_RST_IDX. RST_DRX_IDXo = 0x0;	
QDMA RX descriptor ring #0 initialization	
Offset 0x4500 *QRX_BASE_PTR_o = RX Ring #0 Base Pointer;	
Offset 0x4504	

*QRX_MAX_CNT_o = RX Ring #0 Maximum Count;	
Specify the RX descriptor content with the base address and size of allocated packet buffer for RX packets	
Software fills the fields of descriptor	
Enable RX DMA	
Offset 0x4604	//
*QDMA_GLO_CFG. RX_DMA_EN = 0x1;	//
*QDMA_GLO_CFG. QDMA_BT_SIZE = 0x2;	//16 DWORDs (64-bytes), depends on project's bus fabric
*QDMA_GLO_CFG. BIG_ENDIAN = 0x0;	//
*QDMA_GLO_CFG. DESC_32B_E = 0x0;	//fetch the next RX descriptor by align 16-Byte
*QDMA_GLO_CFG. BYTE_SWAP = 0x0;	//
*QDMA_GLO_CFG. CSR_CLKGATE = 0x1;	//QDMA clock is gating as idle
*QDMA_GLO_CFG. RX_2B_OFFSET = 0x0;	//Rx-buffer will be 4-byte offset

6.5.2.3 Tx Descriptor Ring Initialization

TX ring #0 for example.

Programming Sequence	Memo
Reset QDMA TX descriptor ring #0 index	
Offset 0x4608	
*QDMA_RST_IDX. RST_DTX_IDXo = 0x1;	
Offset 0x4608	
*QDMA_RST_IDX. RST_DTX_IDXo = 0x0;	
Specify the TX descriptor content with the base address and size of allocated packet buffer for TX packets, for Software forwarding path	
Software fills the fields of descriptor	
QDMA TX Forward Queue initialization (for Software Forwarding Path)	
Offset 0x4700	
* QTX_CTX_PTR = a SW assigned null descriptor pointer;	
Offset 0x4704	
* QTX_DTX_PTR = a SW assigned null descriptor pointer;	
QDMA TX Release Queue initialization (for Software Forwarding Path)	
Offset 0x4710	
* QTX_CRX_PTR = a SW assigned null descriptor pointer;	
Offset 0x4714	
* QTX_DRX_PTR = a SW assigned null descriptor pointer;	

Software prepares a descriptor link list and allocates the related packet buffers, for Hardware forwarding path

Software fills the fields of descriptor

QDMA TX Free Queue initialization (for Hardware Forwarding Path)

Offset 0x4720 *QDMA_FQ_HEAD = Free Page Head Pointer;	//SW assigned head pointer of descriptor link list
Offset 0x4724 *QDMA_FQ_TAIL = Free Page Tail Pointer;	//SW assigned tail pointer of descriptor link list
Offset 0x4728 *QDMA_FQ_CNT = Free Page Counter;	//SW assigned free buffer count of descriptor link list
Offset 0x472C *QDMA_FQ_BLEN = Free Page Buffer Length;	

(Optional: To Enable Virtual Queue for SFQ/DRR, TX ring #0 for example)

Specify Virtual Queue Group #0 Comprises How Many Virtual Queues

Offset 0x4690 *VQTX_NUM. VQTX_NUM_0 = Number of virtual queues in virtual queue group #0;	
Offset 0x47C0 *VQTX_0_3_BIND_QID. VQTX_0_BIND_QID = Virtual Queue Group#0 binds to which Physical Queue;	//VQ Group binds to Physical Queue #n.
Offset 0x46B0 *VQTX_VLD_CFG. VQTX_VLD_STRG_0 = VQ valid bit map starting from register slice #n;	//1 VQ valid register slice comprises 16 bit map. The number of VQ valid register slices for 1 VQ group depends on the setting of "VQTX_NUM_#", and hardware allocates groups for each VQ group automatically.
Offset 0x468C *VQTX_INVLD_PTR = An invalid address of this system;	//The pointer address indicates an invalid virtual queue head/tail pointer. Either "VQHPTR" or "VQTPTR" of VQ table is equal to this invalid pointer VQTX_INVLD_PTR, which means there is no valid packet in this virtual queue.

Allocate Virtual Queue Table into DRAM for Virtual Queue Group #0

Software writes virtual queue table data structure into DRAM

Offset 0x4580 *VQTX_TB_BASE_0 = TX Virtual Queue Table #0 Base Address, for Virtual Queue Group #0;	

Select the Virtual Queue Scheduling Mode

Offset 0x4598 *VQTX_SCH. VQTX_SCH_0 = scheduling strategy;	//0: SFQ (packet base round robin) 1: DRR (deficit round robin)

There are different setting between SFQ and DRR, please refer QoS setting section before enable TX DMA.

Enable TX DMA

Offset 0x4604	//
*QDMA_GLO_CFG.TX_DMA_EN = 0x1;	//
*QDMA_GLO_CFG.QDMA_BT_SIZE = 0x2;	//16 DWORDs (64-bytes), depends on project's bus fabric
*QDMA_GLO_CFG.BIG_ENDIAN = 0x0;	//
*QDMA_GLO_CFG.TX_WB_DDONE = 0x0;	//
*QDMA_GLO_CFG.NDP_CO_PRO = 0x1;	//Next Descriptor Pointer Coherence Protection
*QDMA_GLO_CFG.BYTE_SWAP = 0x0;	//
*QDMA_GLO_CFG.CSR_CLKGATE = 0x1;	//QDMA clock is gating as idle

6.5.2.4 Traffic Shaper Programming Guide

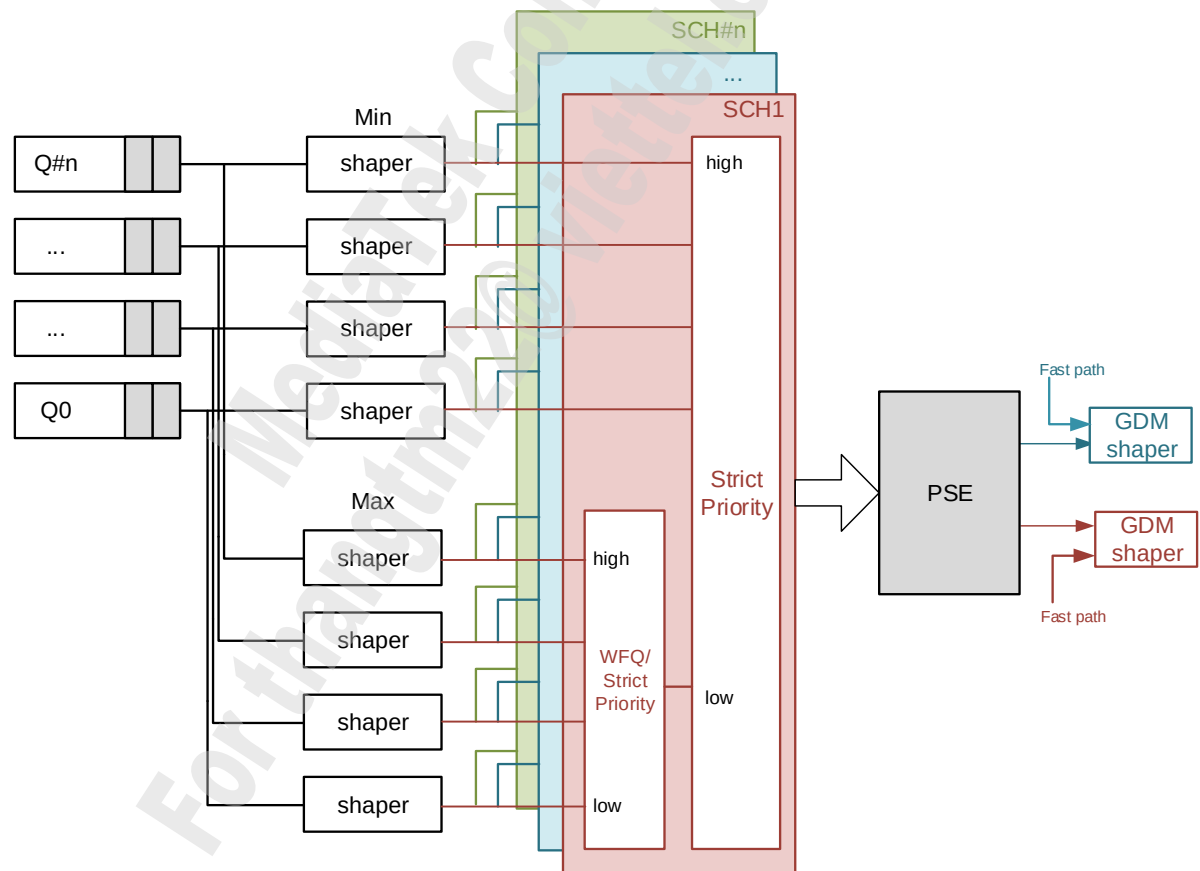


Figure 6-10: QDMA Traffic Shaper Architecture

Set the shaper of Physical Queue, Physical Queue #0 for example

Set the Clock of Scheduler Bucket	
Offset 0x4604 *QDMA_GLO_CFG. BKTCLK_CTRL = 0x0;	//Scheduler bucket clock is 125Mhz
Set the Physical Queue Configuration Page	
Offset 0x4604 *QDMA_GLO_CFG. QTX_CFG_PAGE = 0x0;	// For Example: Select page n =0, switch to physical queue #0~15 configuration registers
Per Physical Queue Buffer Reservation	
Offset 0x4400 *QTX_CFG_o. HW_RESV_CNT= 0x4; *QTX_CFG_o. SW_RESV_CNT= 0x4;	// Reserved buffer number for the packets from HW/SW path
Assign to Scheduler1/2/3/4	
Offset 0x4404 *QTX_SCH_o. TX_SCH_SEL = 0x1;	//Assign to SCH2
Bucket Setting	
Offset 0x4604 *QDMA_GLO_CFG. LEAKY_BK = 0x0;	//Token Bucket setting
Offset 0x4404 *QTX_SCH_o. BUCKET_DEP = 0x0;	
Weighted Fair Queuing Setting	
Offset 0x4404 * QTX_SCH_o. MAX_RATE_WGHT = 0x2;	// The weight to compete with other physical queue // Only valid when this scheduler SCH_MAX_WFQ = 0x1

Set the Scheduler, Scheduler #2 for example

Set Rate Limitation	
Offset 0x4798 *QDMA_TX_SCH1_SCH2. SCH2_LEAKY_BK = 0x0; *QDMA_TX_SCH1_SCH2. SCH2_BUCKET_DEP = 0x0; *QDMA_TX_SCH1_SCH2. SCH2_RATE_EN = 0x1; *QDMA_TX_SCH1_SCH2. SCH2_RATE_MAN = 0x1; *QDMA_TX_SCH1_SCH2. SCH2_RATE_EXP = 0x4;	//Enable rate limitation SCH2_RATE_EXP= 0x4 means select the value of QDMA_RATE_EXP4 (default:0x64) SCH2_RATE = 125M*(SCH2_RATE_MAN/SCH2_RATE_EXP)*8 bps = 125M*(1/QDMA_RATE_EXP4) = 125M*(1/100)*8 = 10Mbps
Bucket Setting	
Offset 0x4798 *QDMA_TX_SCH1_SCH2. SCH2_LEAKY_BK = 0x0; *QDMA_TX_SCH1_SCH2. SCH2_BUCKET_DEP = 0x0;	//Token Bucket setting

Weighted Fair Queuing or Strict Priority

Offset 0x4798	// 0x1: Use Weighted Fair Queuing strategy to select the physical queue for the rate between MN and MAX rate.
*QDMA_TX_SCH1_SCH2. SCH2_MAX_WFQ = 0x1;	// 0x0: Use Strict Priority strategy to Select the physical queue for the rate between MN and MAX rate, queue #0 has lowest priority.

6.5.2.5 Flow Control, RED (Random Early Drop) for Physical Queue

Set the Clock of Scheduler Bucket

Offset 0x4604	
*QDMA_GLO_CFG. BKTCLK_CTRL = 0x0;	//Scheduler bucket clock is 125Mhz

Switch Physical Queue Configuration Page

Offset 0x4604	// For Example: Select page n=0, switch to physical queue #0~15 configuration registers
*QDMA_GLO_CFG. QTX_CFG_PAGE = 0x0;	

Virtual Queue Flow Control Setting, Enable Fullest VQ Dropping Packet

Offset 0x4610

*QDMA_FC_THRES. SW_DROP_FSTVQ_MODE = 0x0;

*QDMA_FC_THRES. SW_DROP_MODE = 0x1;

*QDMA_FC_THRES. SW_DROP_FSTVQ = 0x0;

*QDMA_FC_THRES. SW_DROP_FFA = 0x1;

*QDMA_FC_THRES. SW_DROP_EN = 0x1;

*QDMA_FC_THRES. HW_DROP_FSTVQ_MODE = 0x0;

*QDMA_FC_THRES. HW_DROP_MODE = 0x1;

*QDMA_FC_THRES. HW_DROP_FSTVQ = 0x0;

*QDMA_FC_THRES. HW_DROP_FFA = 0x1;

*QDMA_FC_THRES. HW_DROP_EN = 0x1;

*QDMA_FC_THRES. SHARE_SW_TH = 0x4;

*QDMA_FC_THRES. SHARE_HW_TH = 0x4;

*QDMA_FC_THRES. FREE_TH = 0x4;

*QDMA_FC_THRES. RING_TH = 0x4;

Enable PQ#0 RED(Random Early Discard)

Offset 0x462C	
*QDMA_DROP_PREC. SW_DROP_PREC[0] = 0x1;	//Enable drop by FFA percentage, turn on the RED (Random Early Discard).
*QDMA_DROP_PREC. HW_DROP_PREC[0] = 0x1;	

6.5.2.6 MIB Interface

Enable Virtual Queue MIB counter

Offset 0x46BC

* QTX_MIB_IF. VQTX_MIB_EN= 0x1;	
MIB clear mode	
Offset 0x46BC * QTX_MIB_IF. VQTB_MIB_RC_DIS= 0x0;	// Default the MIB content will be cleared after read access // If user wants to keep the MIB value after read access, must setting this bit to 1. // User should not write the virtual queue MIB information in DRAM directly, it will induce coherence issue and cause wrong MIB record.
Specify the Intended Physical/Virtual Queue ID	
Offset 0x46BC * QTX_MIB_IF. QTX_MIB_QID= 0x0; * QTX_MIB_IF. QTX_MIB_VQID= 0x5;	//For example, user wants to access the MIB of PQ#0/VQ#5
Read MIB Registers	
Offset 0x46C0 *VQTX_MIB_PCNT;	// TX Virtual Queue MIB Packet Count
Offset 0x46C4 *VQTX_MIB_DPCNT;	// TX Virtual Queue MIB Drop Packet Count
Offset 0x46C8 *VQTX_MIB_BCNTL;	// TX Virtual Queue MIB Byte Count Low Bytes
Offset 0x46CC *VQTX_MIB_BCNTH;	// TX Virtual Queue MIB Byte Count High Bytes
Offset 0x46D0 *QTX_MIB_PCNT;	// TX Physical Queue MIB Forward Packet Count
Offset 0x46D4 *QTX_MIB_DPCNT;	// TX Physical Queue MIB Dropped Packet Count
Offset 0x46D8 *QTX_MIB_BCNTL;	//TX Physical Queue MIB Byte Count Low Bytes
Offset 0x46DC *QTX_MIB_BCNTH;	//TX Physical Queue MIB Byte Count High Bytes